Designing Analog and RF Circuits in Nanoscale CMOS Technologies:

Scale the Supply, Reduce the Area and Use Digital Gates.

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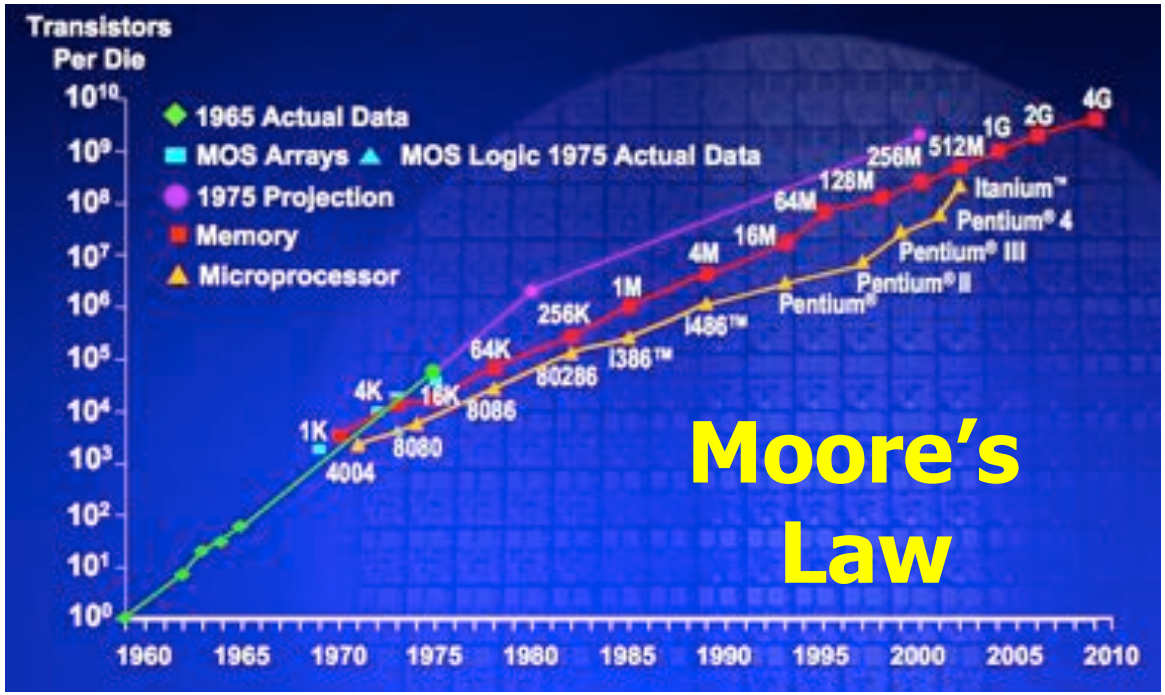
On sabbatical from: Columbia University (New York)

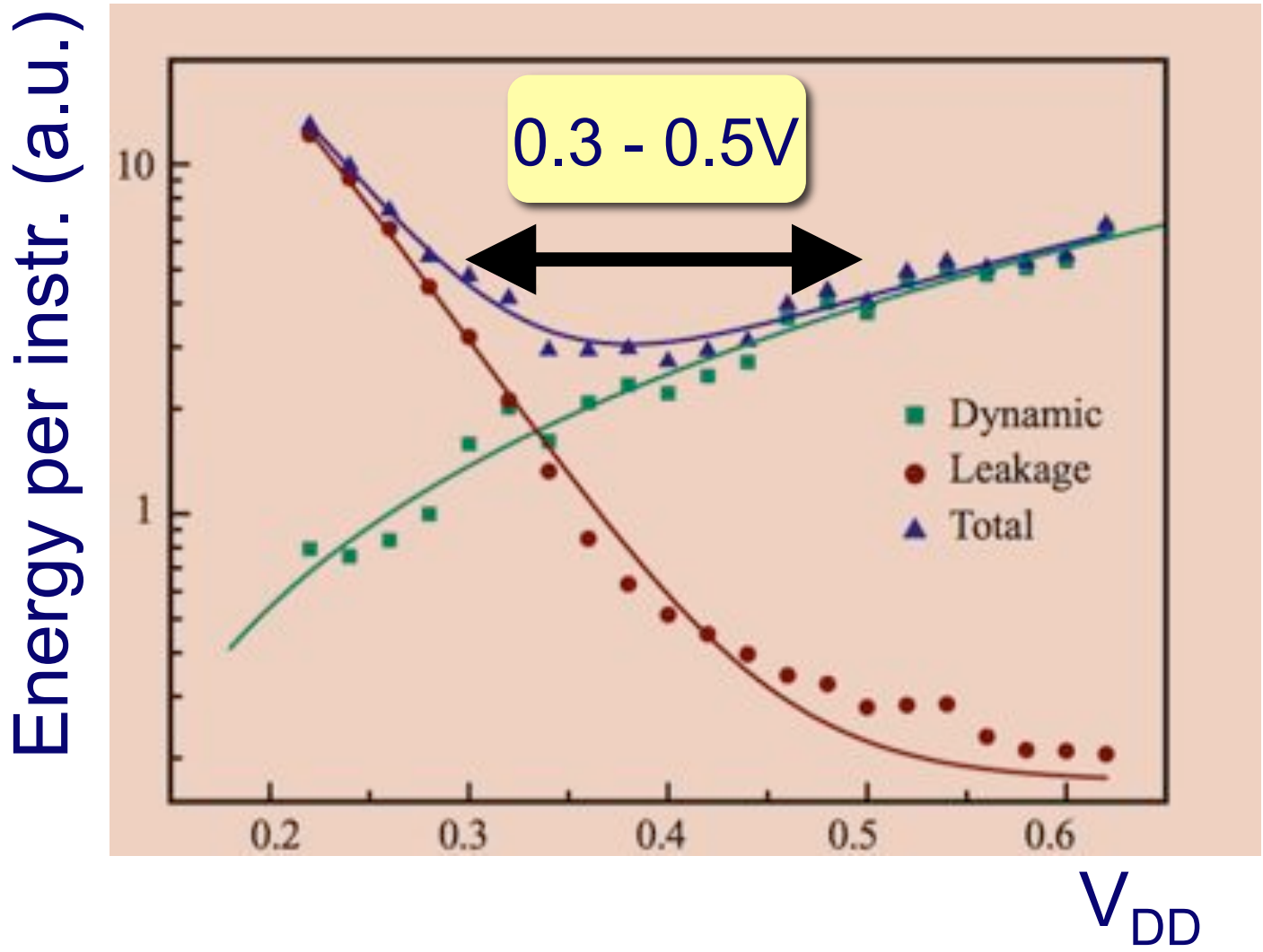
4 Decades of Exponential Growth



G. Moore, "No Exponential is forever…, but we can delay forever," ISSCC 2003

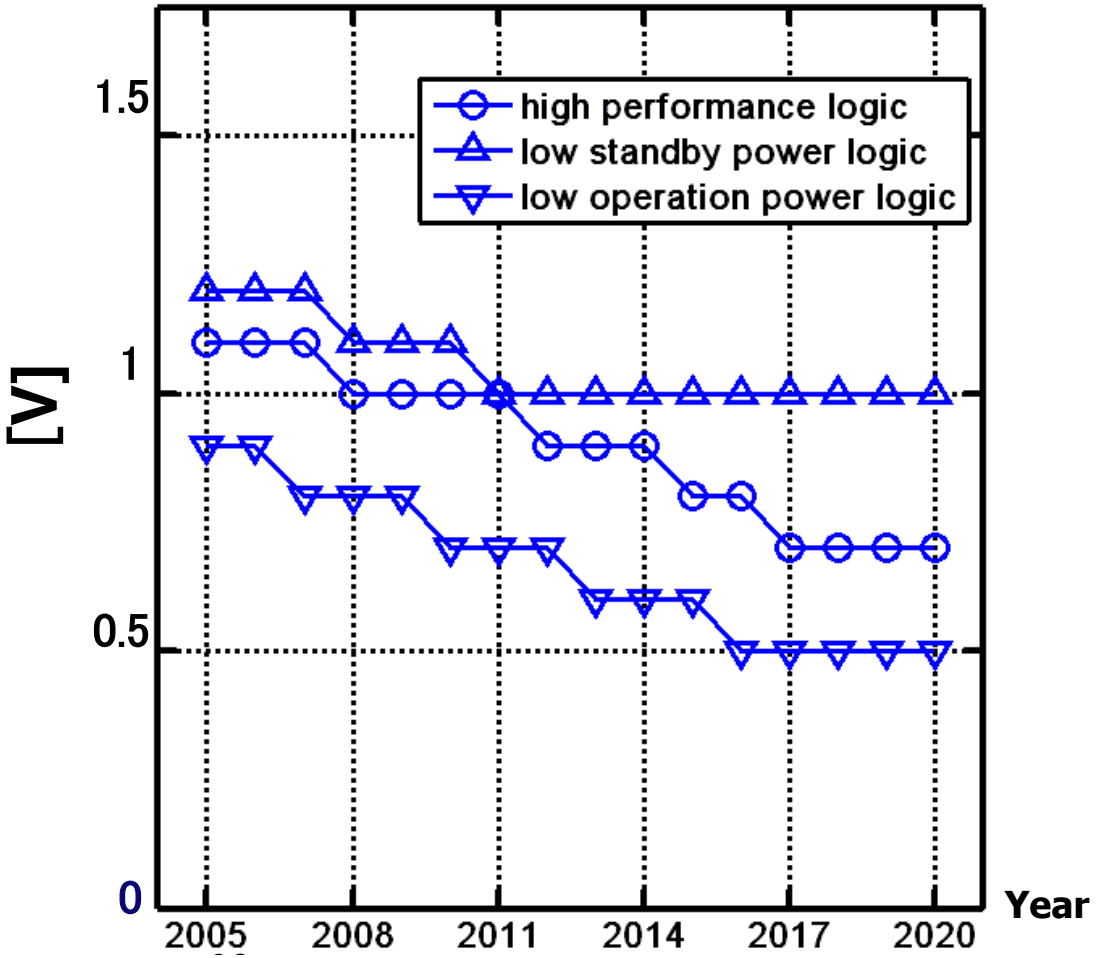
- IC Technology Progress ≡ Device Scaling
- IC Design Progress ≡ More Integration
  - Analog, RF, digital … on a Chip = System on Chip
- Next, highly scaled technologies…

Lowest Energy Digital V_{DD}



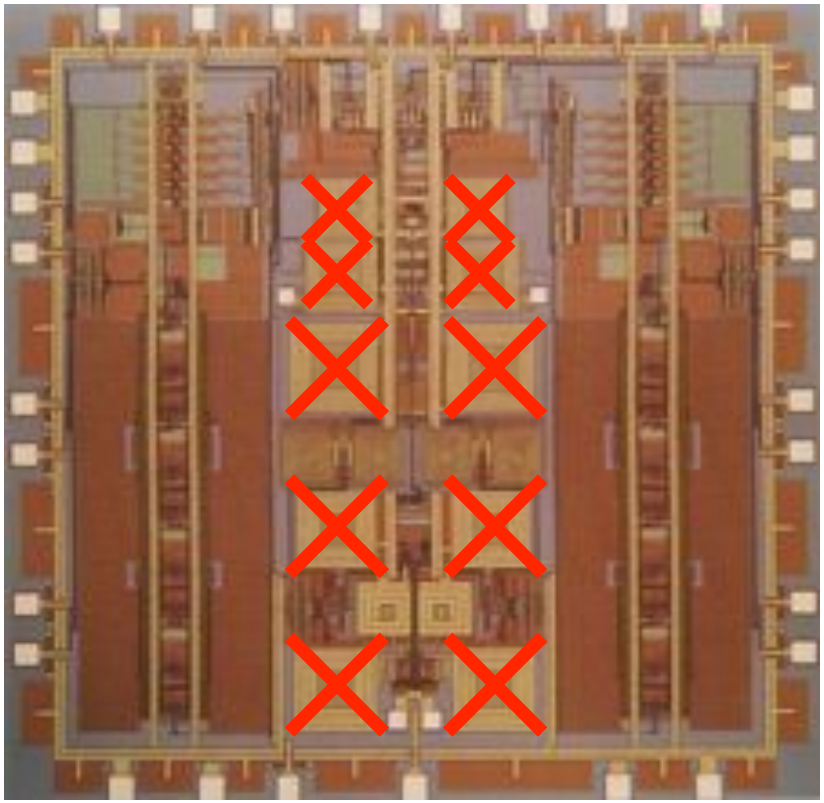
- [Hanson 2006] 8-bit microprocessor in 0.13um CMOS

V_{DD} Scaling for Nanoscale CMOS

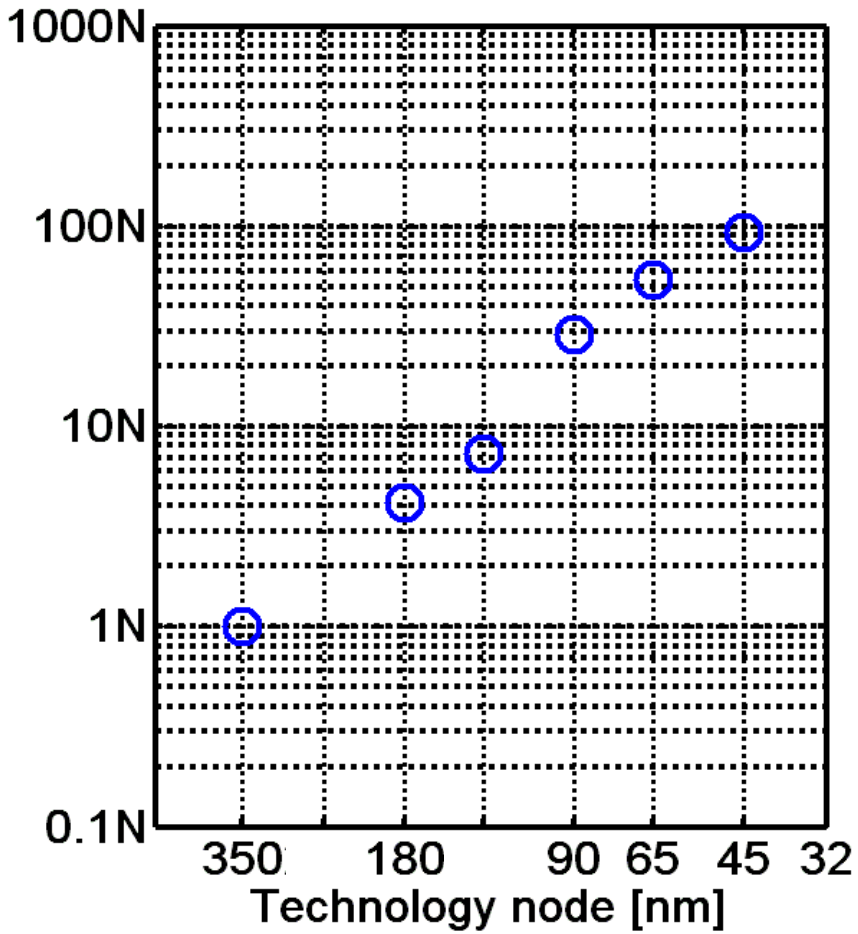


ITRS'09

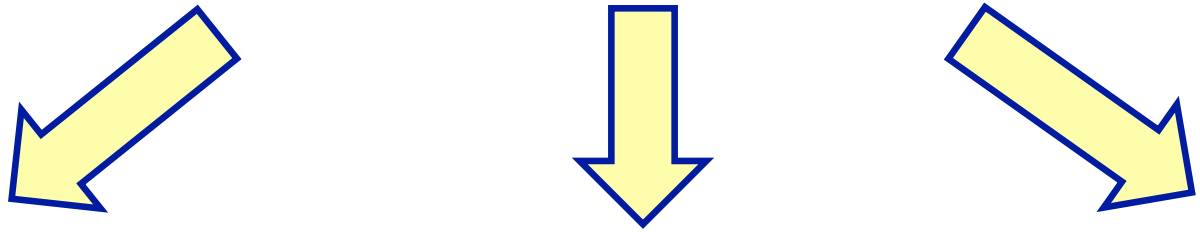
Reduce Area: Motivation



Number of DFFs within an area of 200um x 200um



Design Techniques to Keep Analog & RF Compatible with Nanoscale CMOS

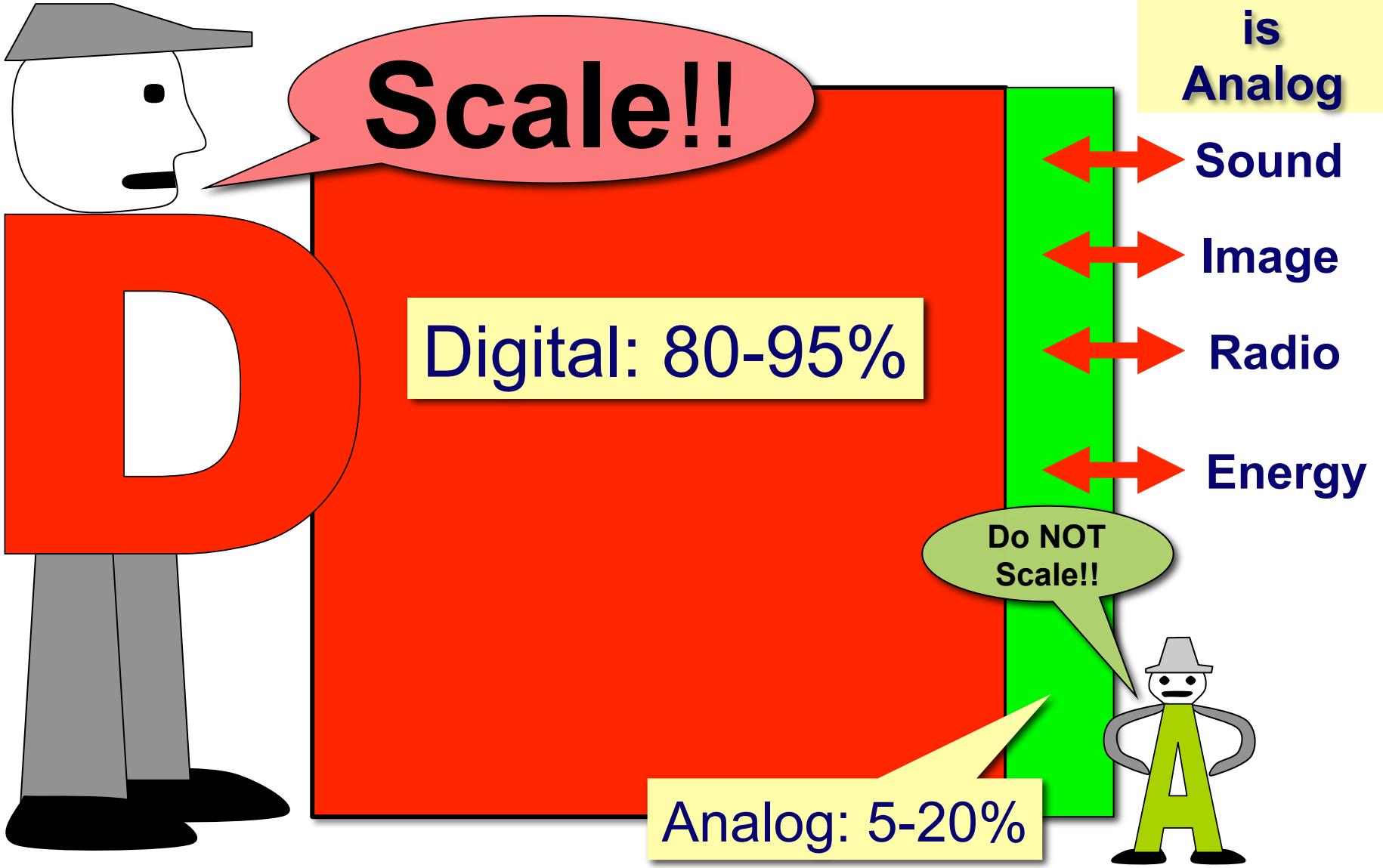


Scale the **Supply Voltage** of Analog/RF Circuits

Reduce the **Area** of RF circuits

Use **Digital Gates** to Improve Analog/RF Performance

System on a Chip

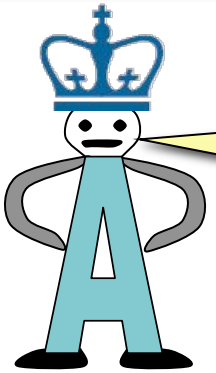


Columbia's 0.5-0.6V Analog & RF Roadmap

Systems

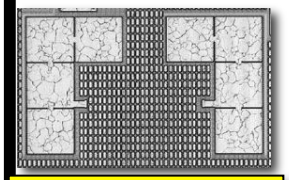
Functions

Blocks



Analog V_{DD} scaling, Sure we can …

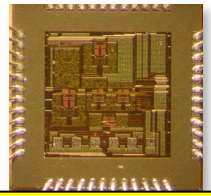
90nm
180nm
250nm



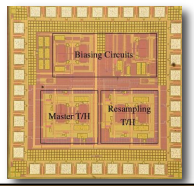
Body-input OTA

Gate-input OTA

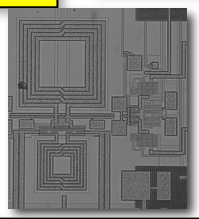
135kHz LPF + Tuning



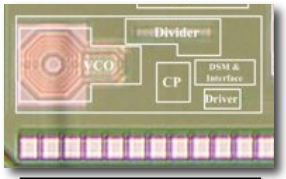
CT 74dB 25kHz ΣΔ A/D



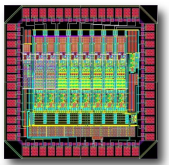
10b 1Ms THA



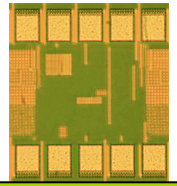
900MHz RF Front-end



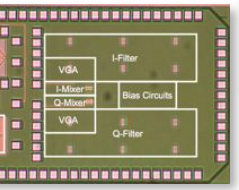
2.4GHz LO Synth.



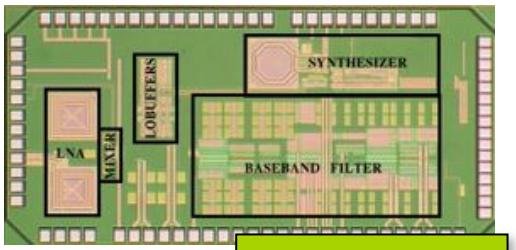
8b 10Ms A/D



0.6V V_{DD} V-Reference



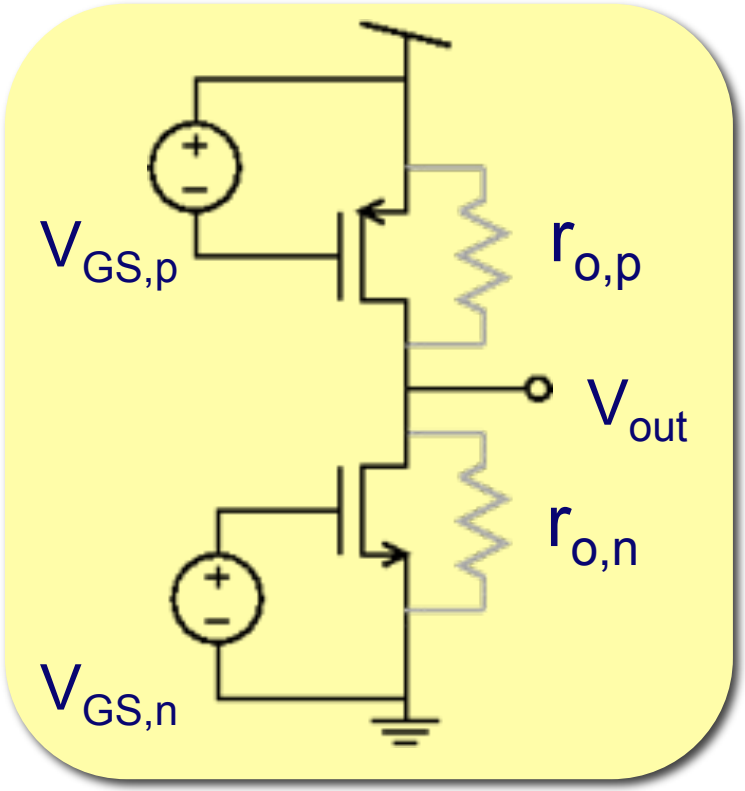
2.4GHz RCV

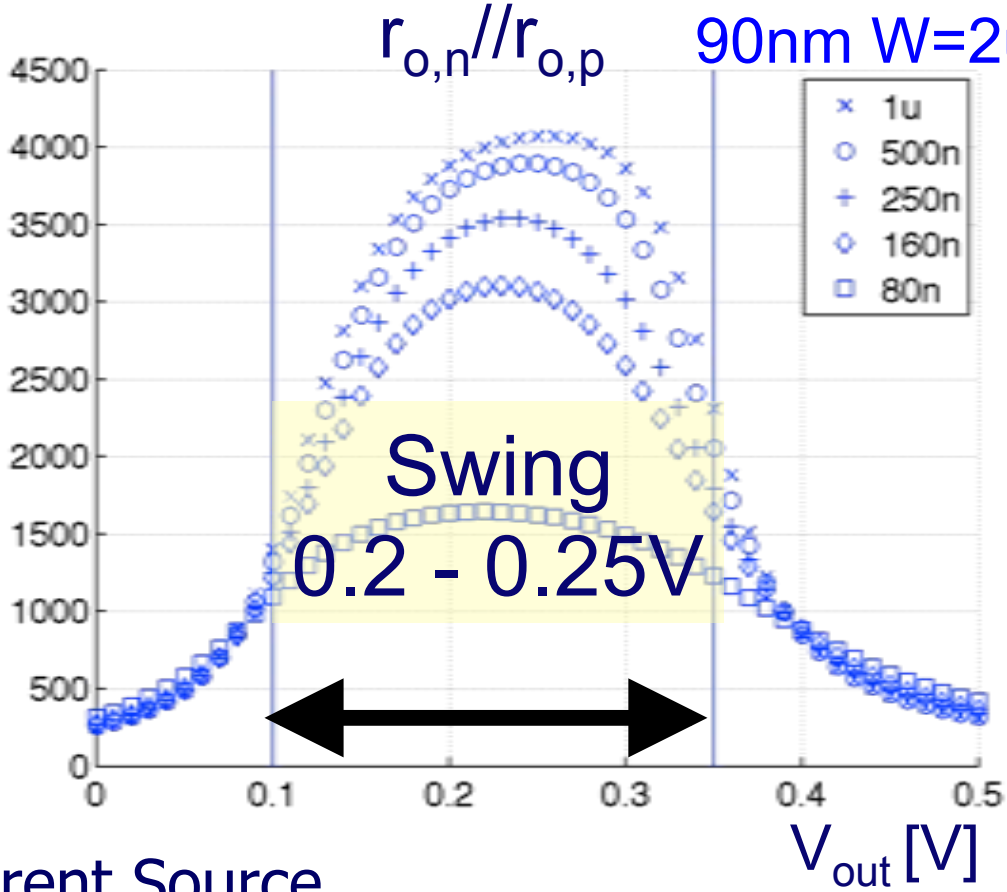


2.4GHz RCV+Synth

2004 2005 2006 2007 2008 2009

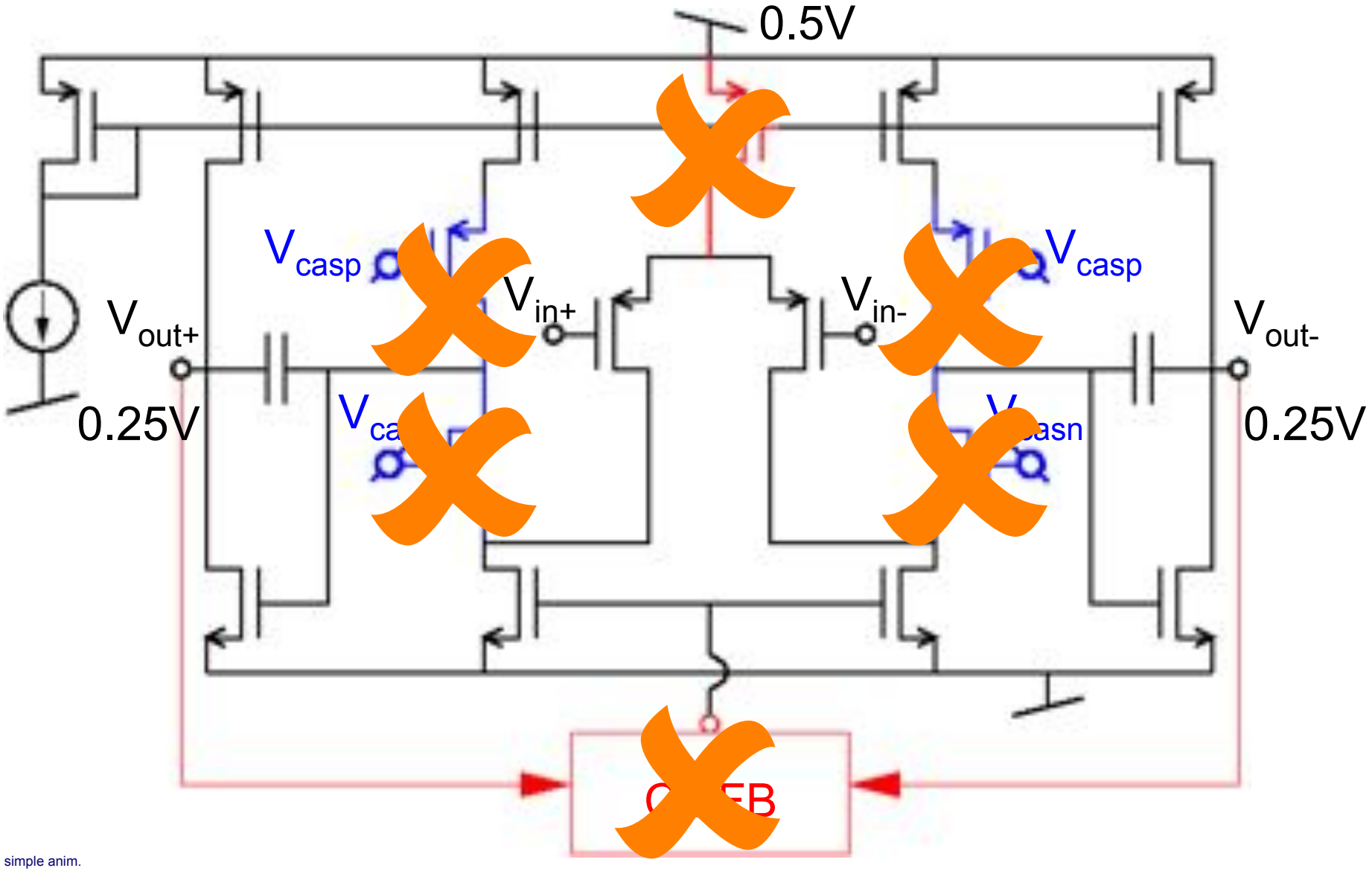
MOST Biasing: CS or VCCS





- Transconductor or Current Source
  V_{DS} > 0.1V to 0.15 V (for V_{GS}-V_{TH} ≤ 0.2 V)
- **Moderate to Strong Inversion**
  (V_{GS}-V_{TH}) ≈ 0.15 V & $|V_{TH}|$ = 0.35V → V_{GS} = 0.5V
  $|V_{TH}|$ = 0.15V → V_{GS} = 0.3V

Ultra-LV Challenges in OTAs



simple anim.

Ultra-low Voltage Analog & RF Design

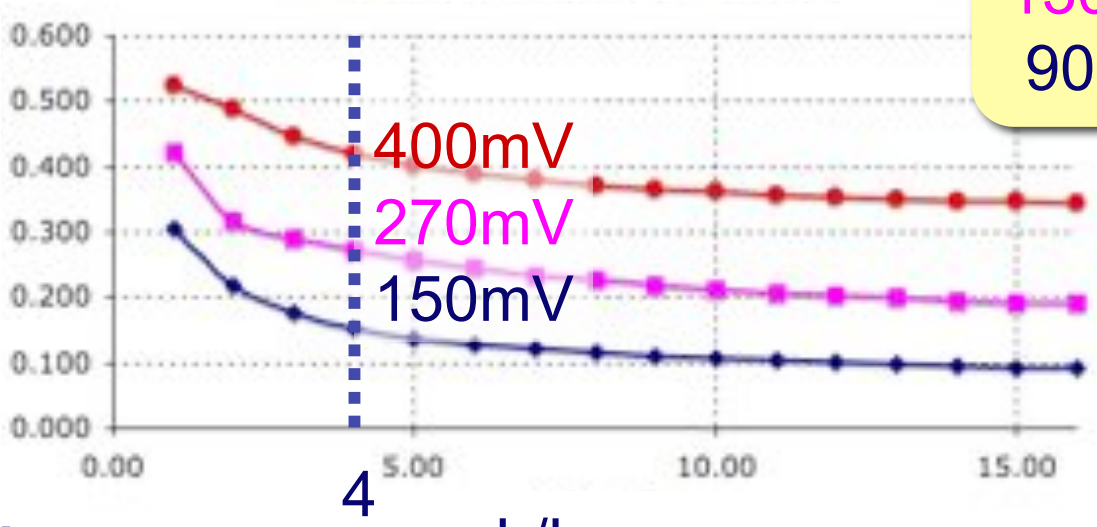
- Exploit full device characteristics
  - RSCE, Body-bias
- Rethink your circuit topologies
  - Eliminate stacks, LCMFB, CMFF, Neg. G
  - Address leakage (cascaded switches),
  - MOS or Schottky based references
- Revise your architectures
  - Eliminate switches in signal path (e.g., RTO),
  - RF front end: Current mode operation/interfaces
  - RF Baseband: Optimize structure
- True low voltage design: no voltage boosting, no special devices

Device Level Solutions

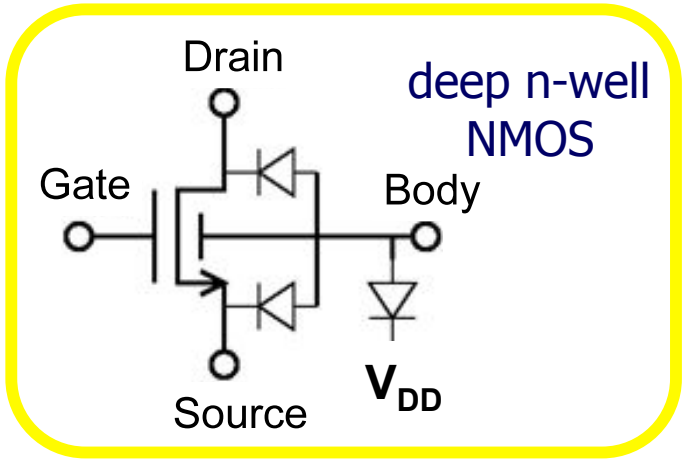
180nm
130nm
90nm

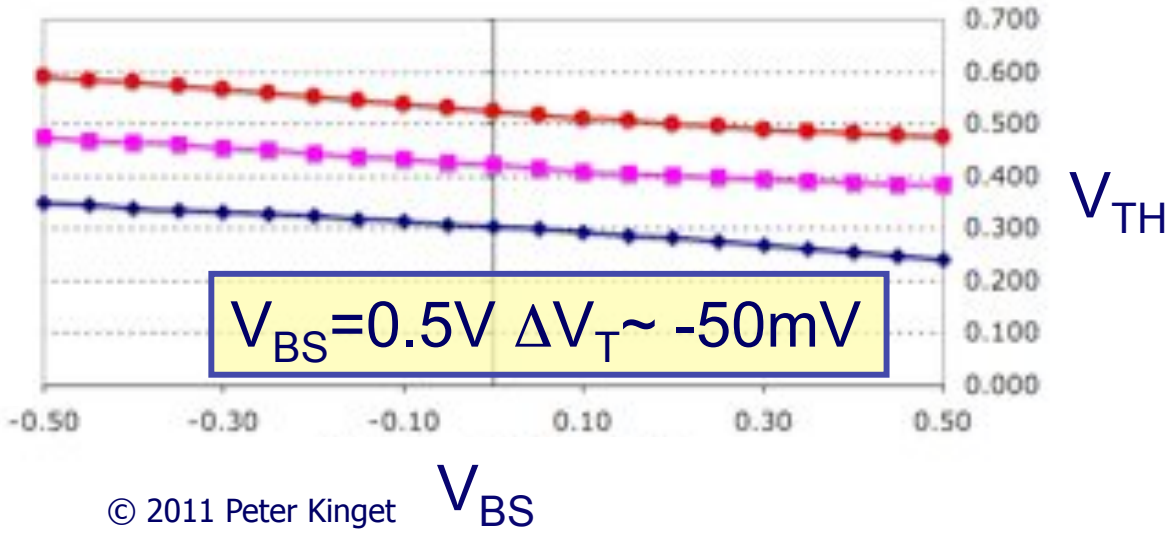
- RSCE

V_T ↓ as L ↑

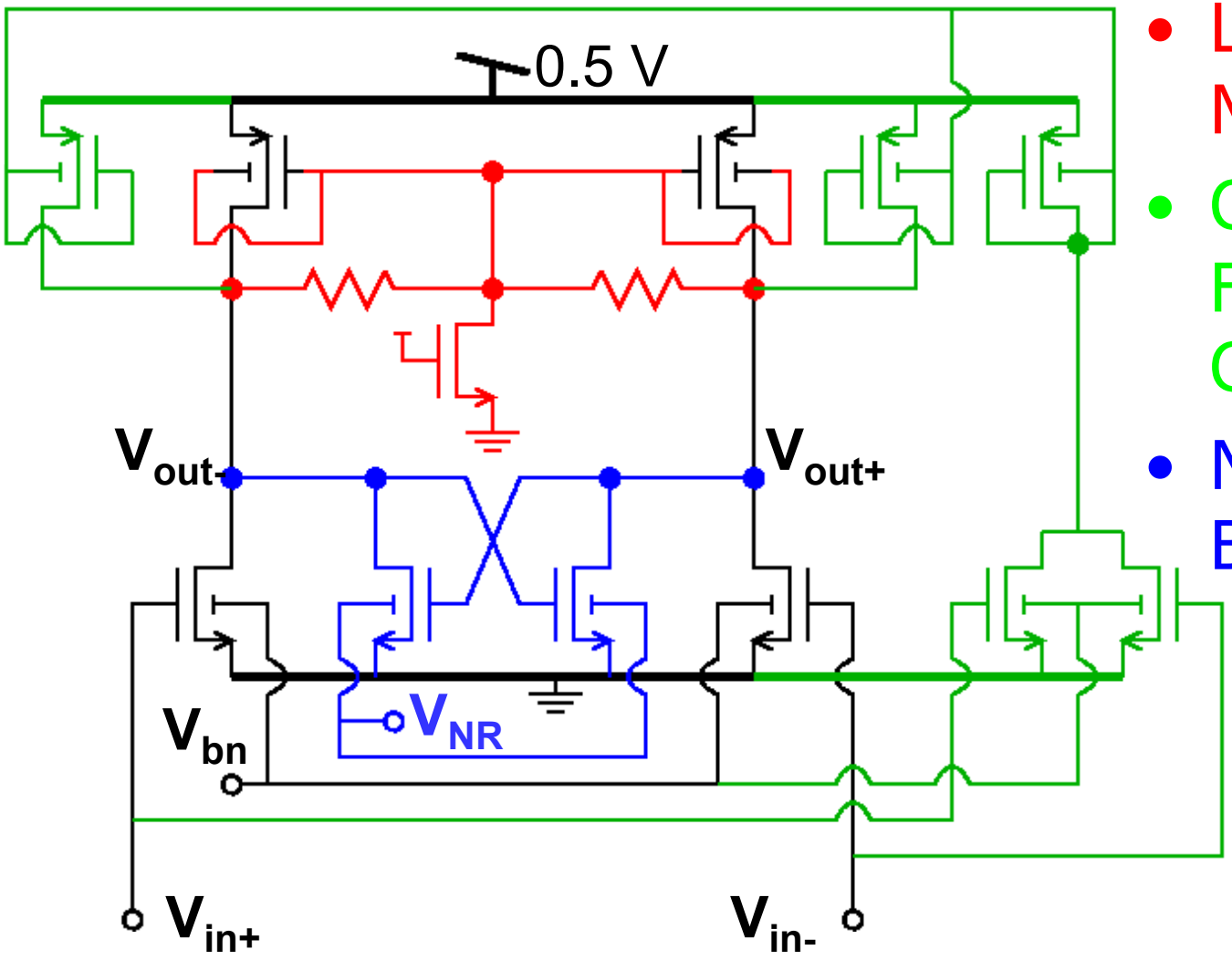


- Forward Body-Bias



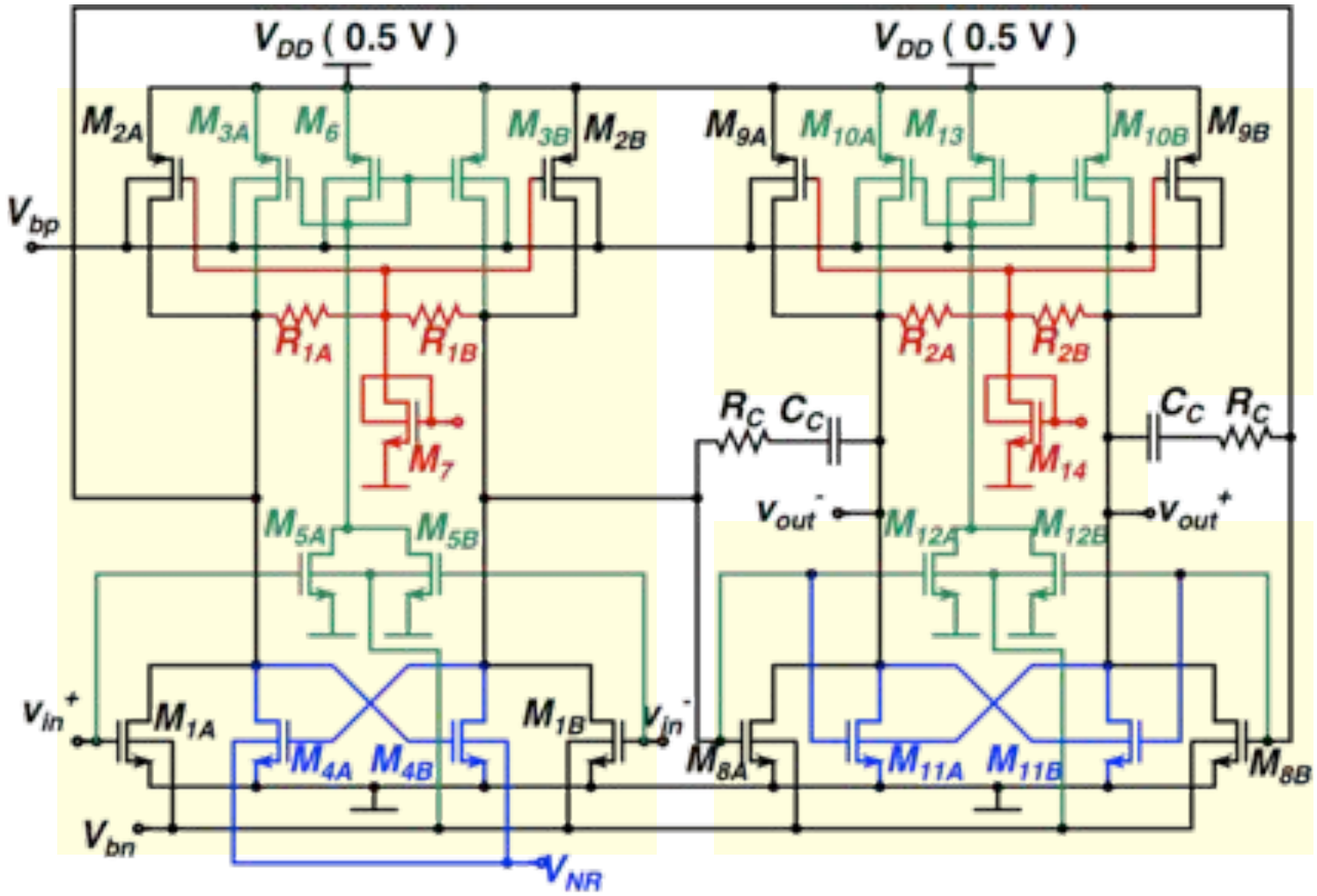


0.5V Gate-Input OTA Stage



- Local Common-Mode Feedback
- Common-Mode Feed Forward Cancellation
- Neg. G Gain Boost

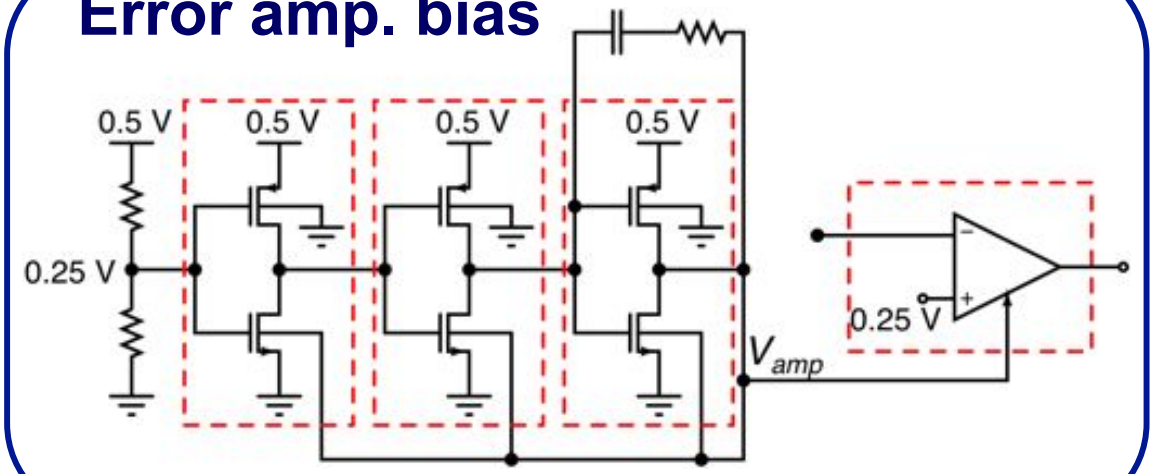
0.5V Two-Stage OTA



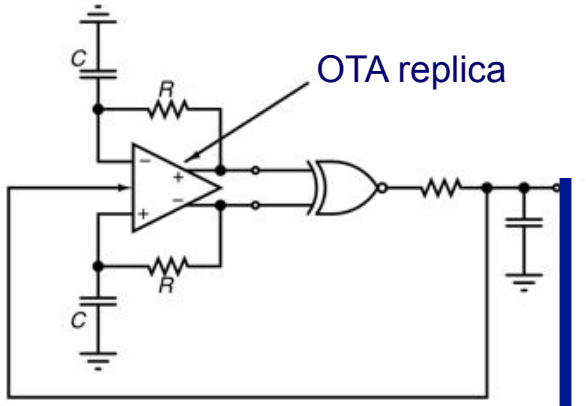
- $V_{T,nom}$=0.5V; CM_{in} 0.4V, 0.18um CMOS
- 62dB DC gain; 10MHz GBW; 10pF $C_{L,diff}$; 75uW

On-Chip Biasing Circuits

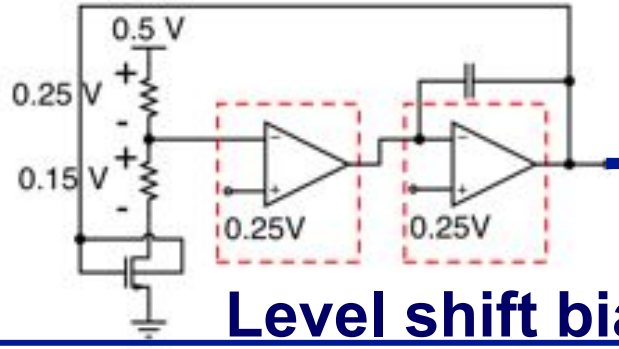
Error amp. bias



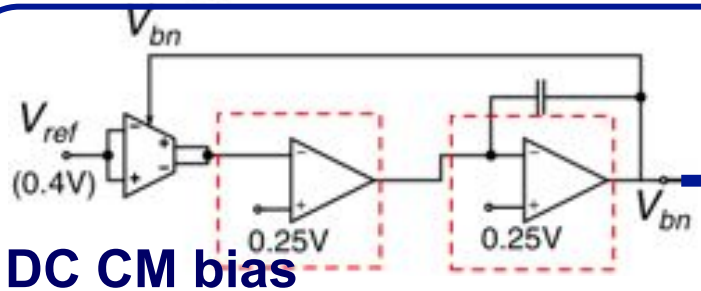
Gain bias



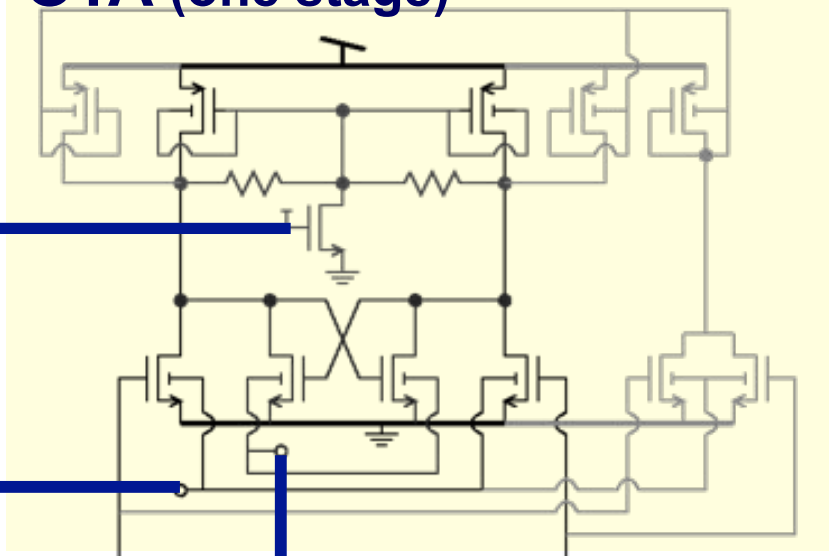
Level shift bias



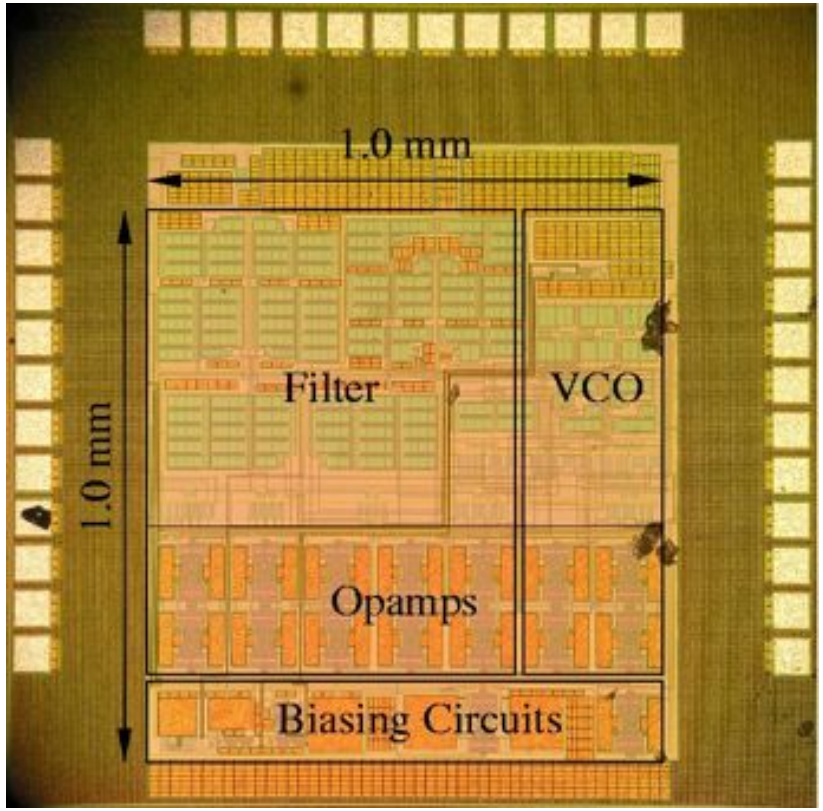
DC CM bias

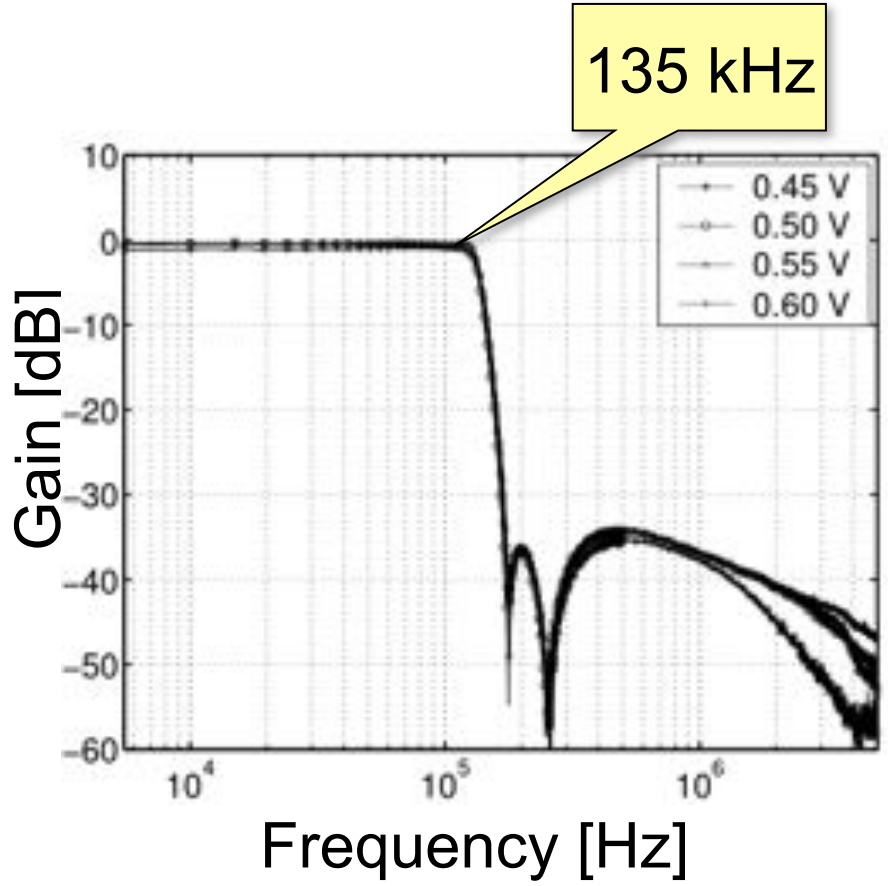


OTA (one stage)



0.5V Fully Integrated 5th Order LPF

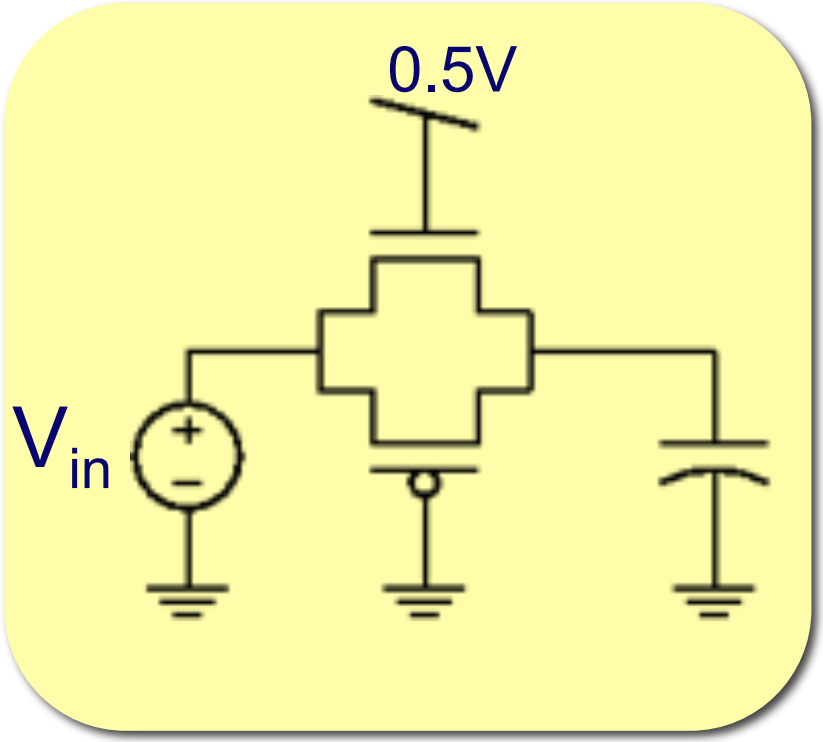




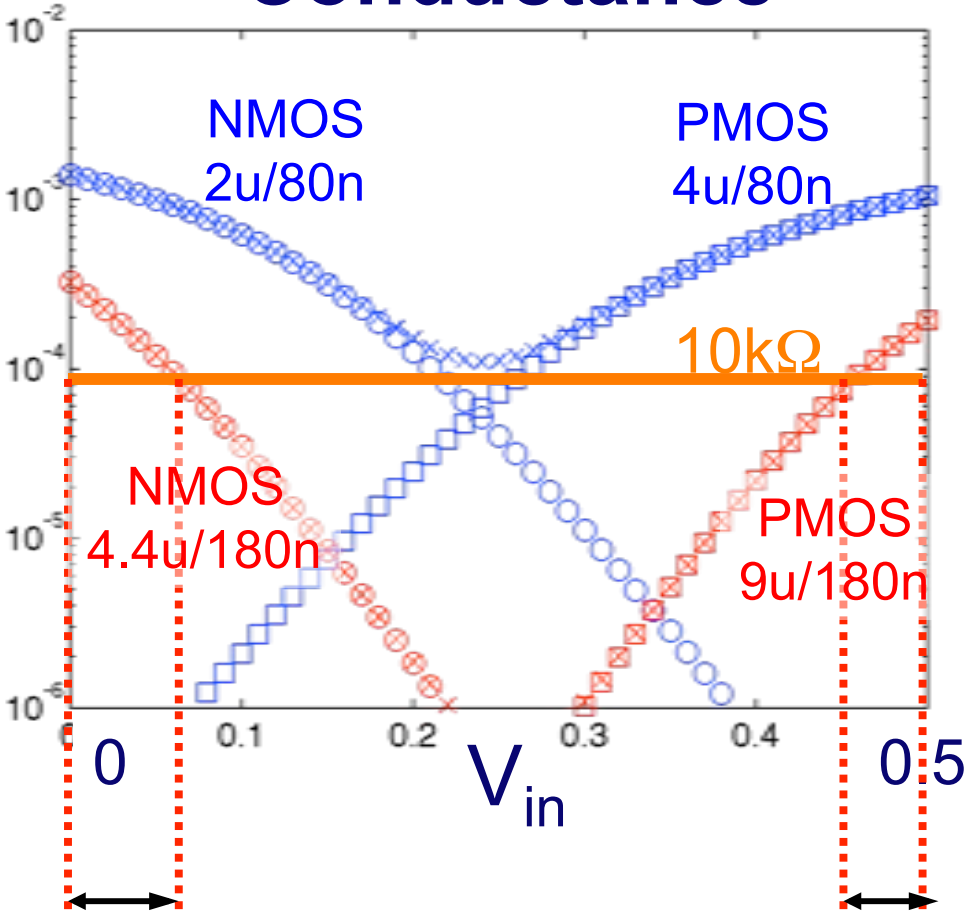
- Operation at 0.45 V to 0.6 V
- 1.1 mW power dissipation
- 57 dB dynamic range

[Chatterjee, Tsividis, Kinget, ISSCC05, JSSC05]

Floating Switch Challenge



Conductance

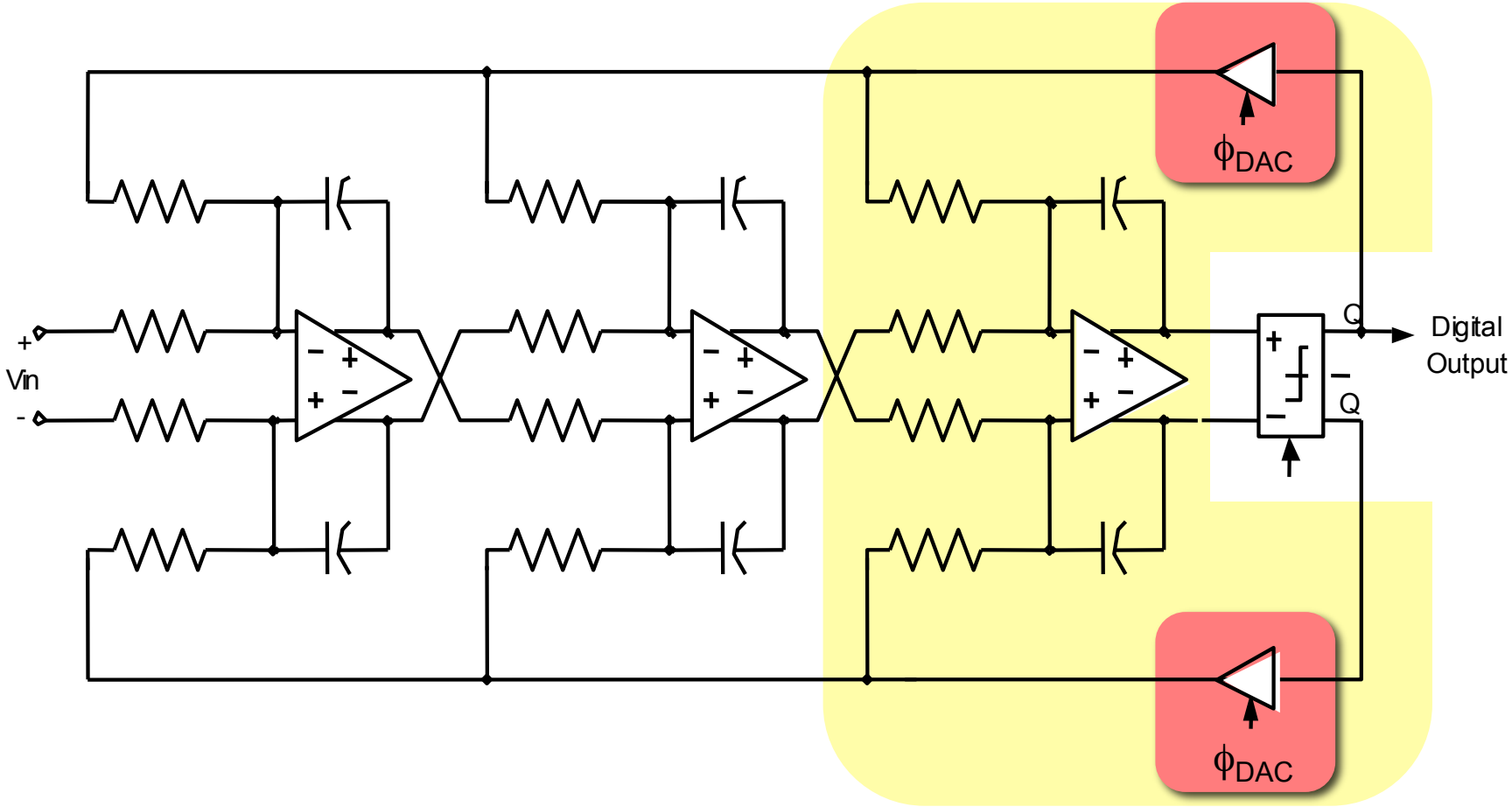


90nm: V_{TH} = 0.3V

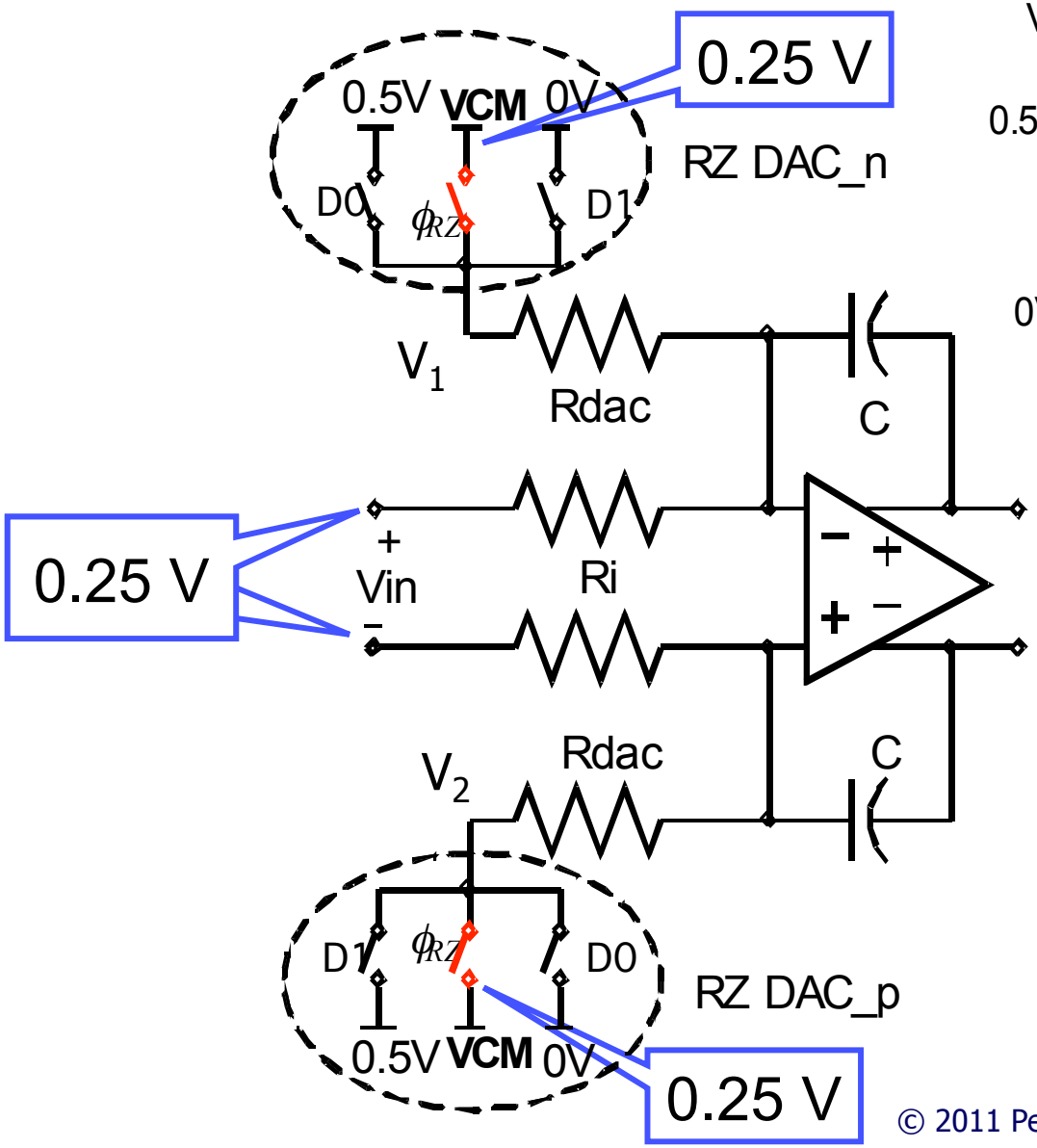
180nm: V_{TH} = 0.55V

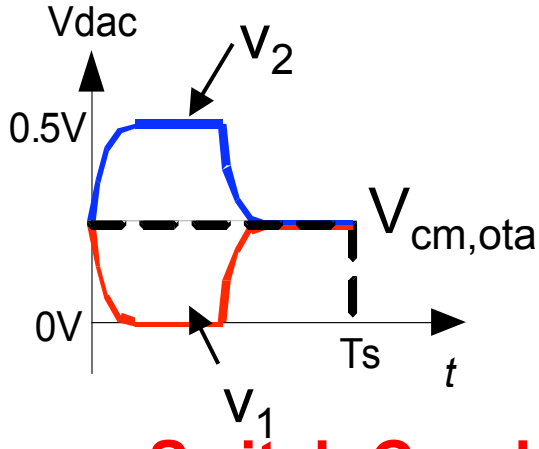
3rd order CT ΣΔ Modulator

Using Active RC integrators

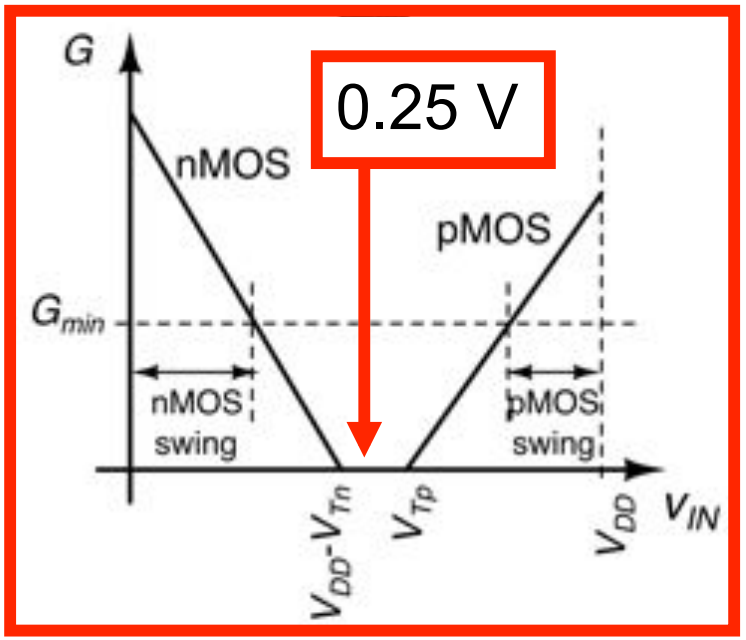


RZ Challenge: Switches at $V_{DD}/2$

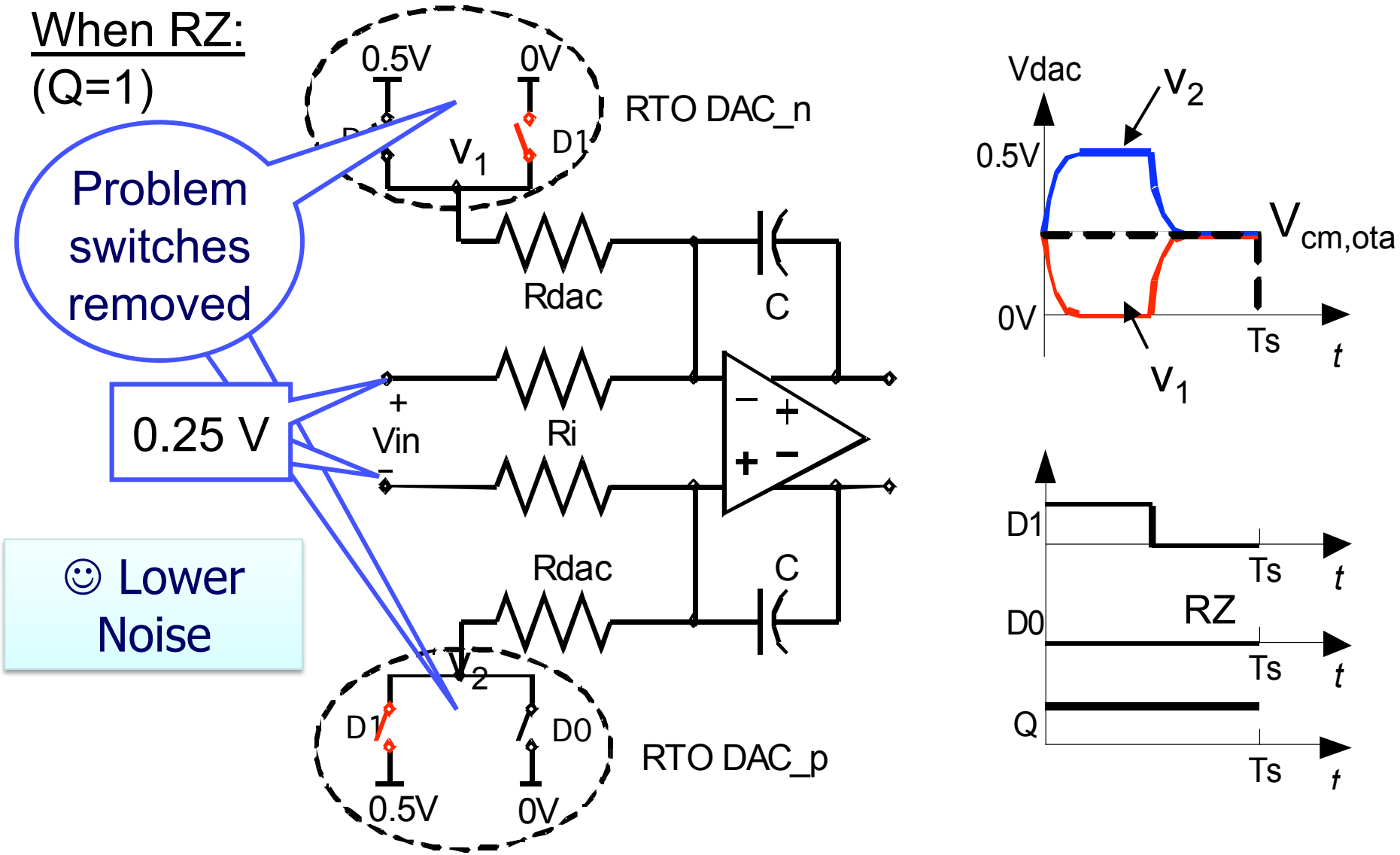




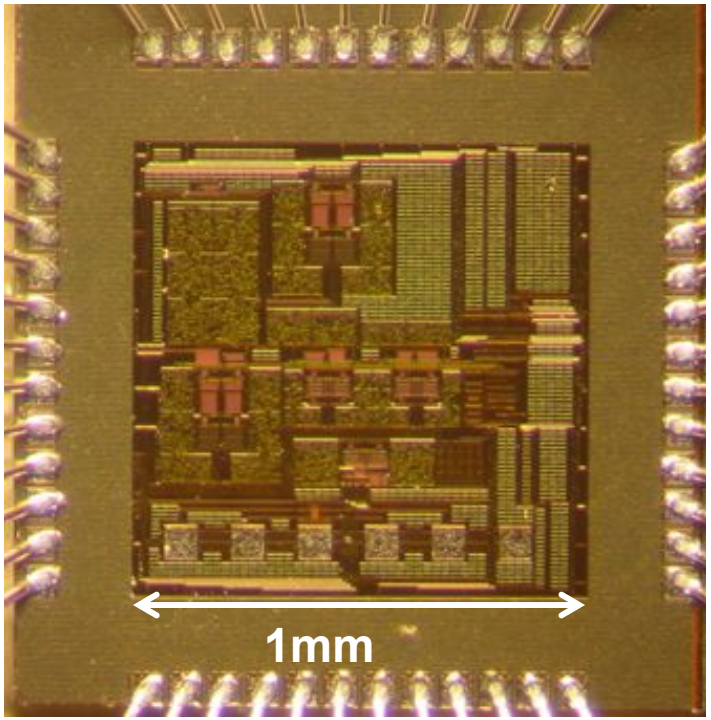
Switch Conductance

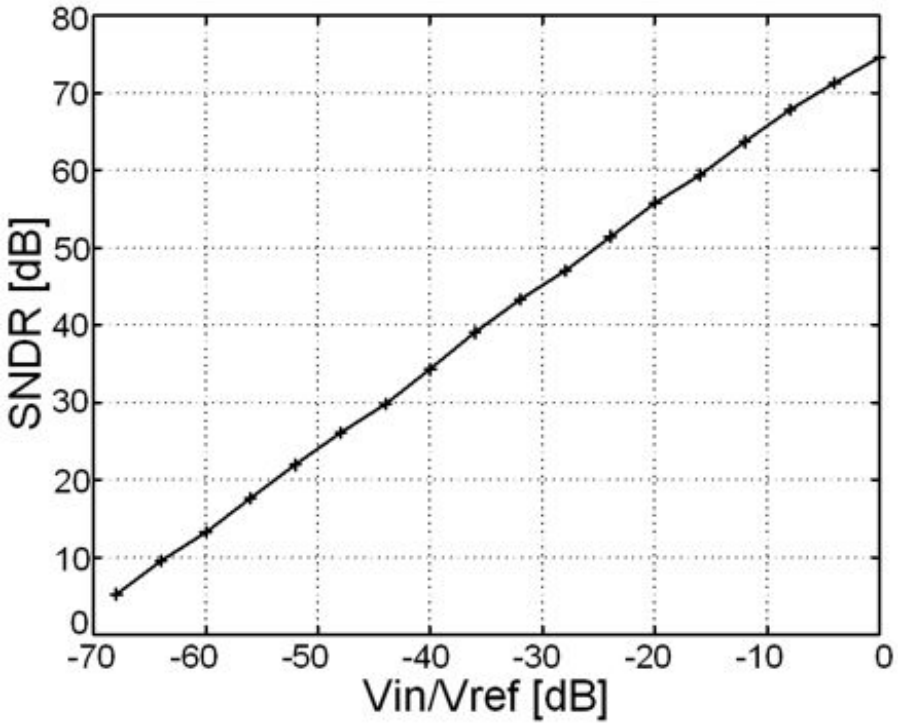


Solution: Return-to-Open



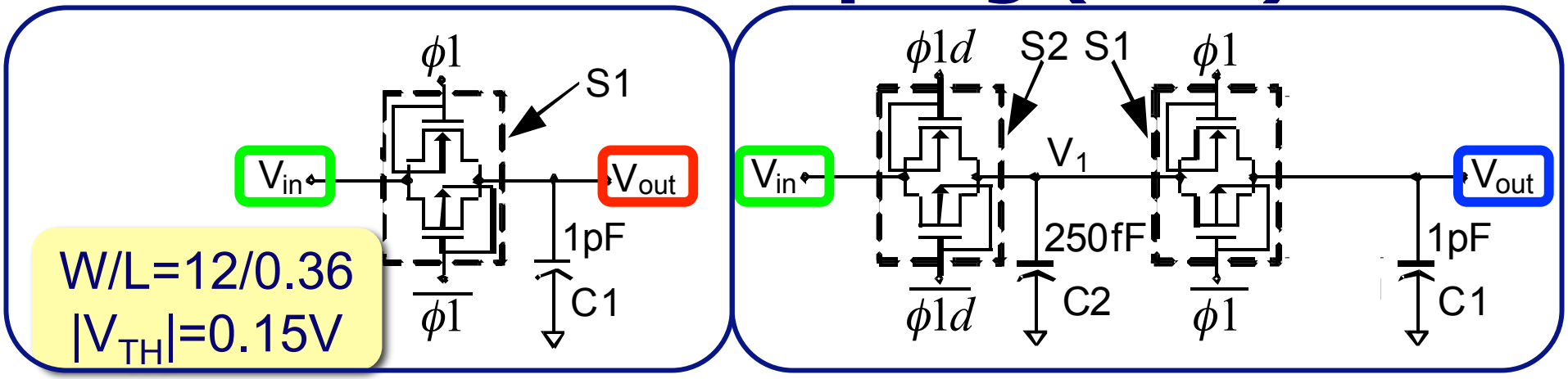
0.5V 74 dB SNDR 25kHz ΣΔ Modulator

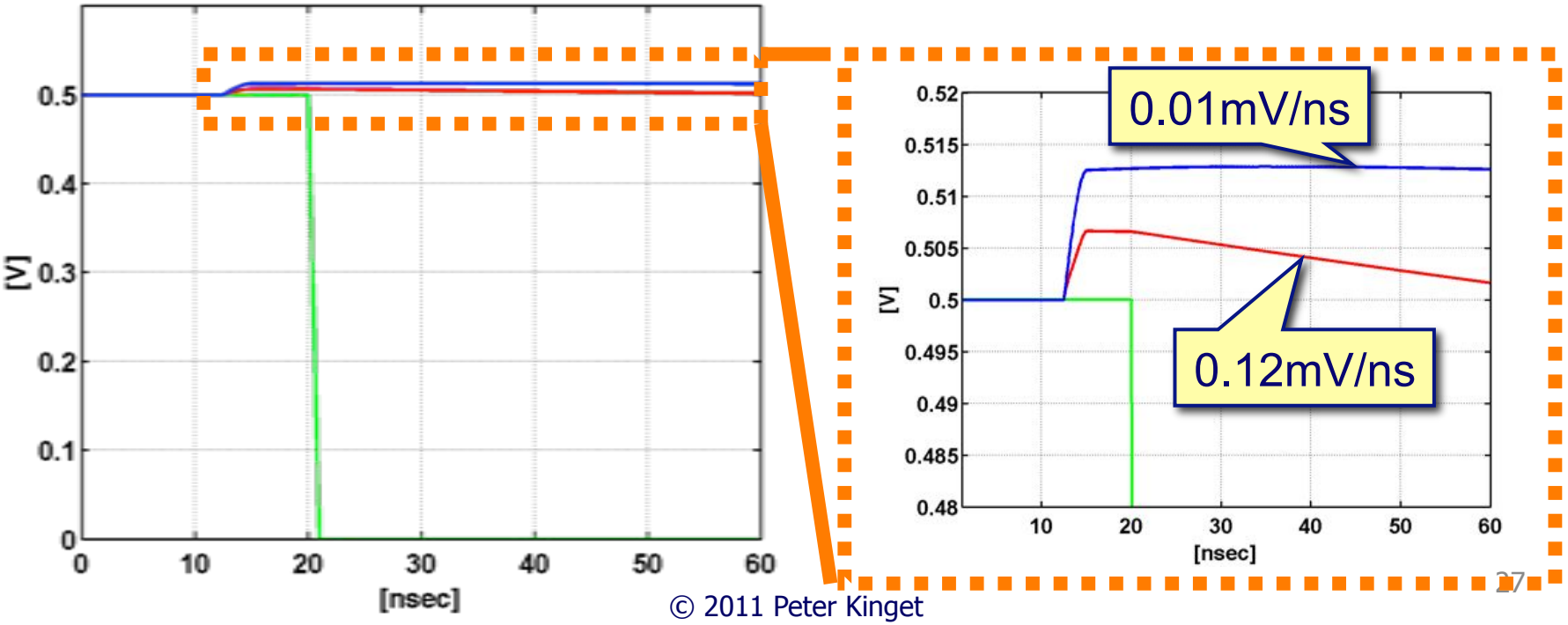




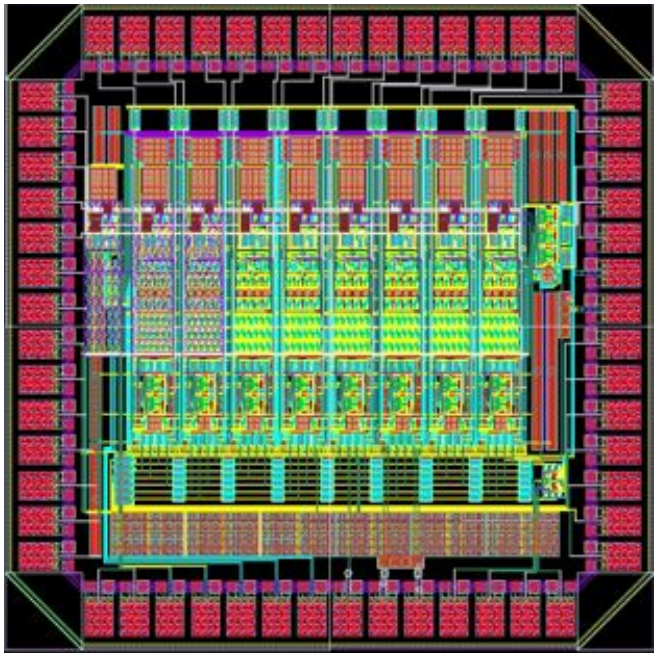
- Operation for V_{DD} = 0.45V to 0.8V
- Return-to-open architecture, body-input gate-clocked circuits
- 74dB SNDR, 25kHz, 64x OSR, 300µW, 0.18um CMOS
- [Pun, Chatterjee, Kinget, ISSCC 06, JSSC 07]

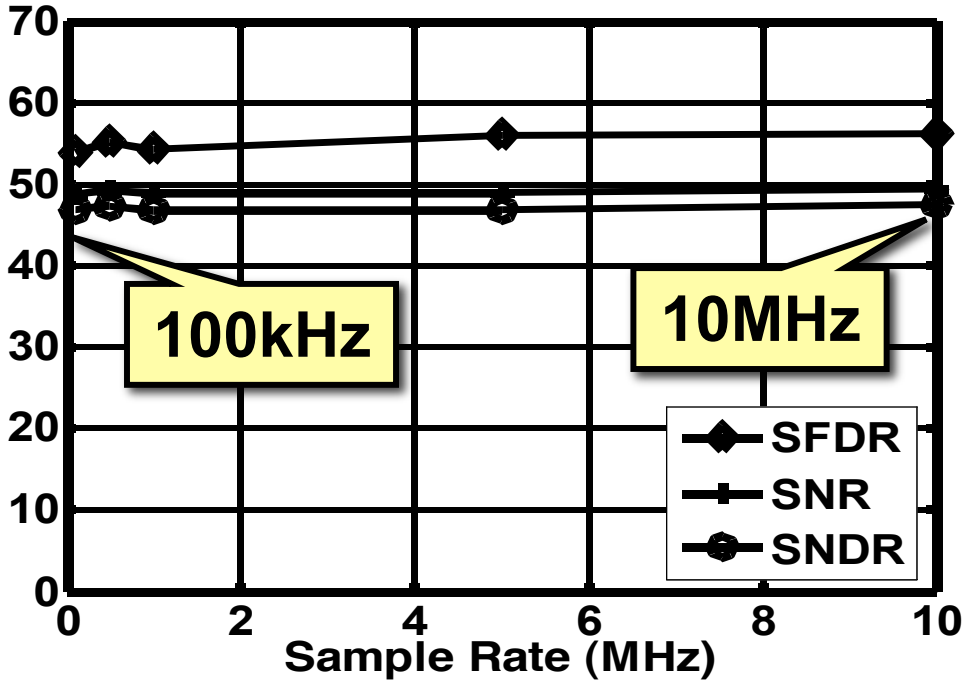
'Low V_{TH}' switch leakage: Cascaded Sampling (Sim.)





0.5V 8bit 10Msps Pipelined ADC

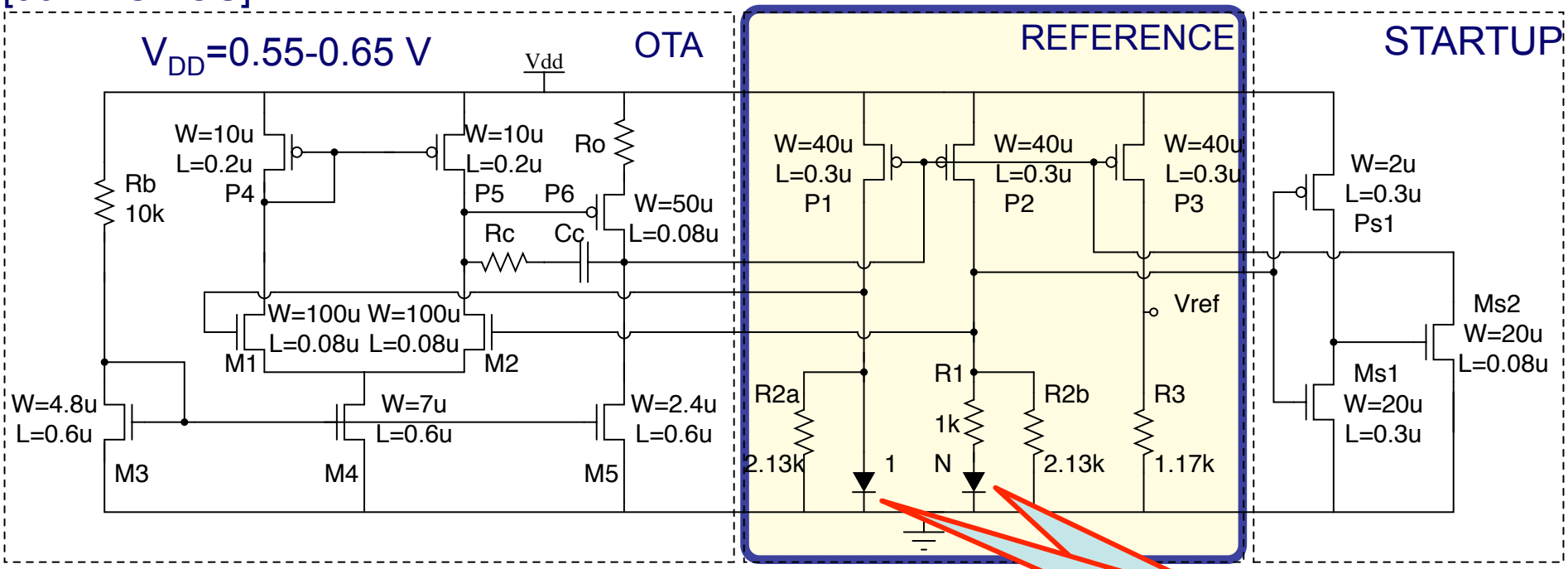


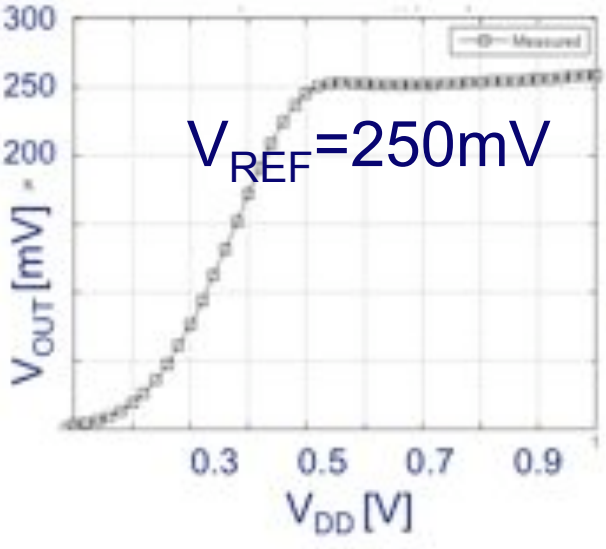


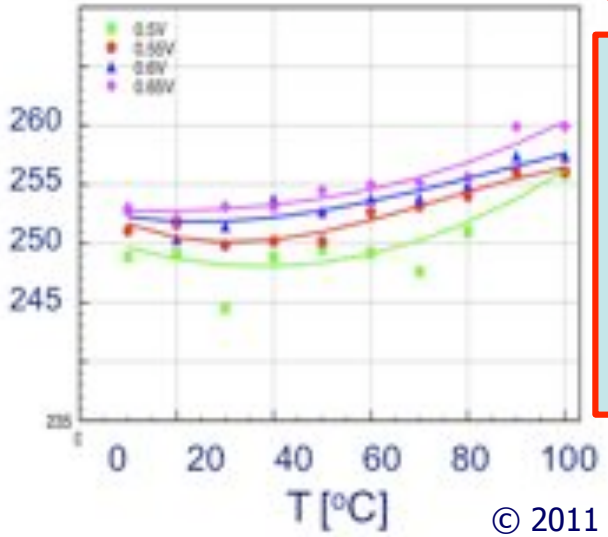
- No internal voltage or clock boosting; regular devices; cascaded sampling technique.
- Aux. S/H for the sub-ADC to eliminate front-end SHA.
- 10Msps: SNDR 48dB@101kHz, 43.3dB@4.9MHz.
- 2.4mW in 90nm CMOS [Shen, Kinget, VLSI07, JSSC08].

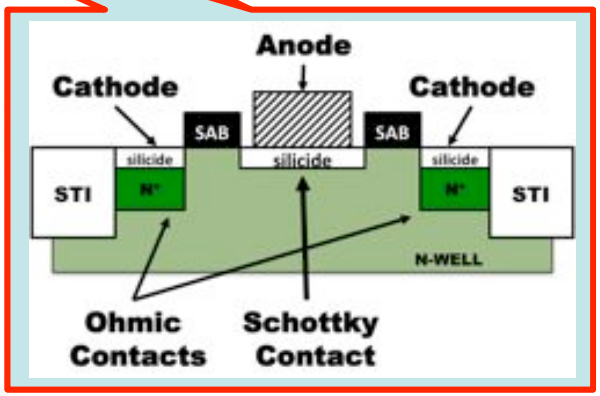
ULV Schottky Reference

[90nm CMOS]

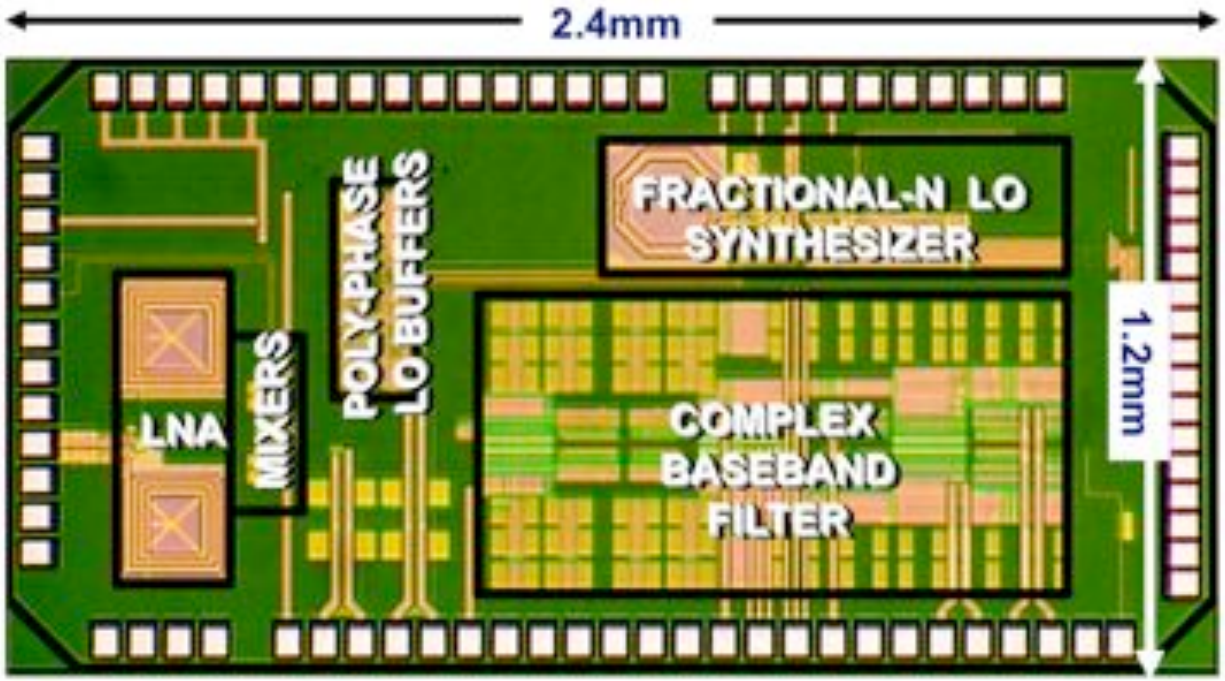






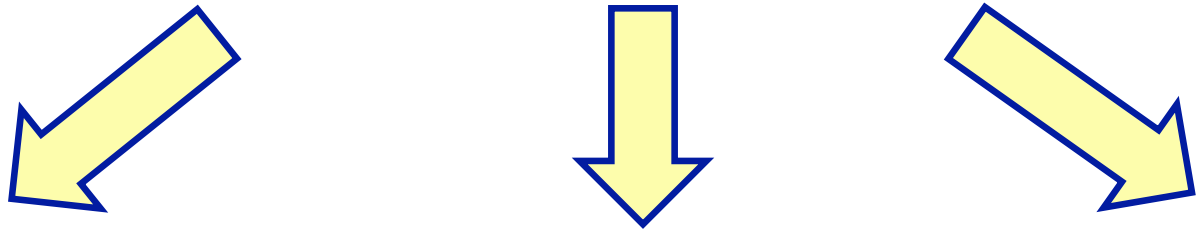


0.6V 2.4GHz ZIF/LIF RCV + Synth.



- 2.9 mm^2 - 90nm RVT CMOS - 64-pin QFN package
- 2.4-2.5 GHz operation @ 0.6V & 32mW
  - 16dB NF, -10.5dBm IIP_3, 67dB Gain
  - PN -127dBc/Hz @ 3MHz offset
- Fully functional 0.55V to 0.65V V_{DD}

Design Techniques to Keep Analog & RF Compatible with Nanoscale CMOS



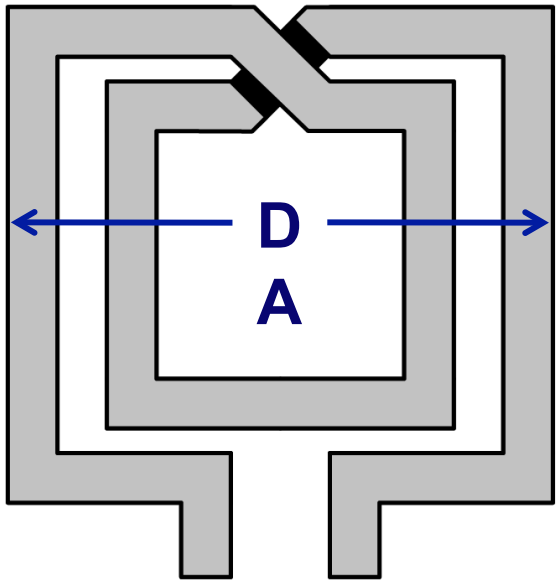
Scale the **Supply Voltage** of Analog/RF Circuits

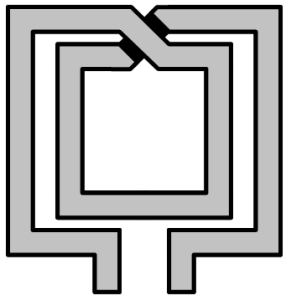
Reduce the **Area** of RF circuits

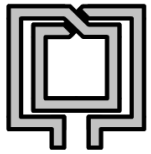
Use **Digital Gates** to Improve Analog/RF Performance

Use f_T for VCO Area Scaling

- Scaled CMOS ➔ higher f_T
  ➔ operate @ N x higher frequency
  ➔ divide by N

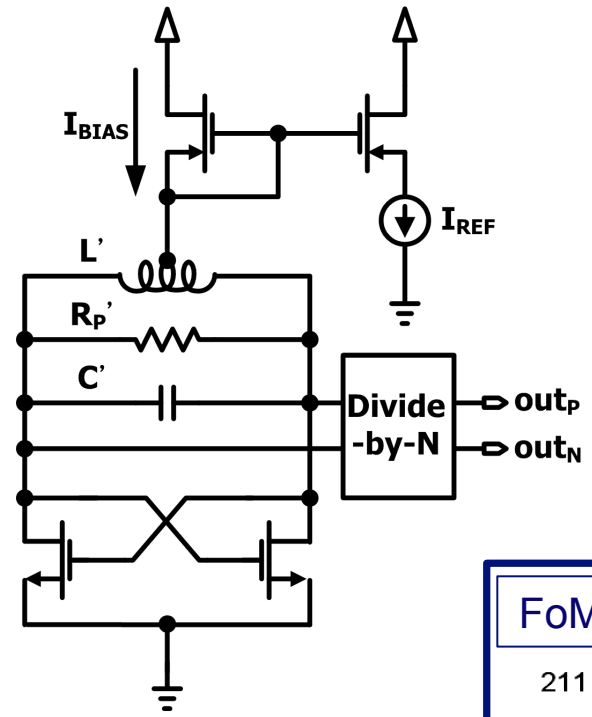


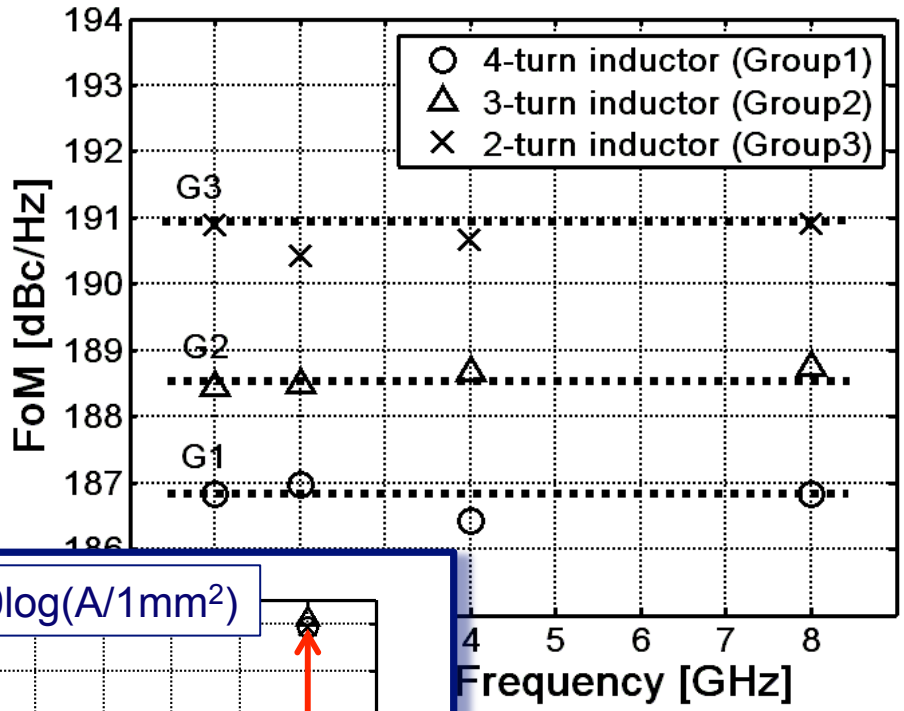


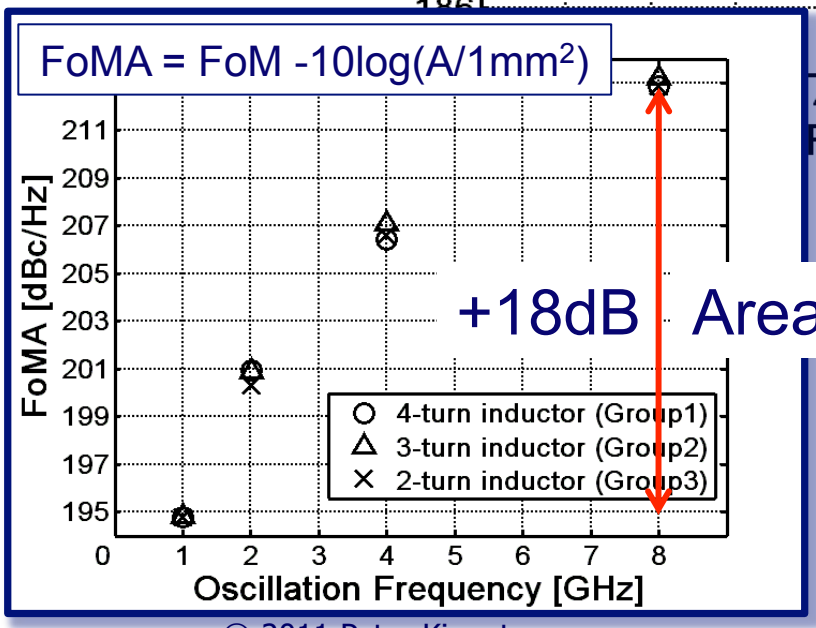


D/2 A/4	D/4 A/16	D/8 A/64
L, Rs, Q@f_0	L/2, Rs, Q@$2f_0$	L/4, Rs, Q@$4f_0$	L/8, Rs, Q@$8f_0$

VCO Area Scaling





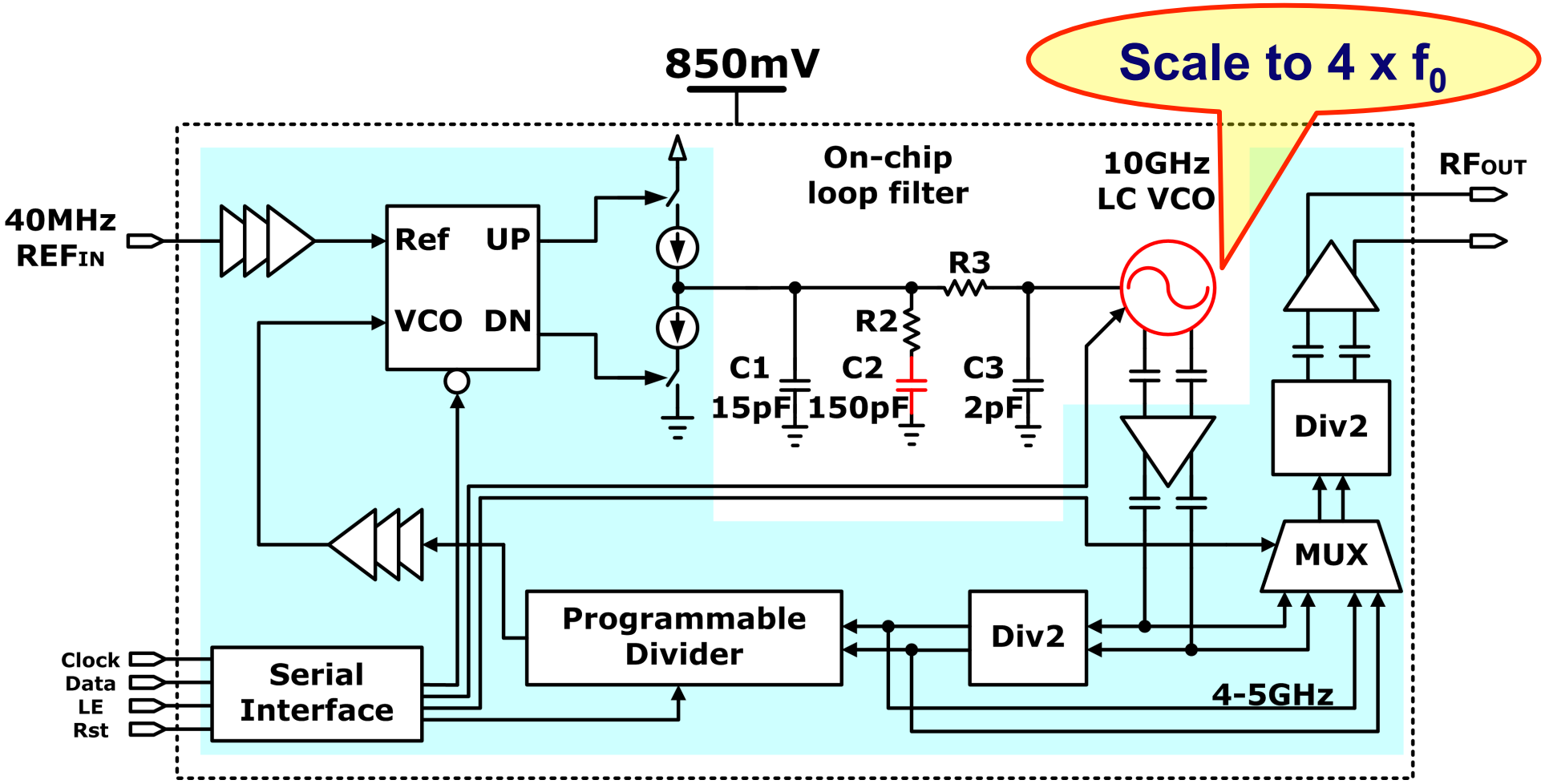


+18dB Area/64

[Yu, Kinget, TCASII 09]

[Sim. in 45nm]

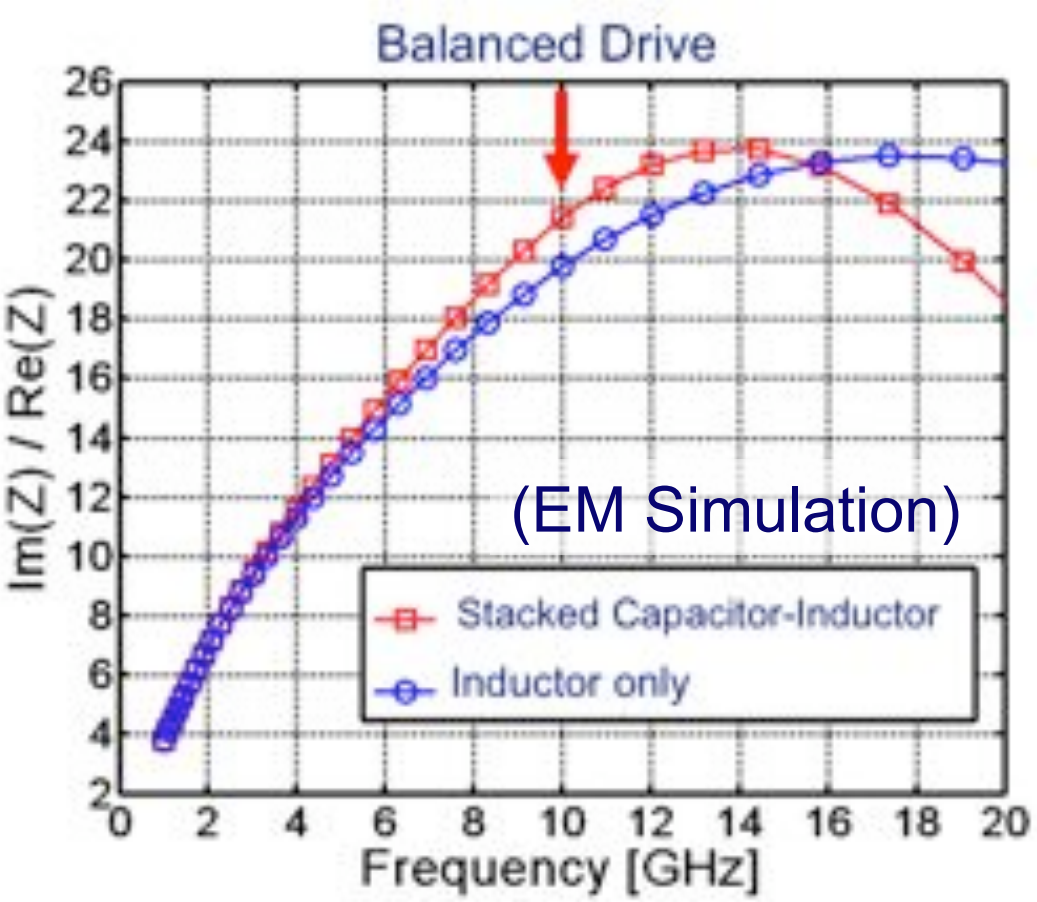
PLL and Area Scaling

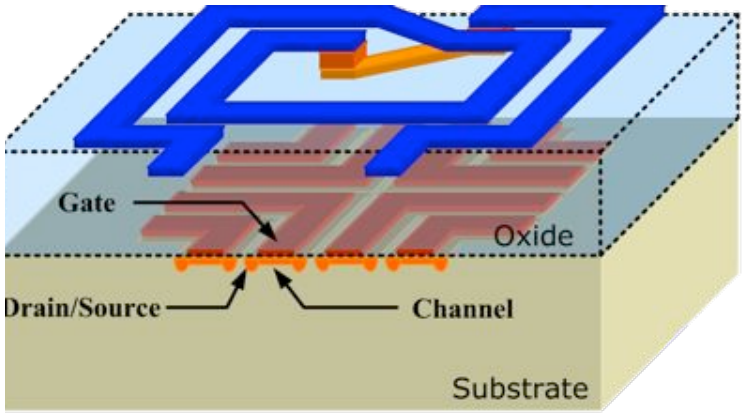


Circuits that scale easily with feature size

- 150pF needs ~13000um^2 of inversion-mode MOS capacitor

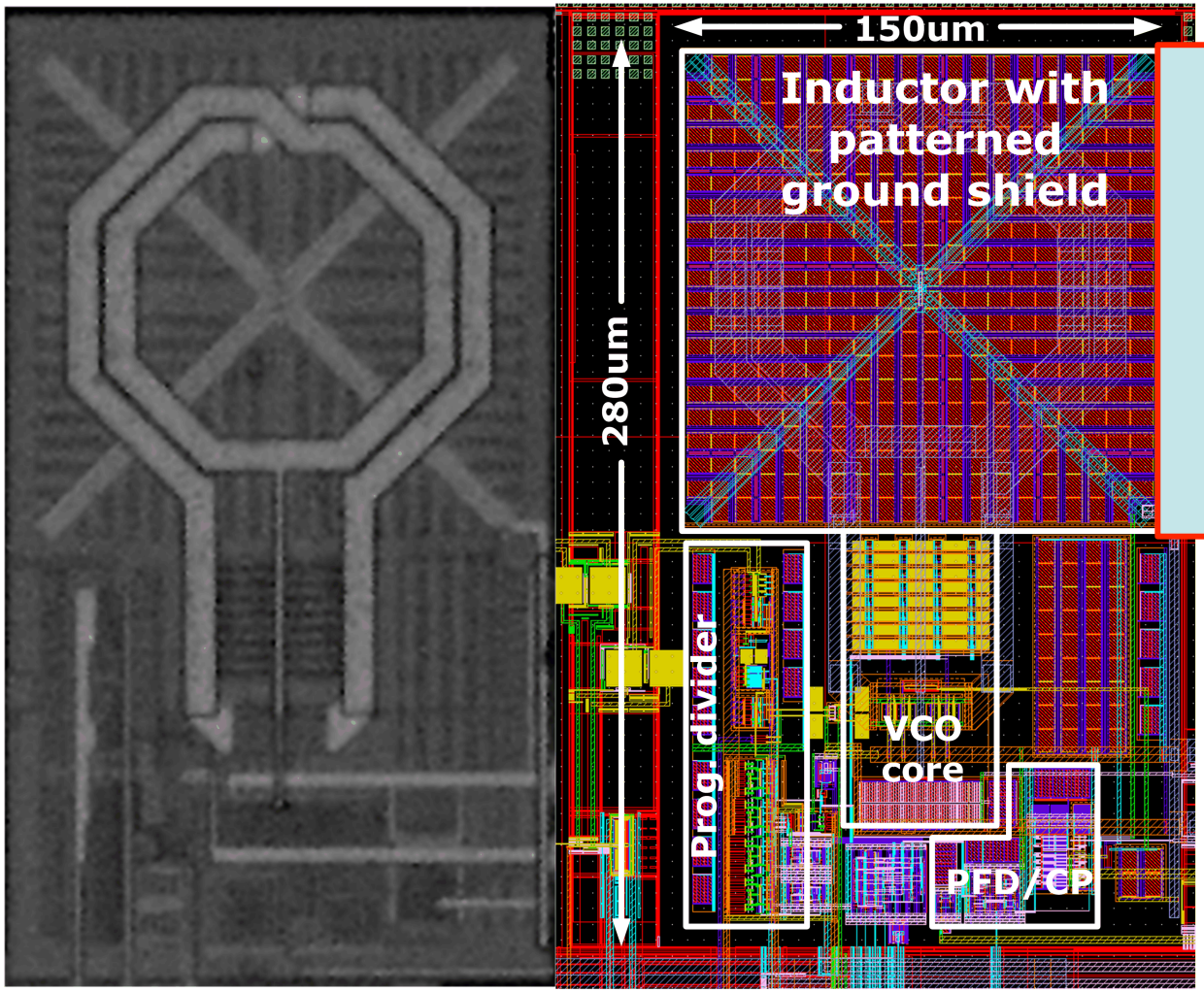
Stacked MOS Cap-Inductor





➔ no Q degradation, even improvement (shielding)

0.042mm2 Fully Int. PLL



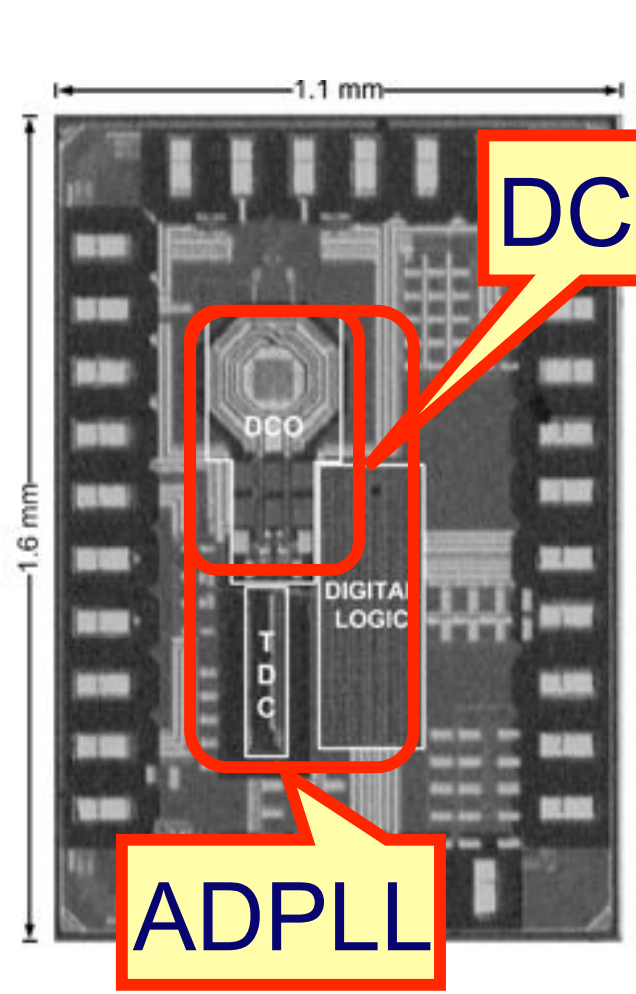
Loop Filter Capacitor C2

Area Saving 30%

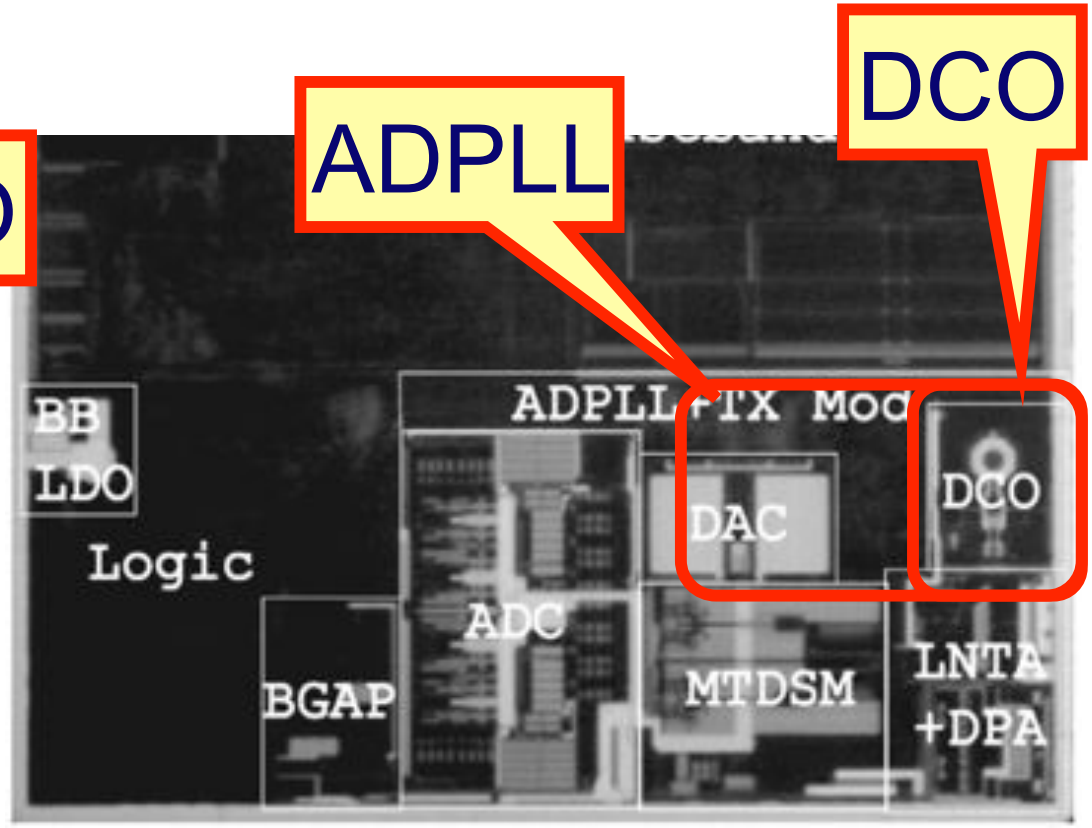
[Yu, Kinget, Esscirc 08]

Fully Integrated PLL, on-chip loop filter under VCO inductor
45nm LP CMOS; V_{DD}=0.85V; 10GHz VCO; 2.5GHz o/p

All-Digital PLLs

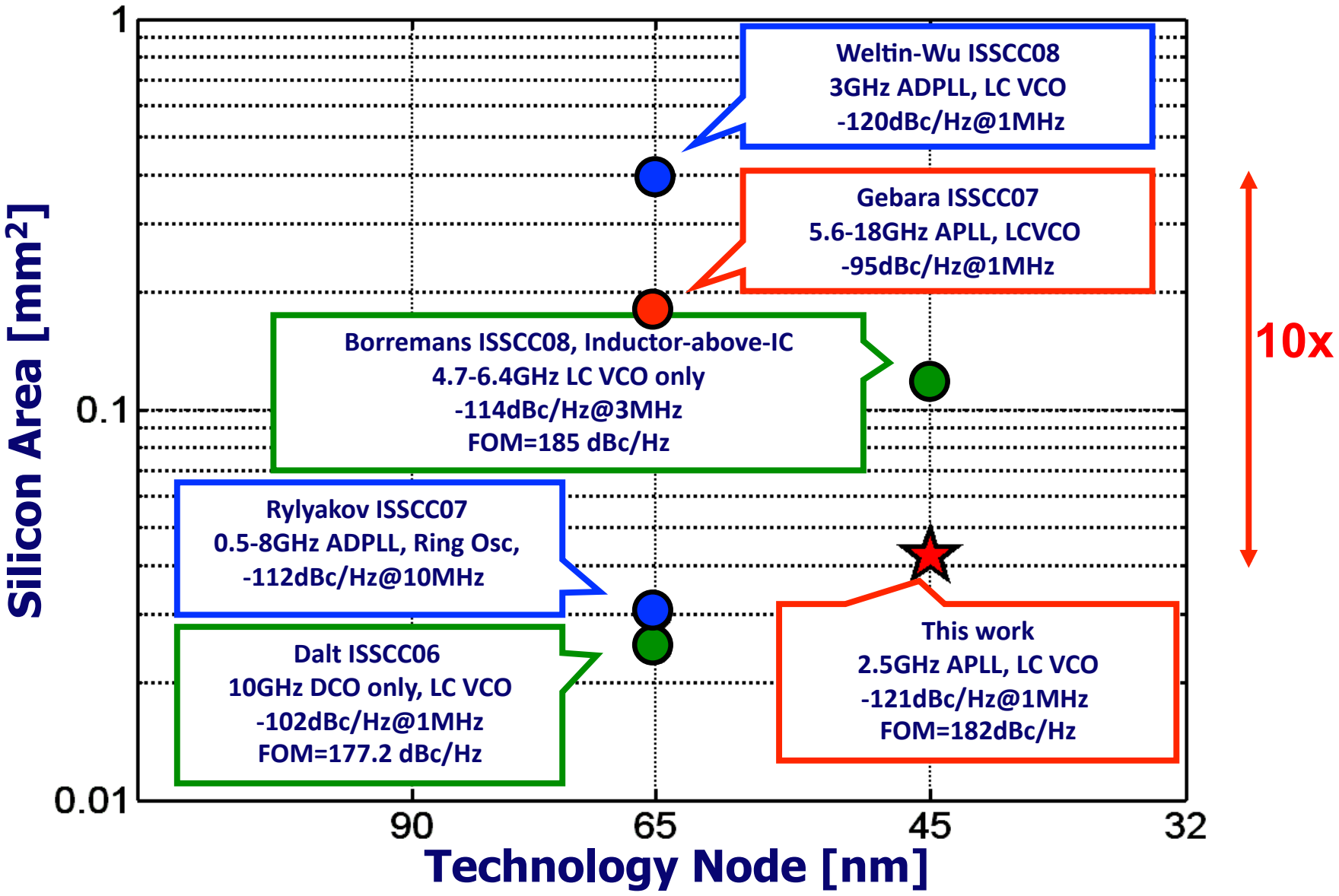


[Weltin-Wu, 2008]

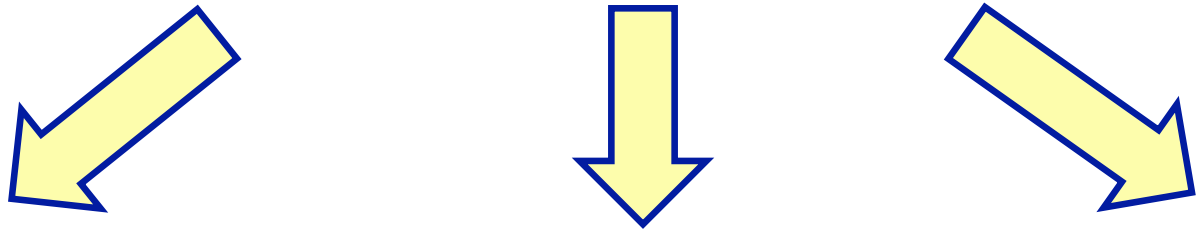


[Staszewski, 2004]

Area & Performance Comparison



Design Techniques to Keep Analog & RF Compatible with Nanoscale CMOS

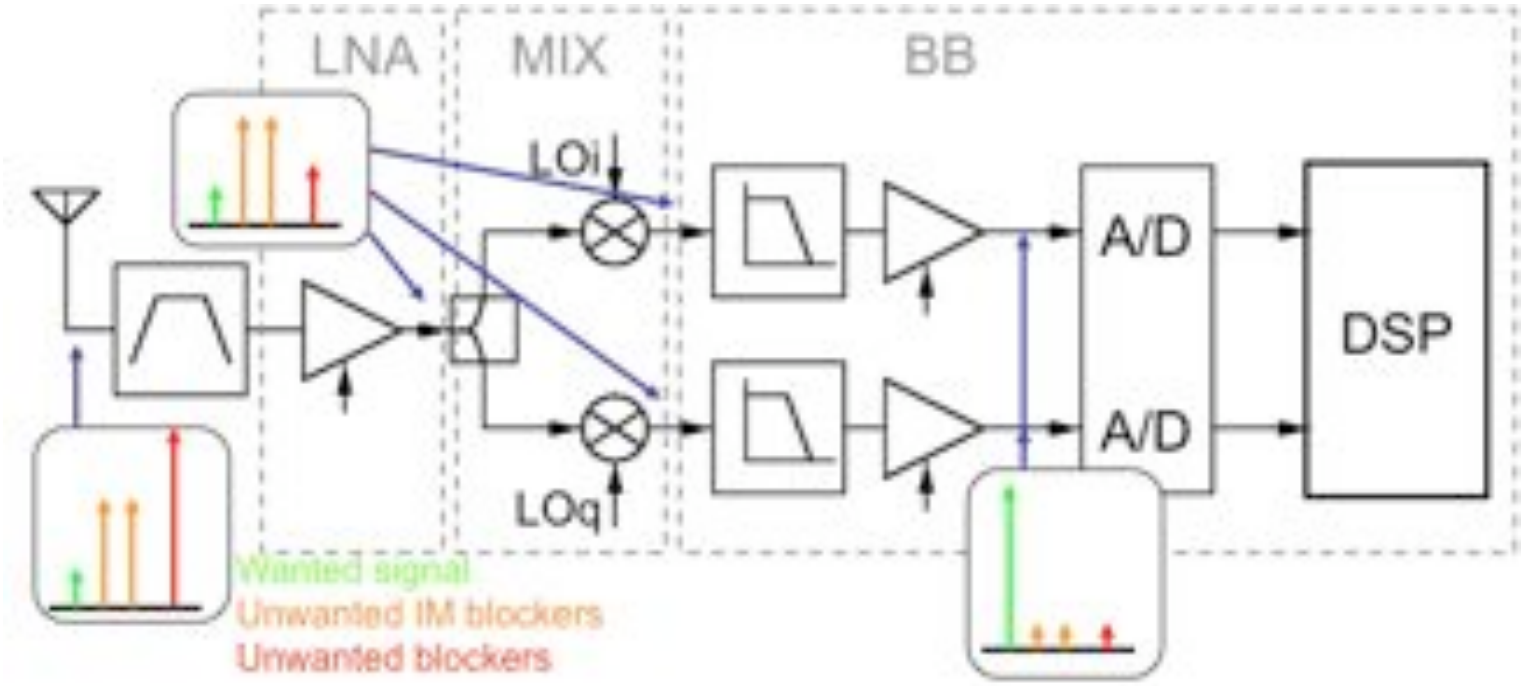


Scale the **Supply Voltage** of Analog/RF Circuits

Reduce the **Area** of RF circuits

Use **Digital Gates** to Improve Analog/RF Performance

Use Digital Gates In RF… How?

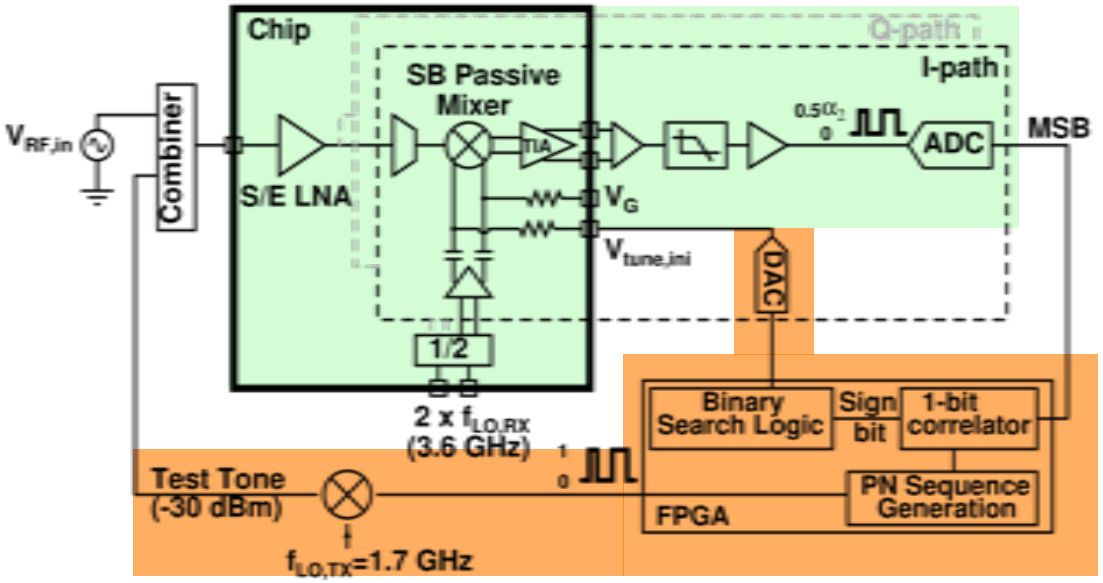


- For RF, improvement of linearity using digital gates has many opportunities
- The signals generating the errors are *out-of-band interferers,* which do not reach the baseband…
- In contrast to mixed signal digital assistance we need to **address problem in the front-end for RF!**

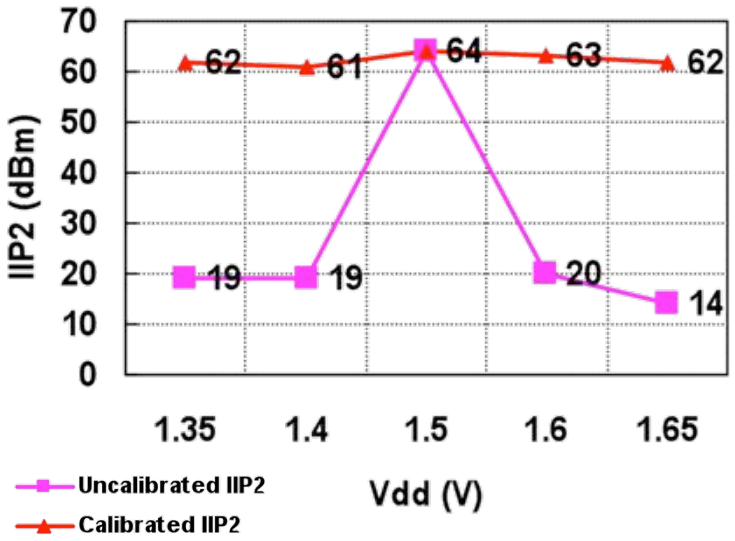
➔ **Use digital assistance to self-calibrate RF front-end**

Digital Self-Calibration of RCV IIP2

Block Diagram



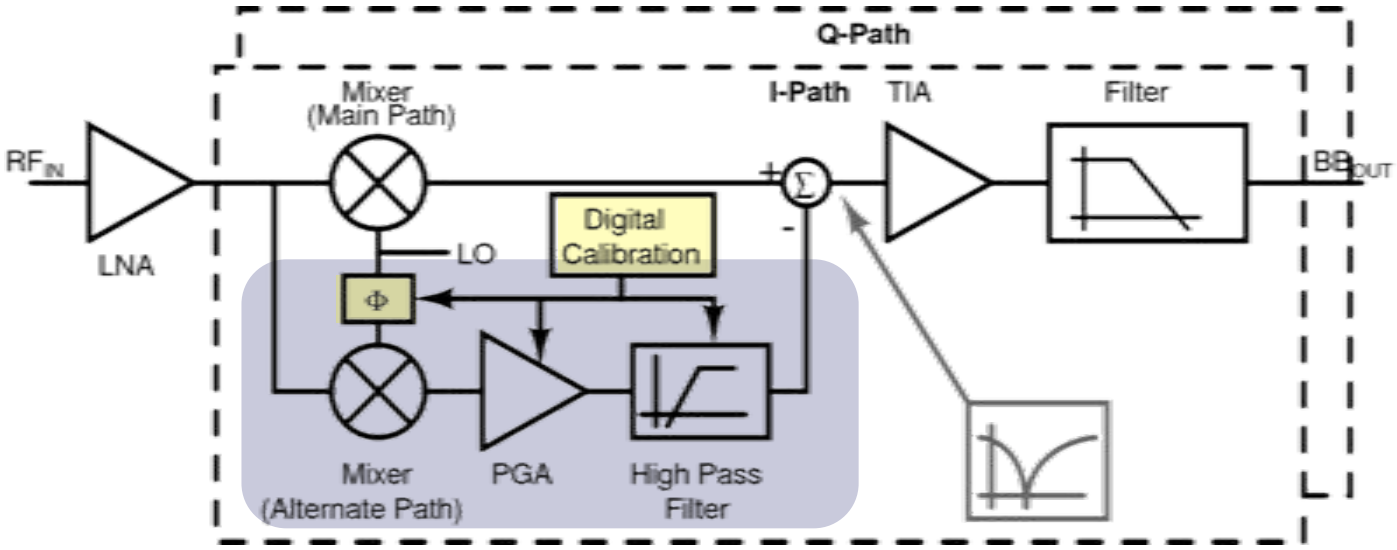
Measured Results Receiver



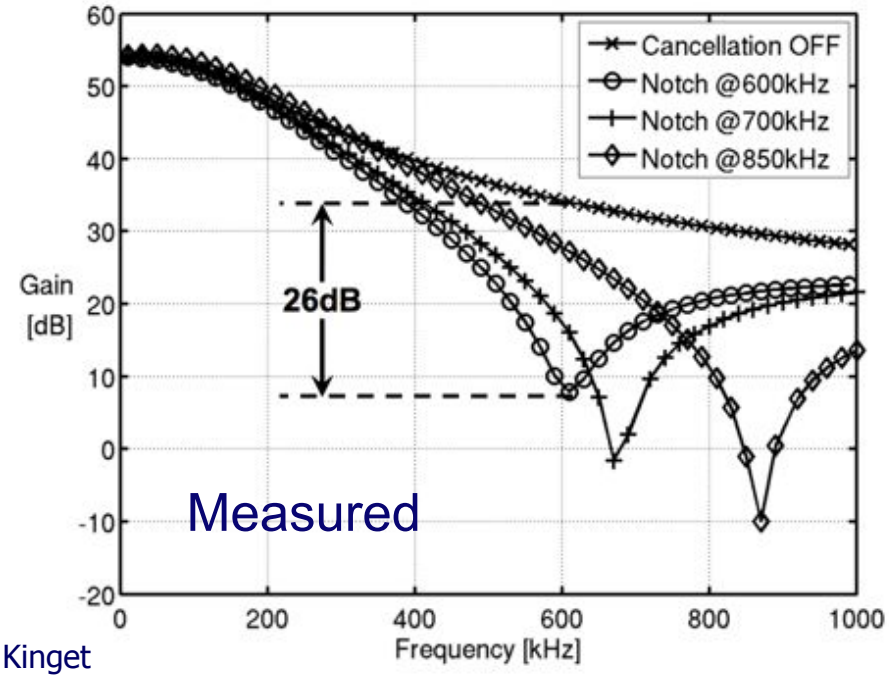
[ISSCC 2010]

- >40dB IIP2 improvement!
- Performance very stable w.r.t. any changes (VDD, freq., …)
- *Simpler, lower power RF circuits* can be used taking advantage of calibration engine
- Low Power, no extra power consumption for RF operation!

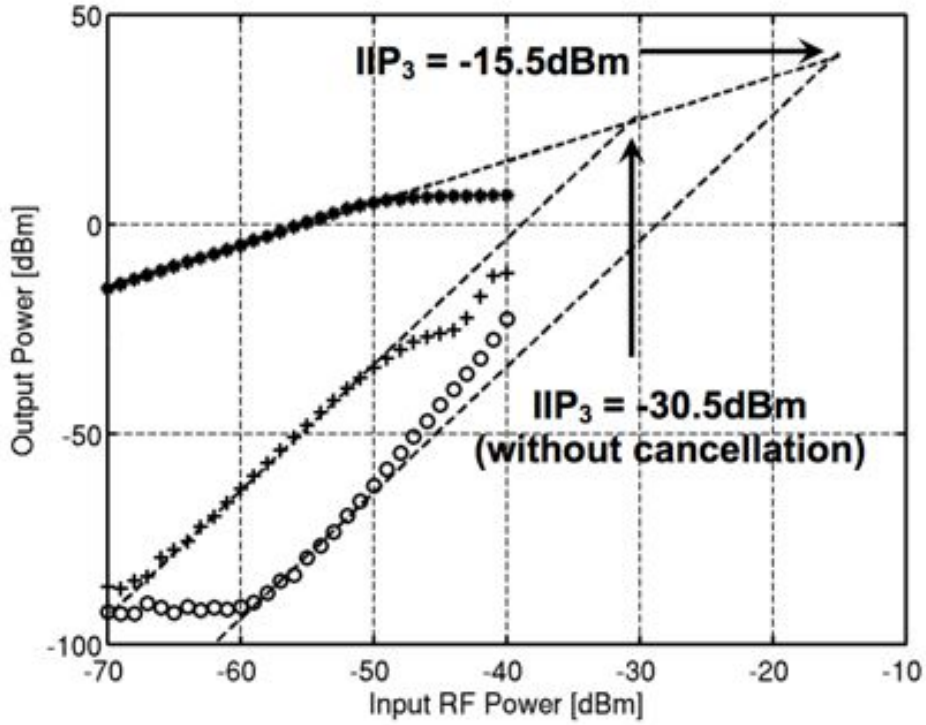
ULV RCV with FF In-band Interf. Cancel.

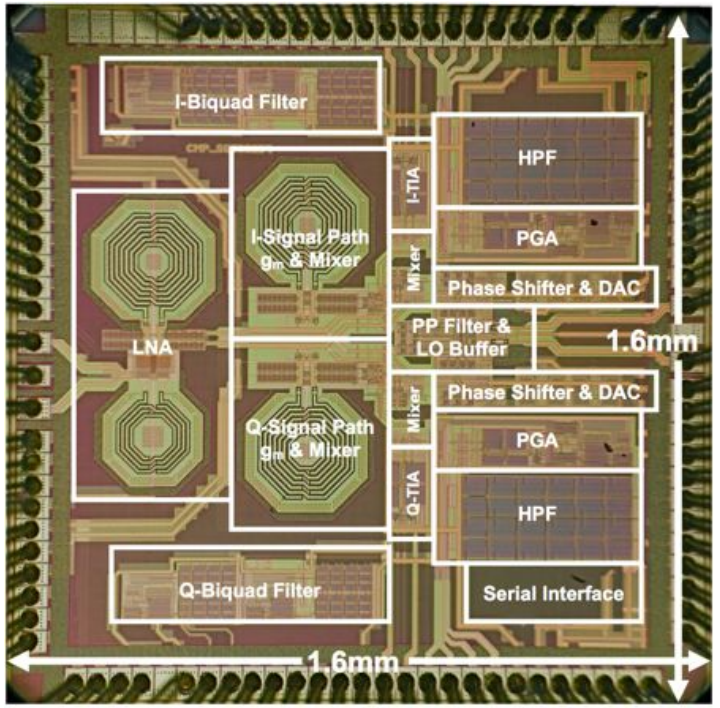


- Front-end ***Interferer Cancellation*** significantly reduces baseband linearity requirements resulting in a significant performance improvement
- >20dB of attenuation for out of channel blockers
- Digital calibration of LO phase (Φ) and alt. path gain is **key enabler** to *automatically* tune the position of the cancellation notch



0.6V GSM Receiver



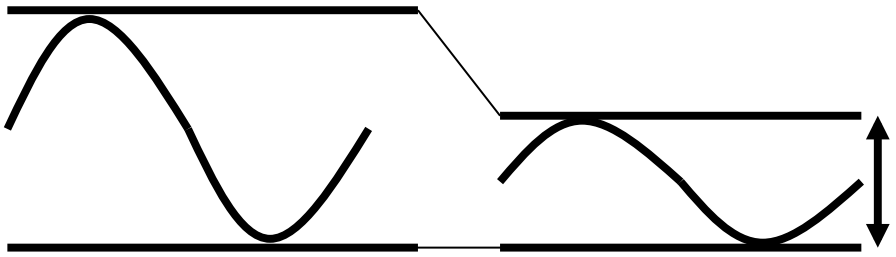


[VLSI, 2010]

- 55dB Gain, 6dB NF, -15.5dBm IIP_3,
- 21mW @ 0.6V (LNA, Mixers, Cancellers, Baseband, LO Buffers)
- 65nm CMOS

Review & Outlook

Fundamentals: Power Limits



$$V_{DD} = 2\sqrt{2}\,V_{RMS}$$

- Noise limited circuits [Vittoz90]:

$$SNR = \frac{V_{RMS}}{\sqrt{v^2_{n,RMS}}} \qquad \overline{v^2}_{n,RMS} = \frac{kT}{C} \qquad I_{DC} = 2f\,C\sqrt{2}V_{RMS}$$

$$P \geq 8\,kT\,f\,SNR^2$$

ideal class B

- Mismatch limited circuits [Kinget96]:

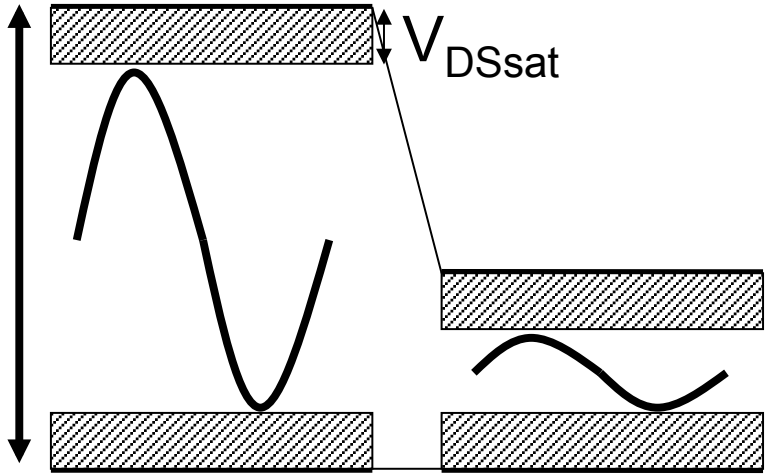
$$Acc = \frac{V_{RMS}}{3\sigma(V_{os})} \qquad \sigma^2(V_{os}) = \frac{C_{ox}A^2_{VT}}{C} \qquad I_{DC} = 2f\,C\sqrt{2}V_{RMS}$$

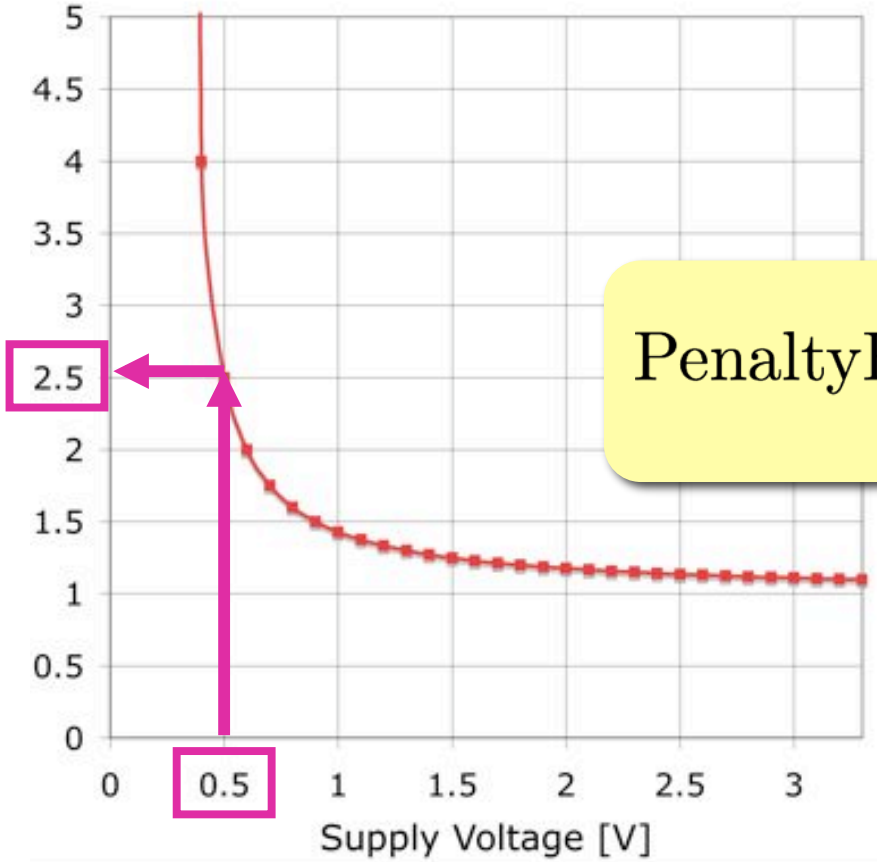
$$P \geq 24\,C_{ox}\,A^2_{VT}\,f\,Acc^2$$

Low Voltage Power Penalty

- Finite V_{DSsat}:

$$V_{DD} = 2\sqrt{2}\,V_{RMS} + 2V_{DSsat}$$

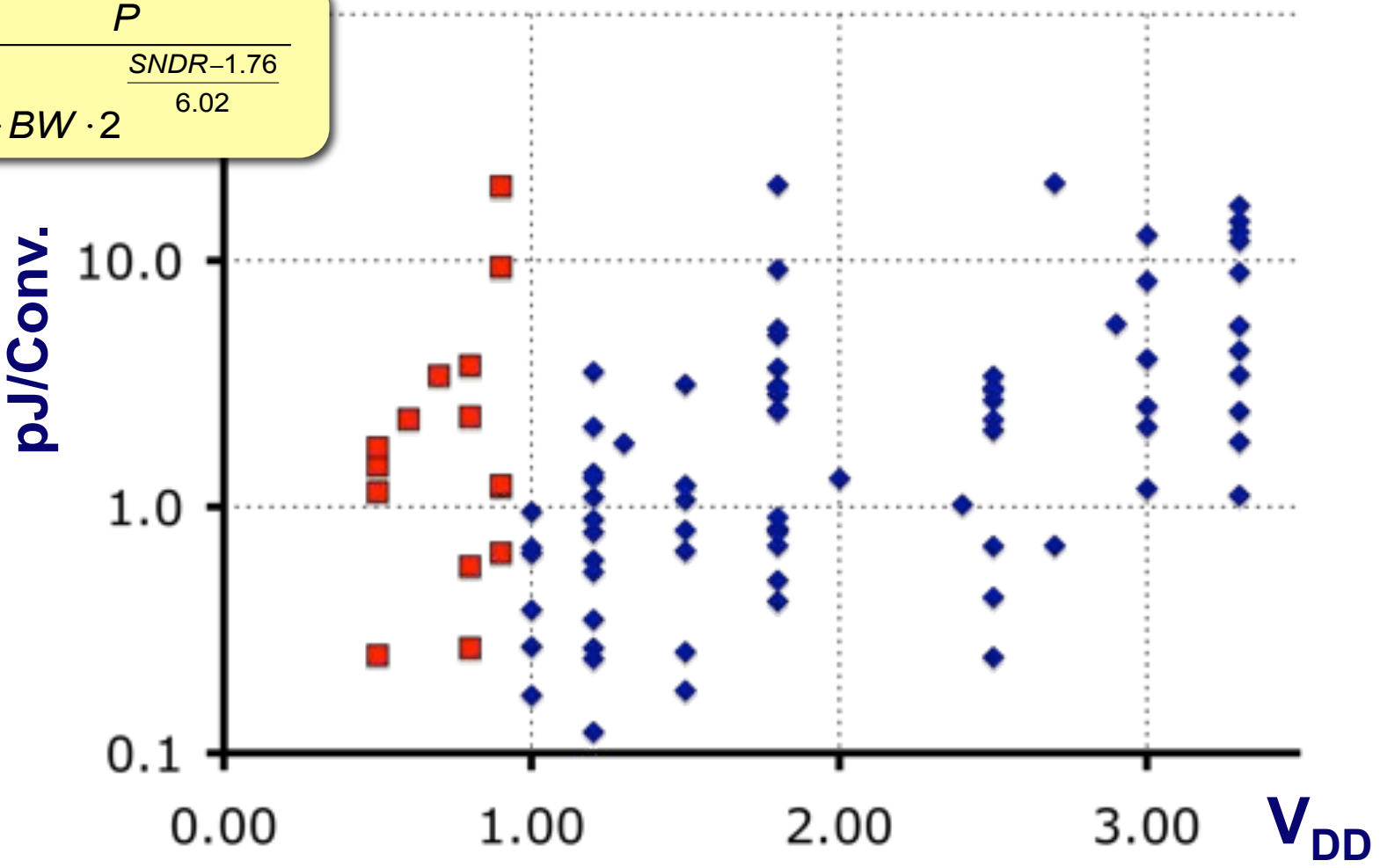




$$\text{PenaltyFactor} = 1 + \frac{2V_{DS,sat}}{V_{DD} - 2V_{DS,sat}}$$

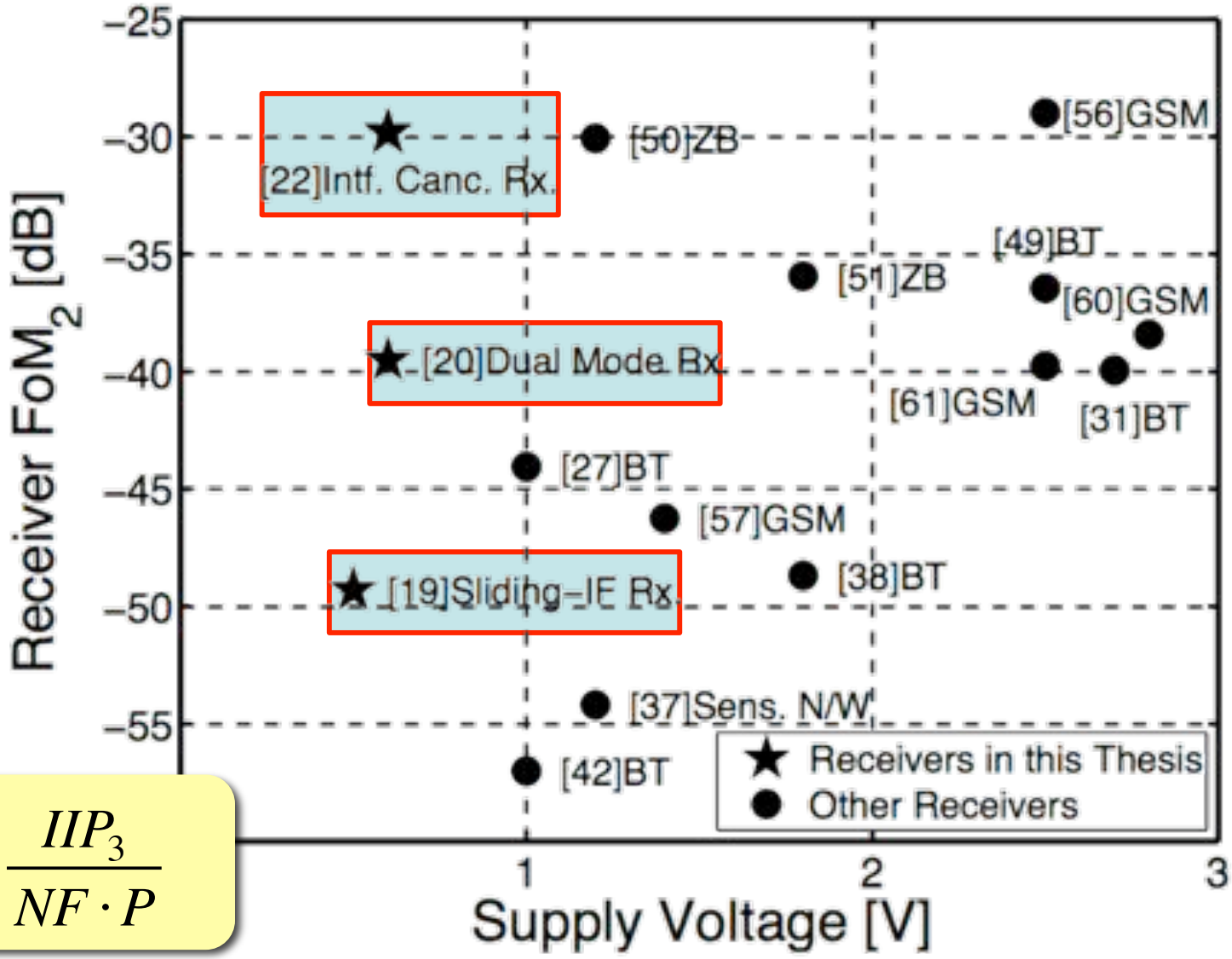
ADC FOM vs V_{DD}

$$\text{FOM} = \frac{P}{2 \cdot BW \cdot 2^{\frac{SNDR - 1.76}{6.02}}}$$



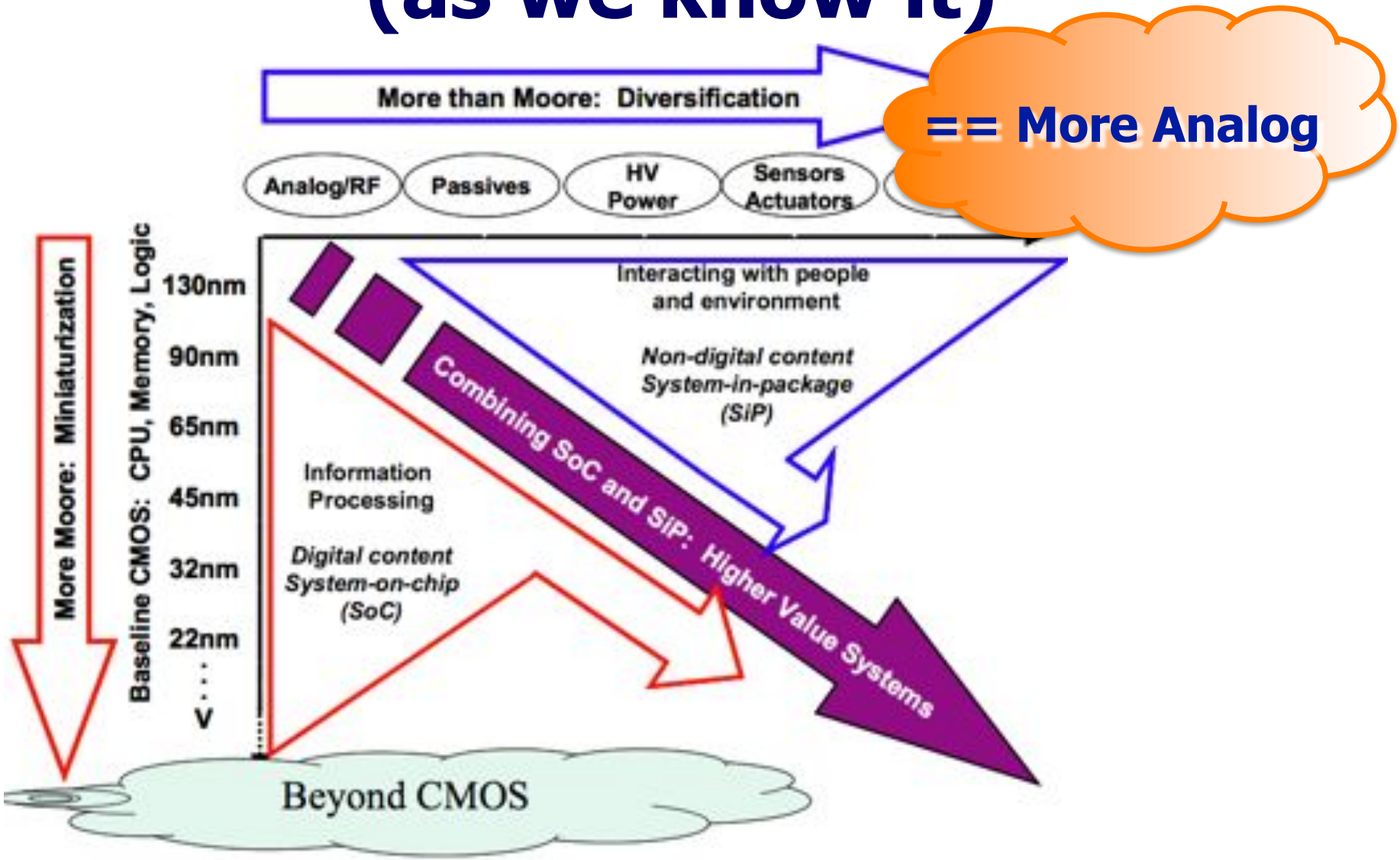
Most data taken from B. Murmann,
"A/D Converter ISSCC Performance Data"

Receiver FOM vs V_{DD}



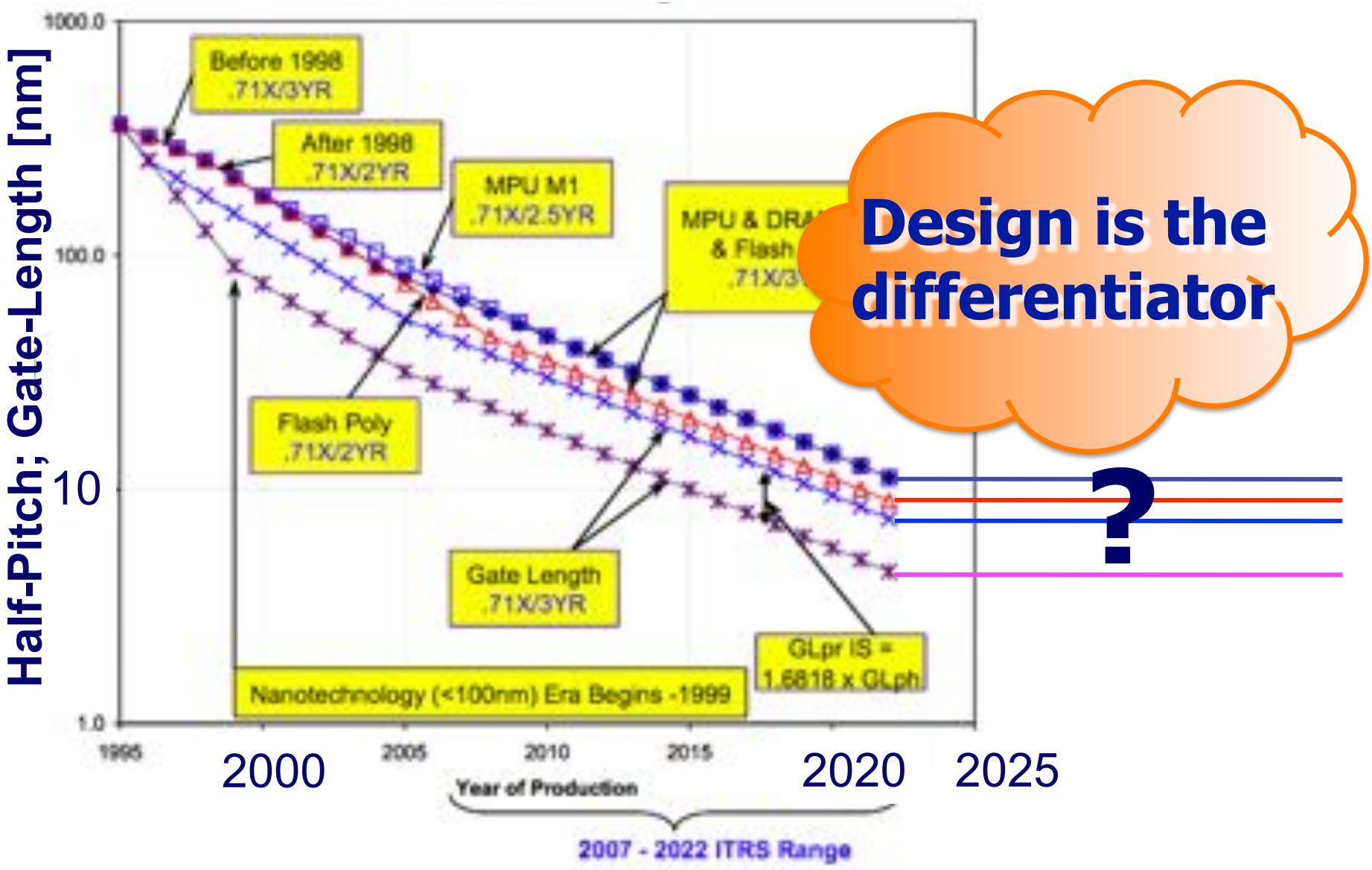
$$\mathrm{FOM}_2 = \frac{IIP_3}{NF \cdot P}$$

End of Moore's Law…?
(as we know it)



[ITRS 2007]

ITRS 2007-2022 – After Moore?



Conclusions

- Scaling is driving semiconductor technology and will continue for another decade, but with significant design challenges.
- Future Analog/RF in nanoscale CMOS
  - ➔Reduce supply voltage
  - ➔Reduce area
  - ➔Exploit digital gates
- Design is becoming a prime differentiator

Plenty of open opportunities!!

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- Collaborators: Y. Tsividis, K.P. Pun (Chinese Univ. Hong Kong), S. Chatterjee (now IIT Delhi), F. Zhang (now TI), B. Hung and T.L. Li (UMC), A. Balankutty (now Intel), Y. Feng (now MHI Consulting), J. Shen (now ADI), N. Stanic (now SiLabs), C. Vezyrtzis, and S. Yu (now MaxLinear).
- Analog Devices, Bell Labs, Broadcom, Intel, Marvell, Silicon Labs and Toshiba for financial support.
- Europractice, Philips (now NXP) , Toshiba , ST Microelectronics and UMC for fabrication support.
- Integrand Software for EMX software.

Thank you for your attention!

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See http://www.ee.columbia.edu/~kinget/publications.html

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