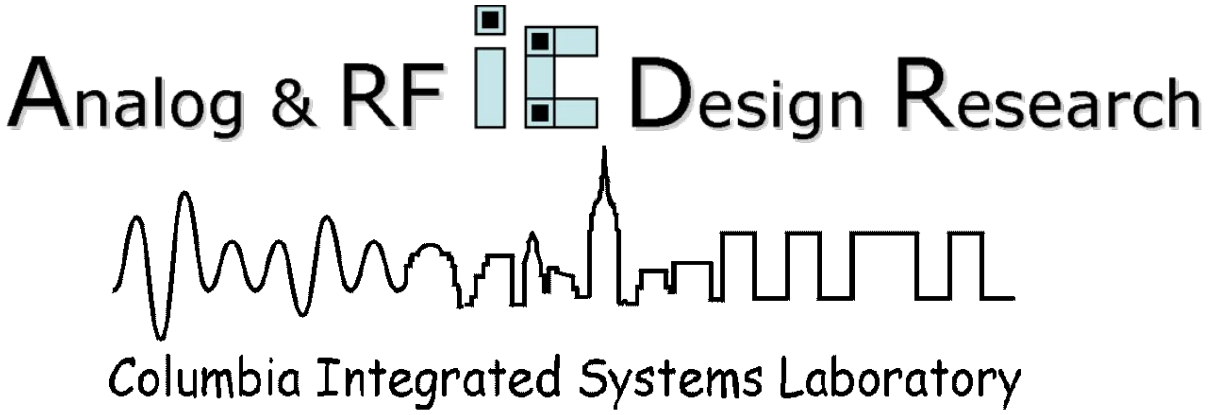
COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

Designing Analog and RF Circuits for Ultra-Low Supply Voltages

Peter Kinget



Motivation

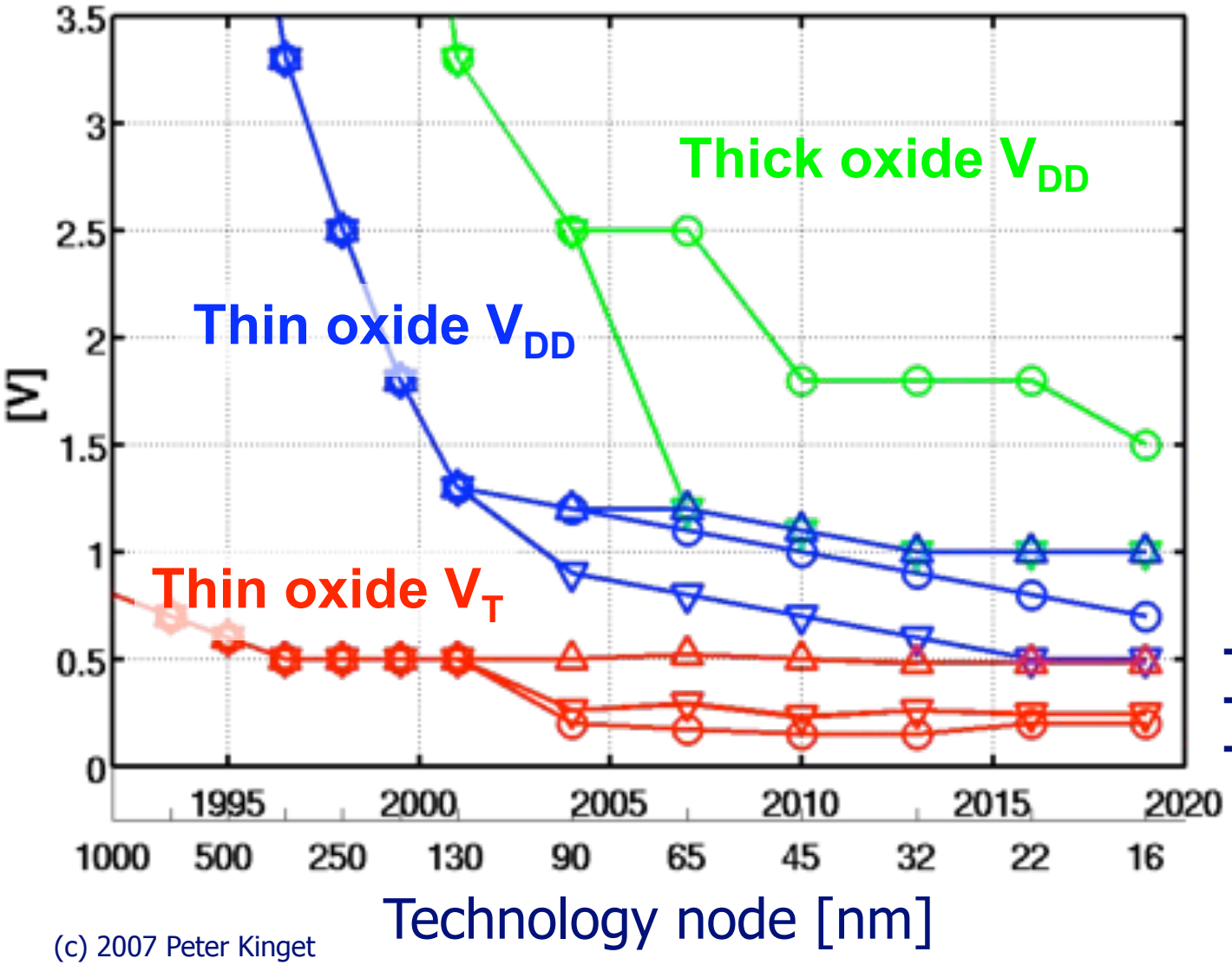
- Past 4 decades in electronics:

  IC Technology Progress ≡ Device Scaling

  IC Design Progress ≡ More Integration

- Sub 100nm technologies…

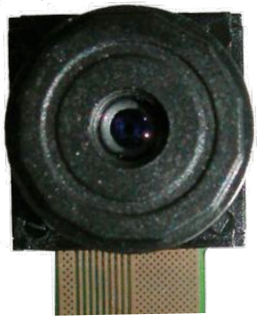
Nano CMOS : Supply Voltage



[ITRS'05]

–O– High Perf.
–Δ– Low Standby
–V– Low Power

World is Analog *^%&*$;-)



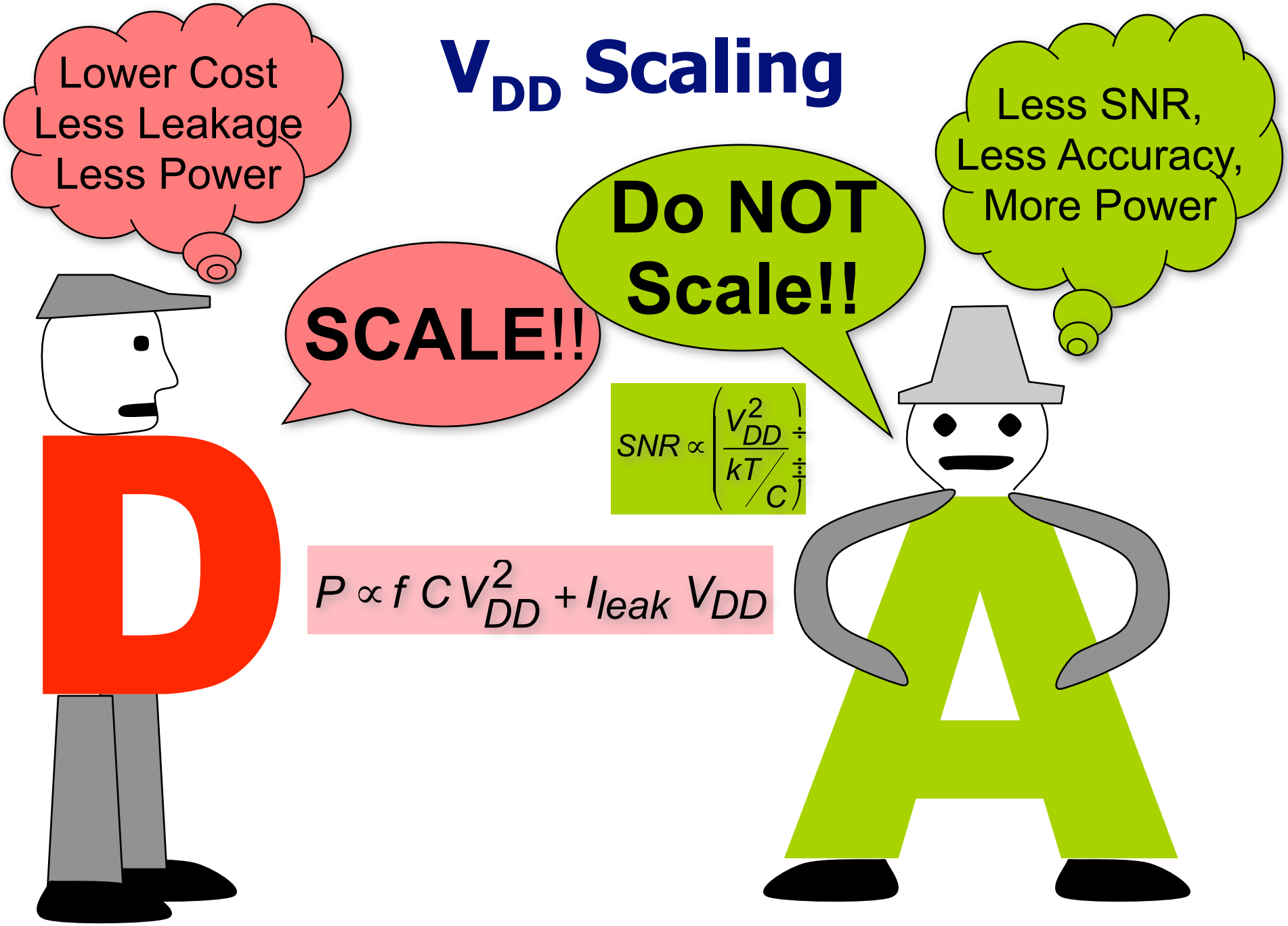
Analog/RF Interfaces

Digital Core

SOC

'Analog & RF bring the bits to life'

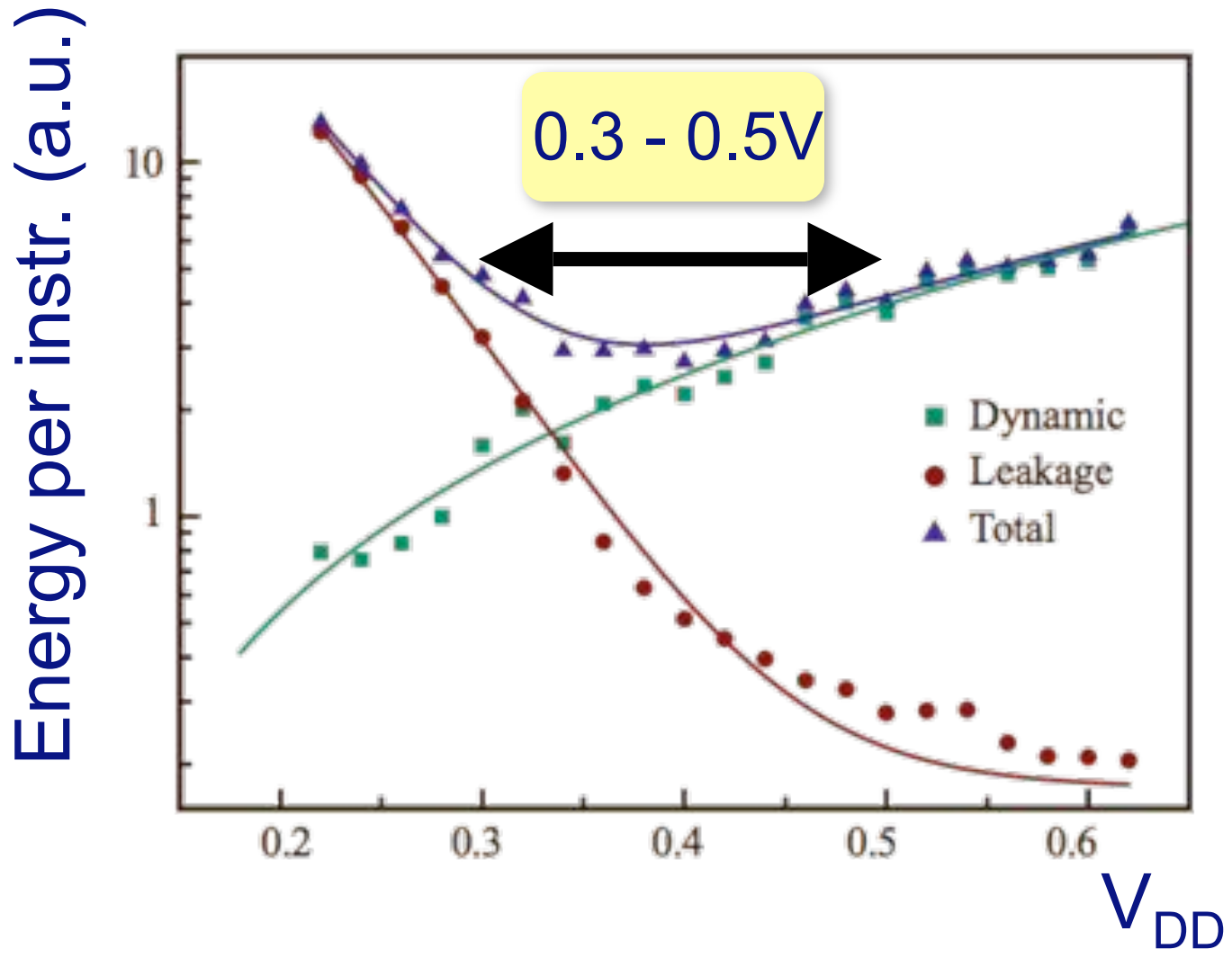
V_{DD} Scaling



$$SNR \propto \left(\frac{V_{DD}^2}{kT/C} \right)$$

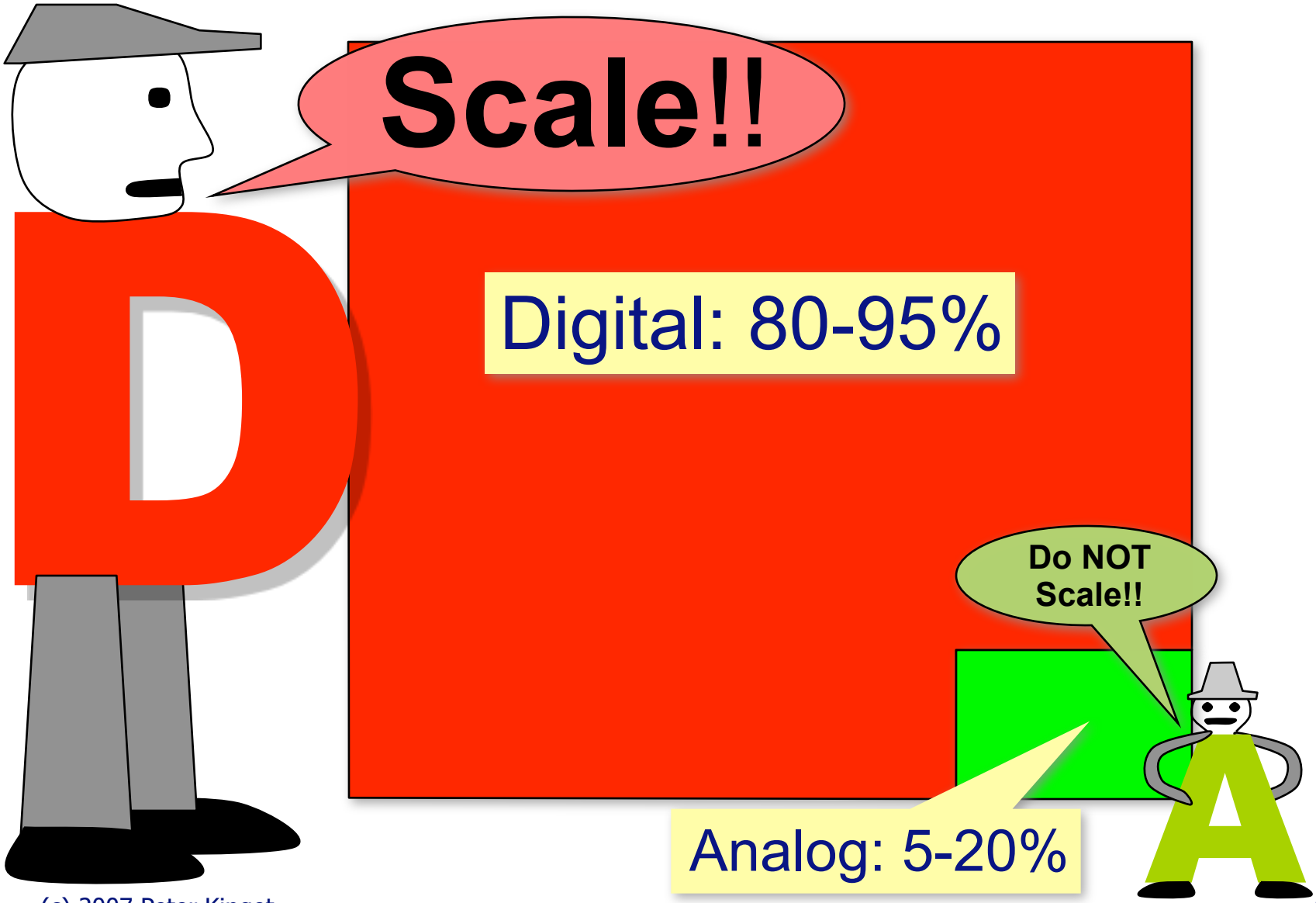
$$P \propto f\, C\, V_{DD}^2 + I_{leak}\, V_{DD}$$

Lowest Energy Digital V_{DD}



- [Hanson 2006] 8-bit microprocessor in 0.13um CMOS

System on a Chip



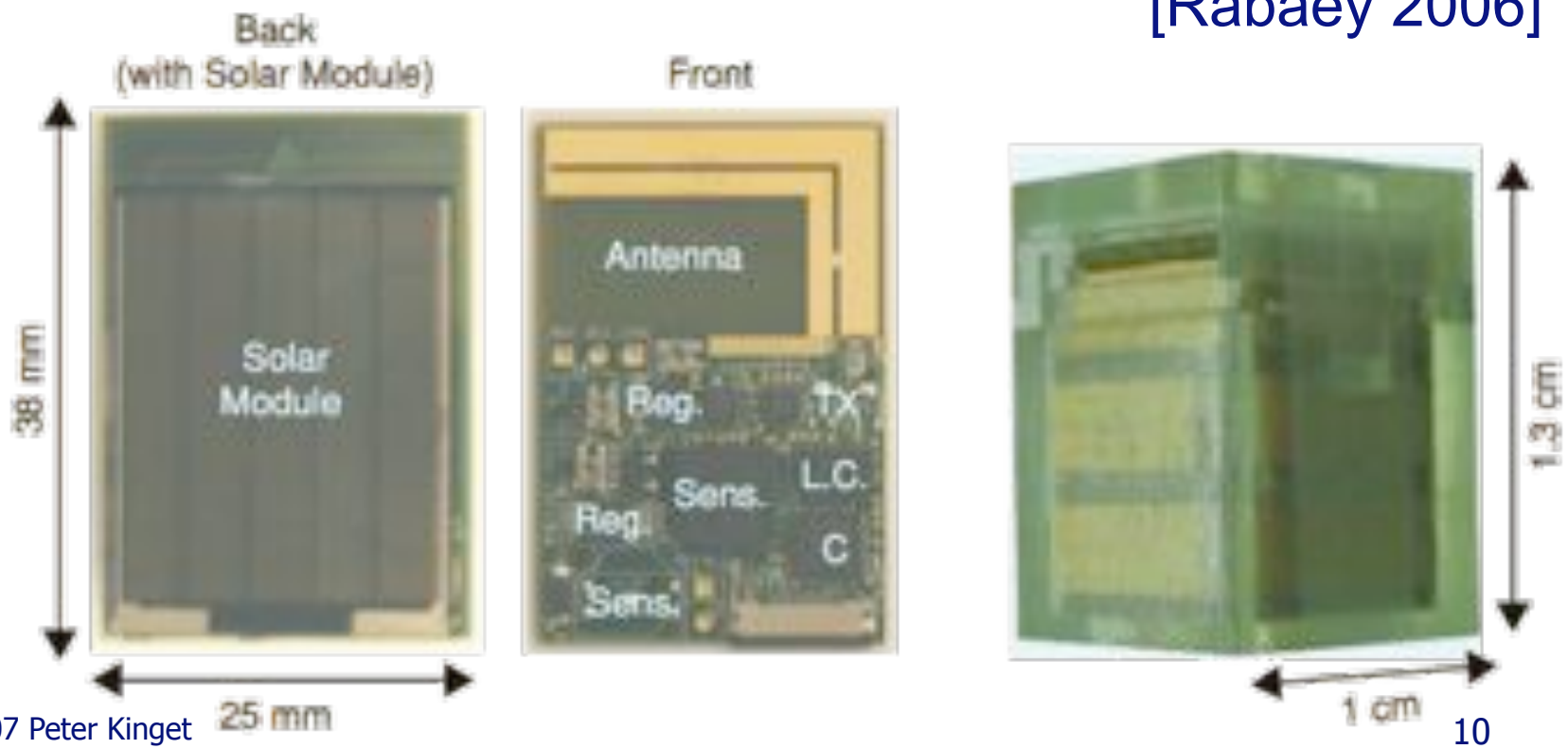
Of course

- There are **thick oxide devices**;
- There are **DC-DC converters** or **custom supplies**;
- Heterogeneous technologies can be combined with **system in a package**,….

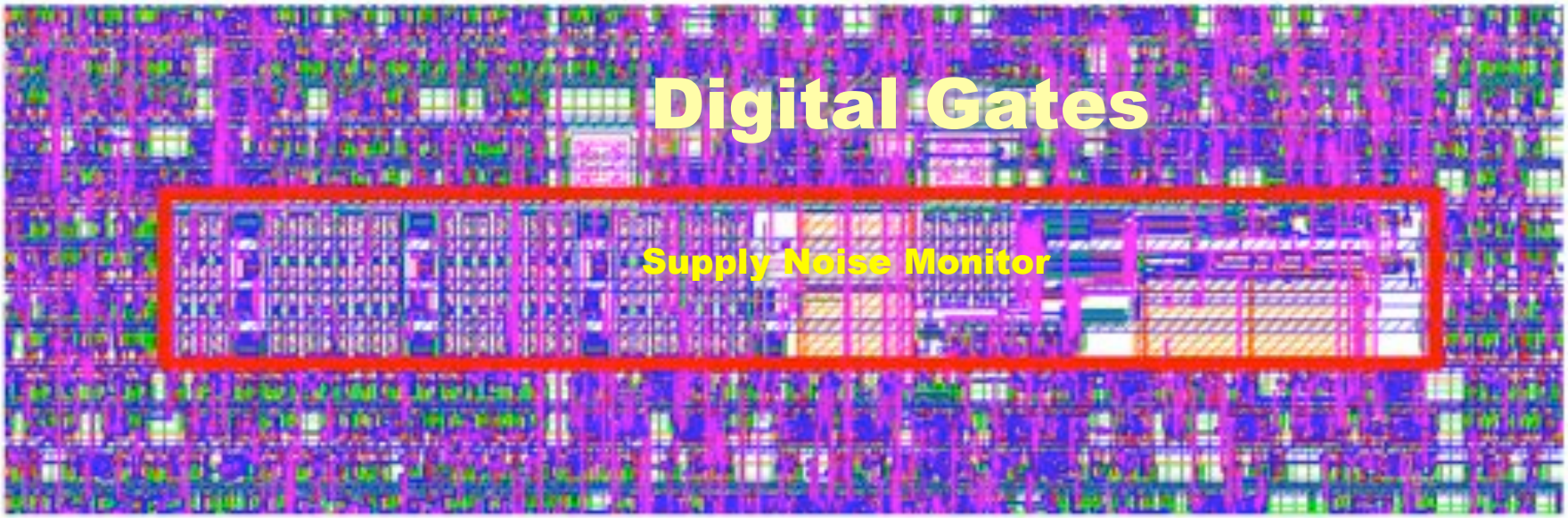
"Disappearing Electronics"

- E.g., pico nodes in wireless sensor nets
  - Scavenge energy with one solar cell
  - V_{DD} 0.4 to 0.5V

[Rabaey 2006]



Analog Assist for Digital



[Petrescu 2006]

- Embed analog monitors in digital circuits to monitor temperature, V_{TH}, V_{DD}, substrate interference, signal integrity, ….
- **Need to be fully compatible to digital** (layout, VDD, technology, …)

So, let's **explore,**

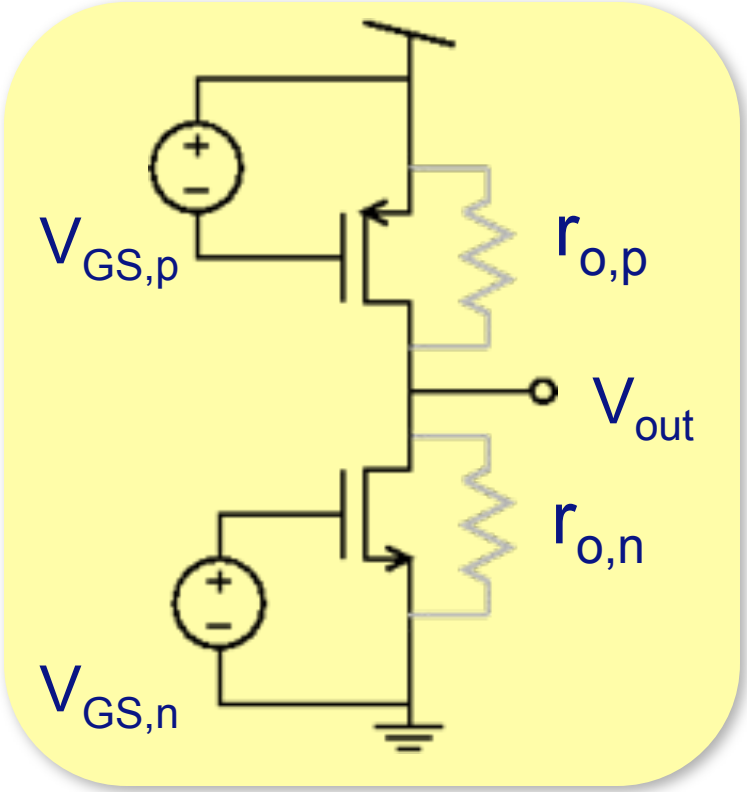
how we can design

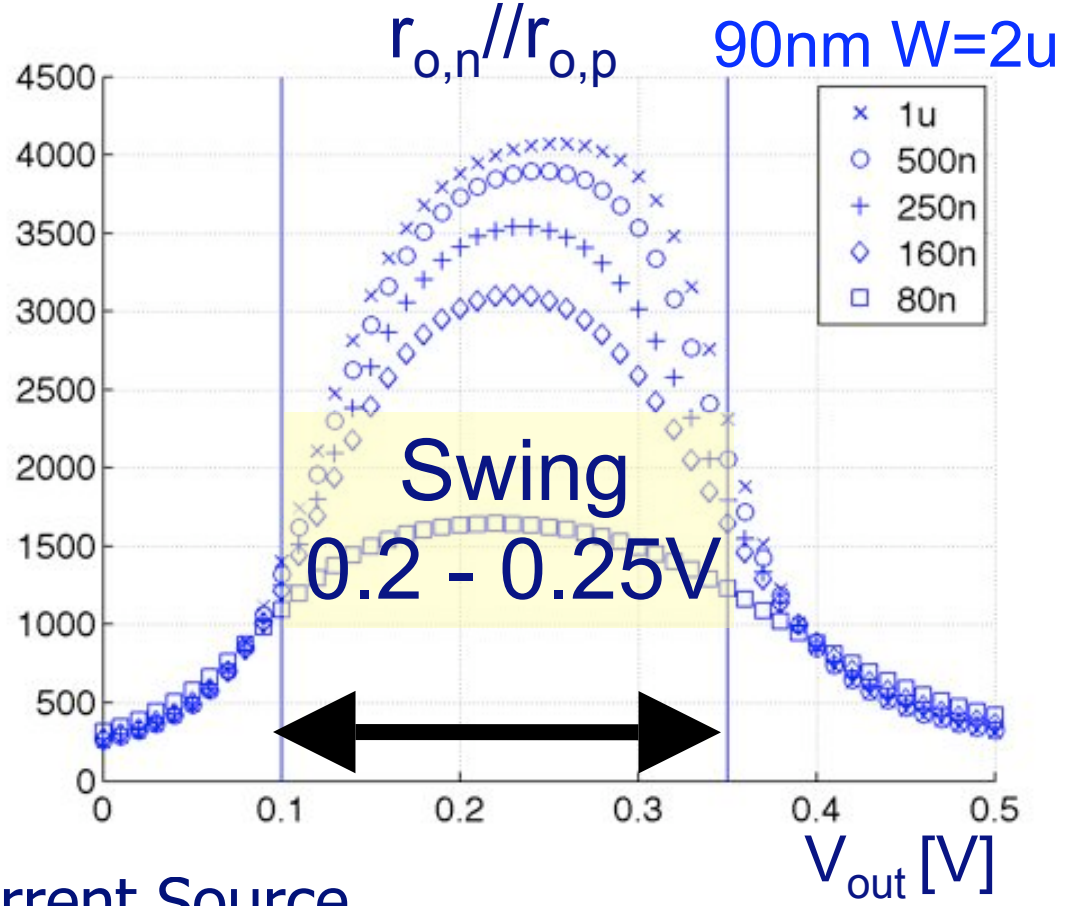
ultra-low voltage analog & RF ICs?

Outline

- Motivation
- The Challenges
- The Opportunities
  - Device Sizing & Biasing
  - Building Block Topologies
  - System Level Solutions
- Outlook & Conclusions

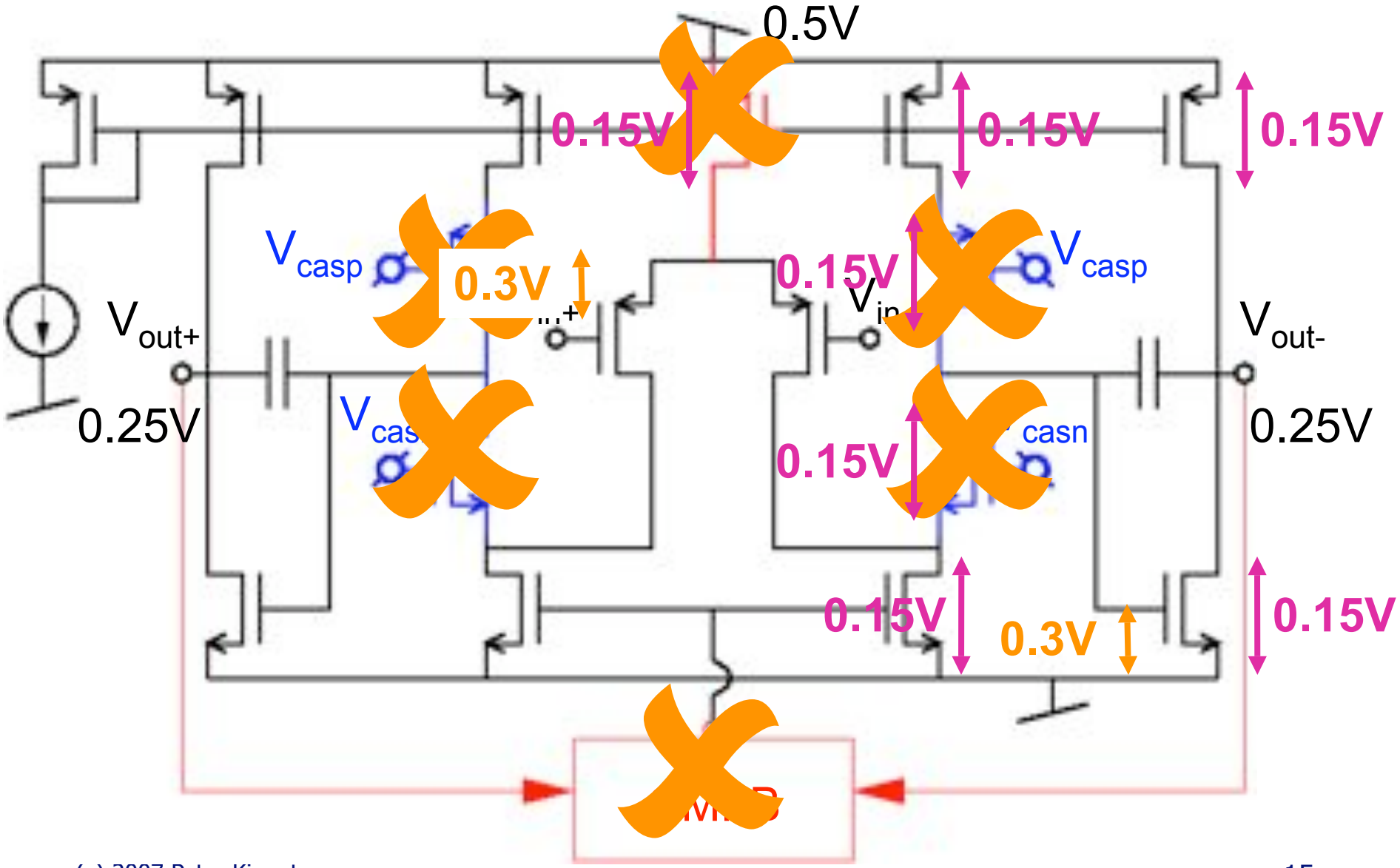
MOST Biasing: CS or VCCS



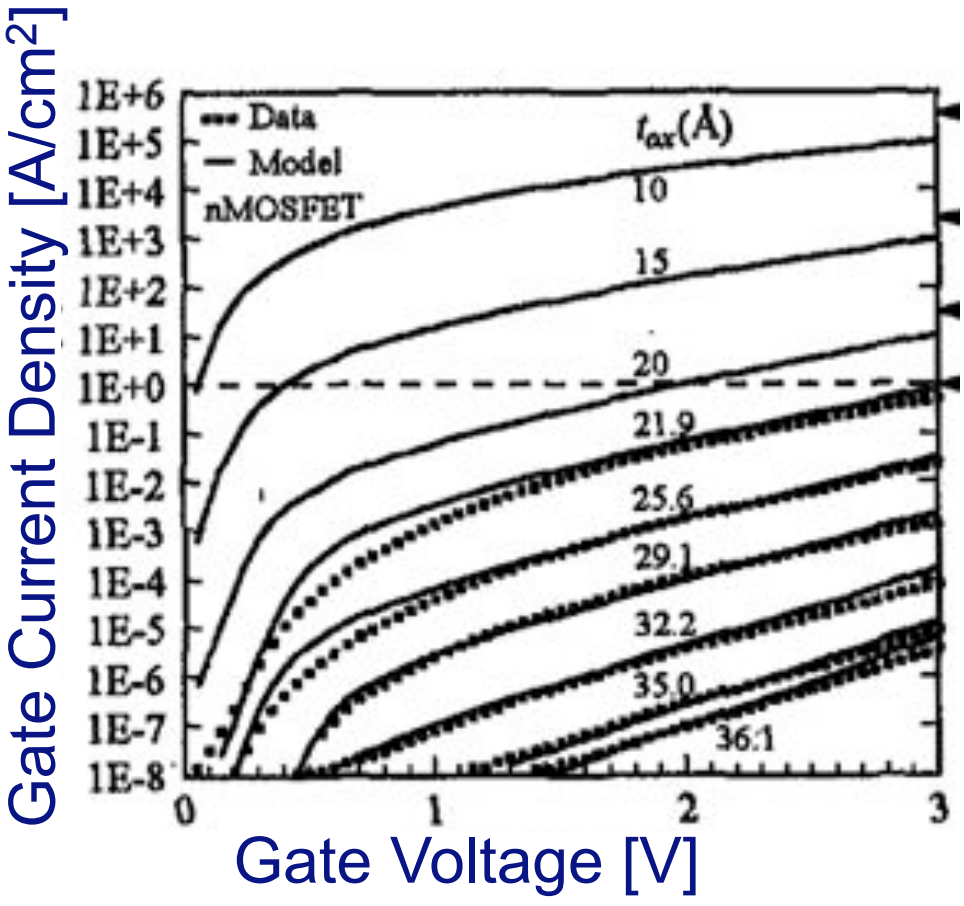


- Transconductor or Current Source
  V_{DS} > 0.1V to 0.15 V (for V_{GS}-V_{TH} ≤ 0.2 V)
- **Moderate to Strong Inversion**
  (V_{GS}-V_{TH}) ≈ 0.15 V & $|V_{TH}|$ = 0.35V → V_{GS} = 0.5V
  $|V_{TH}|$ = 0.15V → V_{GS} = 0.3V

Ultra-LV Challenges in OTAs



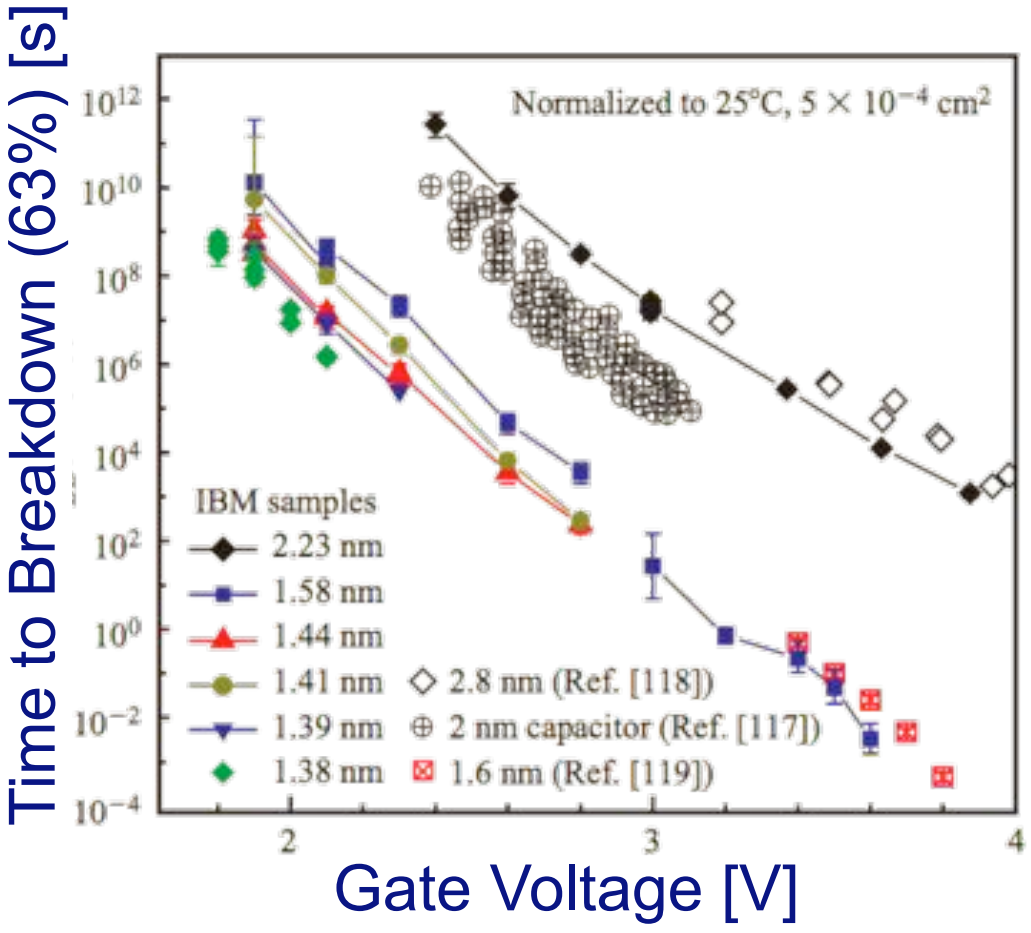
Gate Leakage



[Taur 1999]

Gate current decreases **exponentially** with decreasing oxide voltage

Reliability



[Stathis 2002]

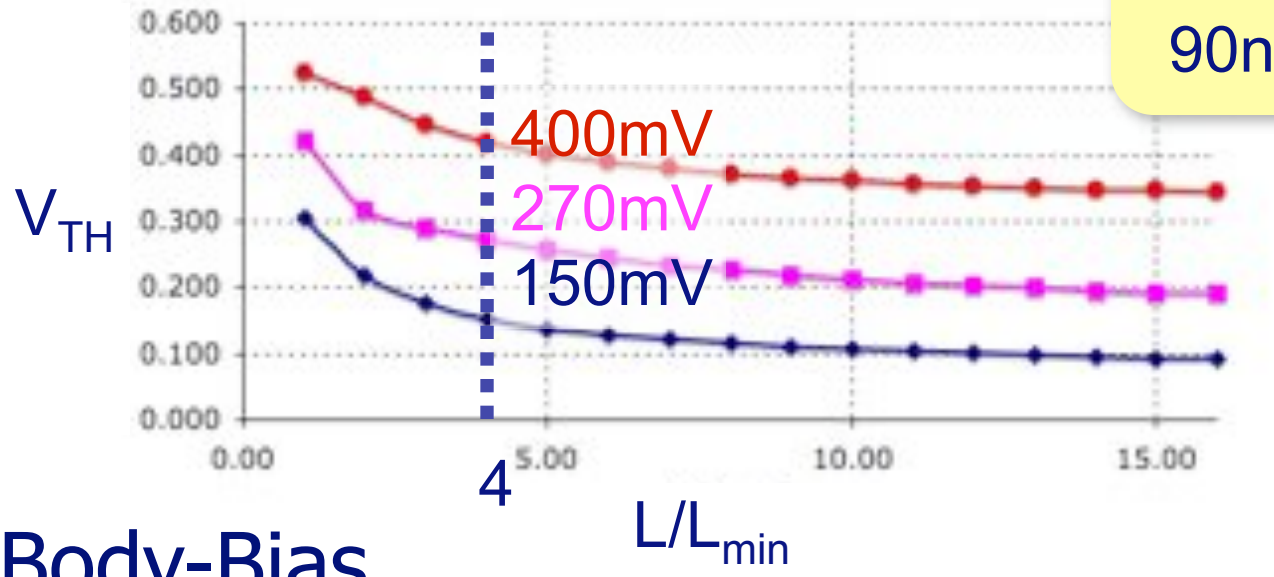
Time to Breakdown increases **exponentially** with decreasing gate voltage

Device Level Solutions

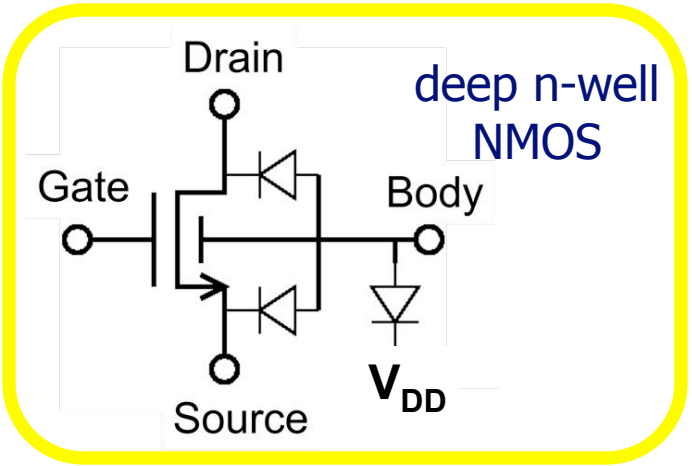
180nm
130nm
90nm

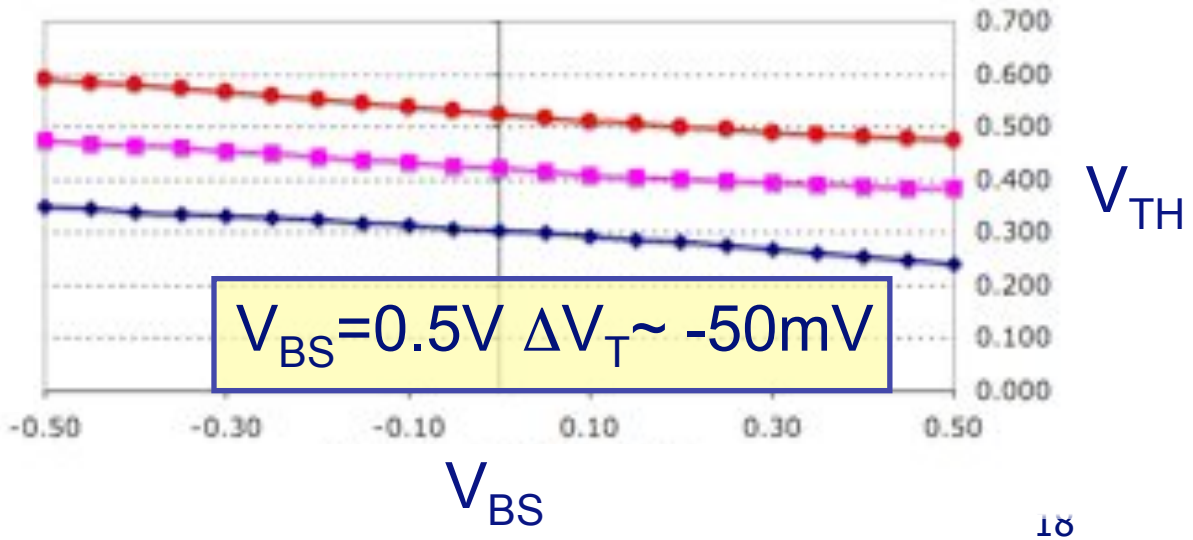
- RSCE

V_T ↓ as L ↑



- Forward Body-Bias



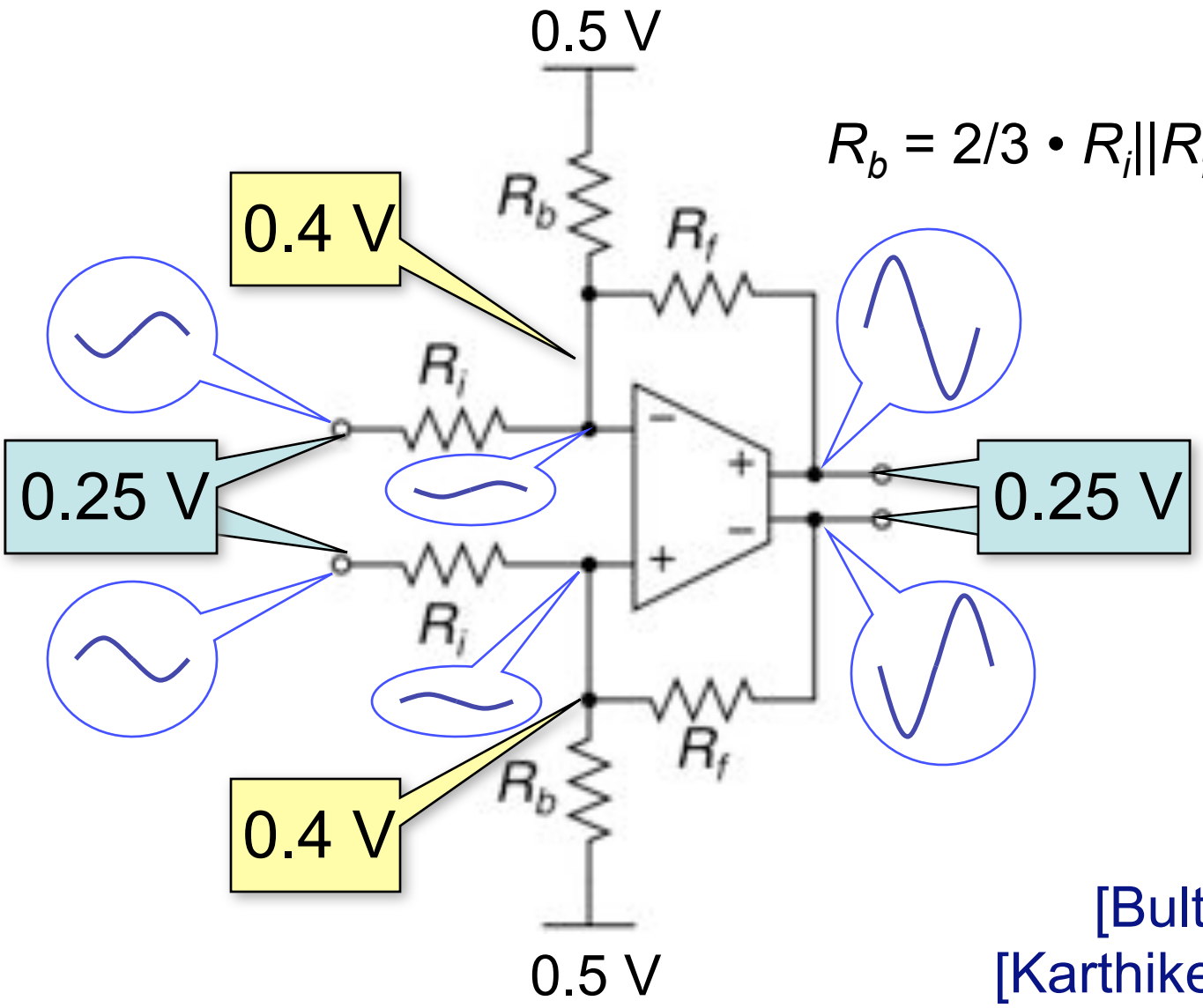


Building Block Solutions

Rethink your topologies!!

- Examples:
  - 0.18um OTAs
    - V_T = 500mV = V_{DD}
  - 90nm OTAs
    - V_T= 150-300mV

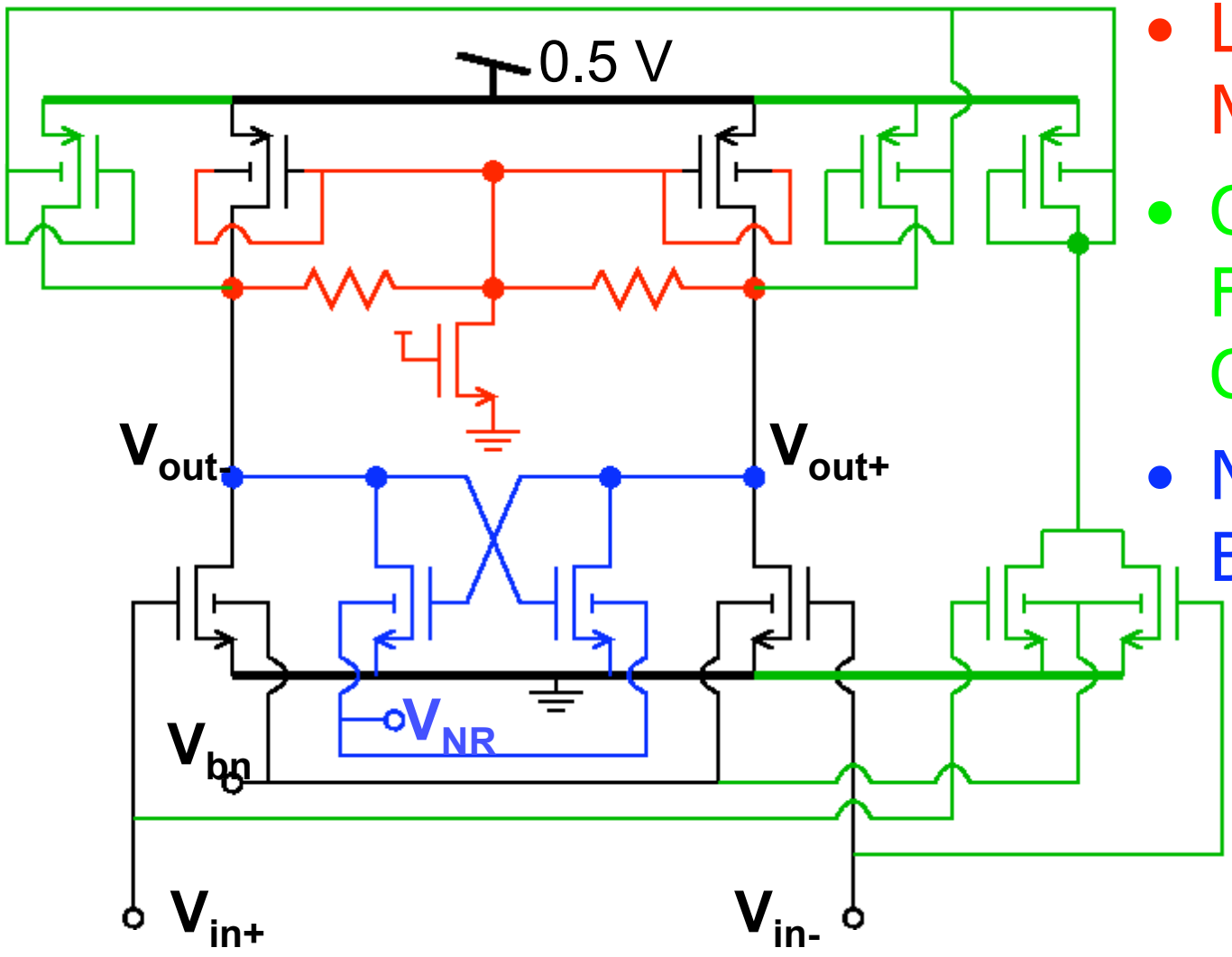
OTAs: CM Level Shifting



$R_b = 2/3 \bullet R_i||R_f$

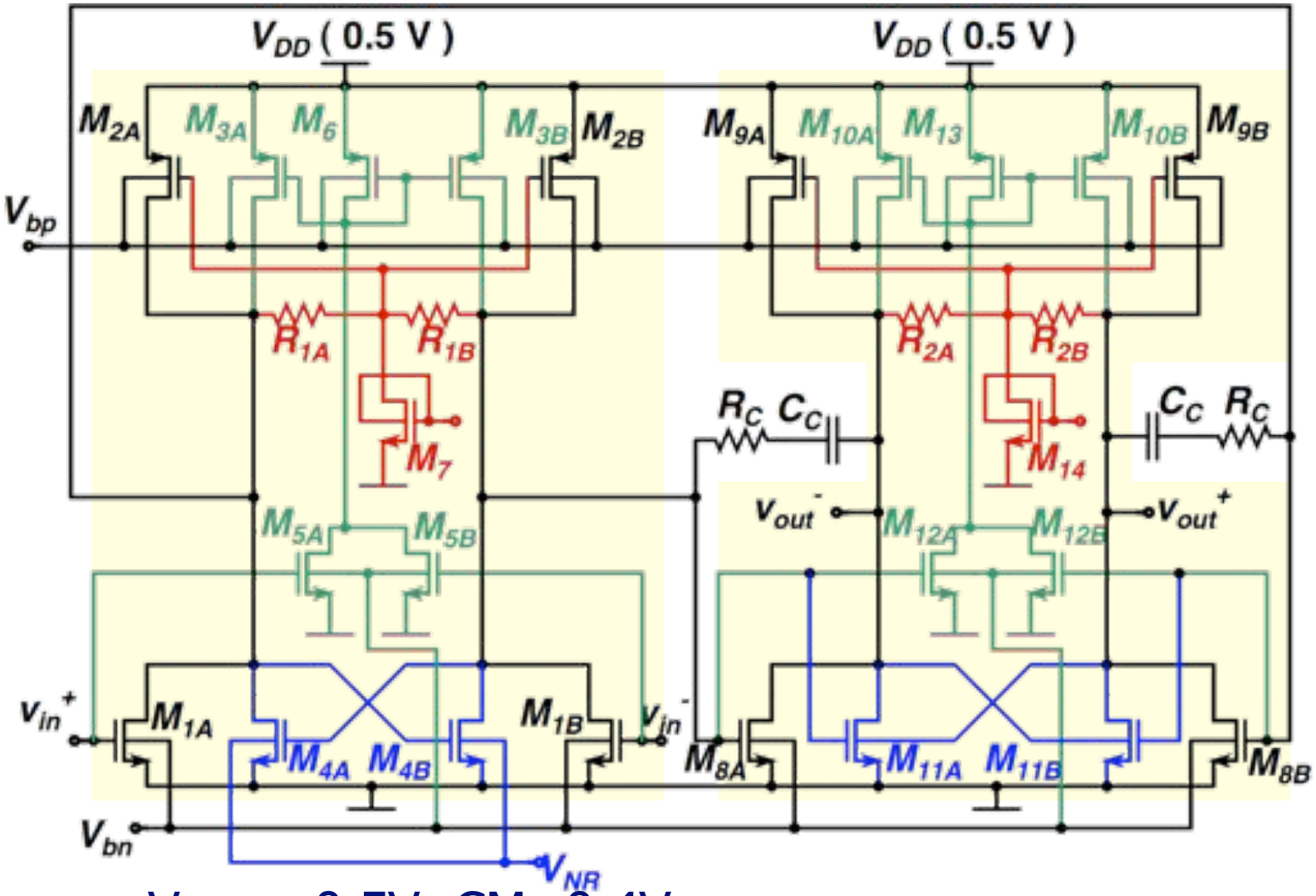
[Bult 2000]
[Karthikeyan 2000]

0.5V Gate-Input OTA Stage



- Local Common-Mode Feedback
- Common-Mode Feed Forward Cancellation
- Neg. G Gain Boost

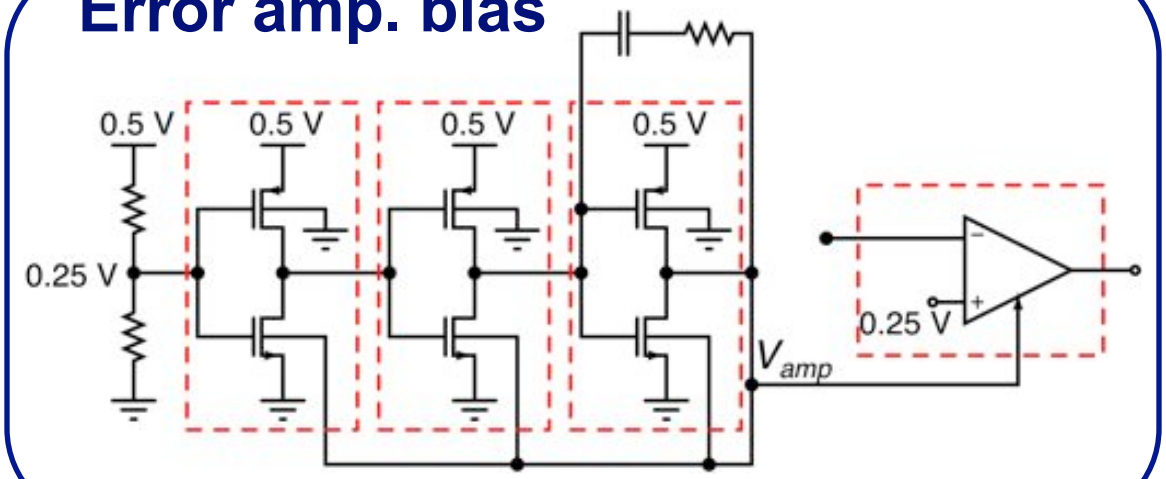
0.5V Two-Stage OTA in 0.18um



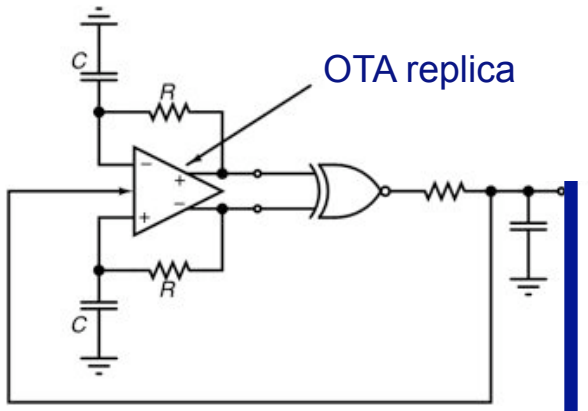
- $V_{T,nom}$=0.5V; CM_{in} 0.4V
- 62dB DC gain; 10MHz GBW; 10pF $C_{L,diff}$; 75uW

On-Chip Biasing Circuits

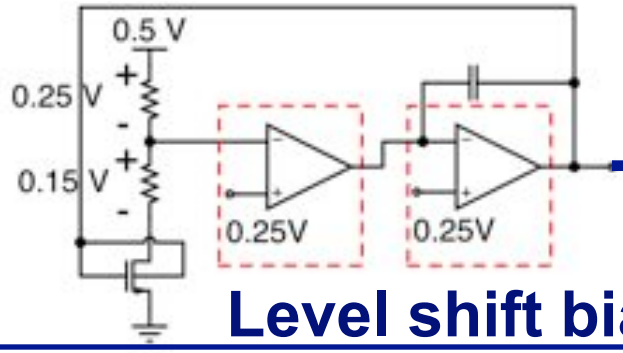
Error amp. bias



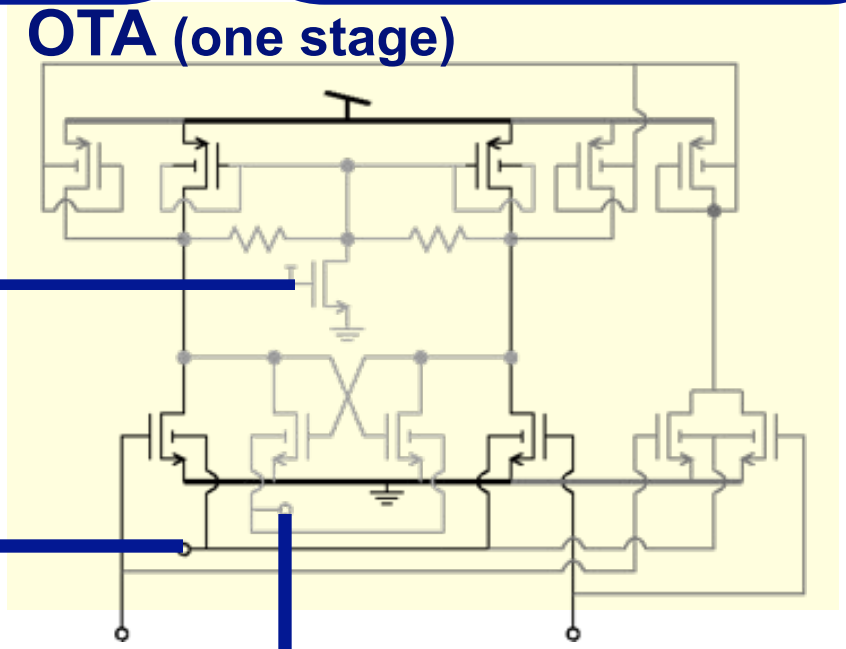
Gain bias



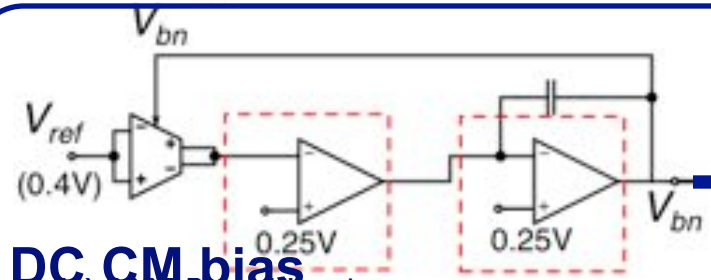
Level shift bias



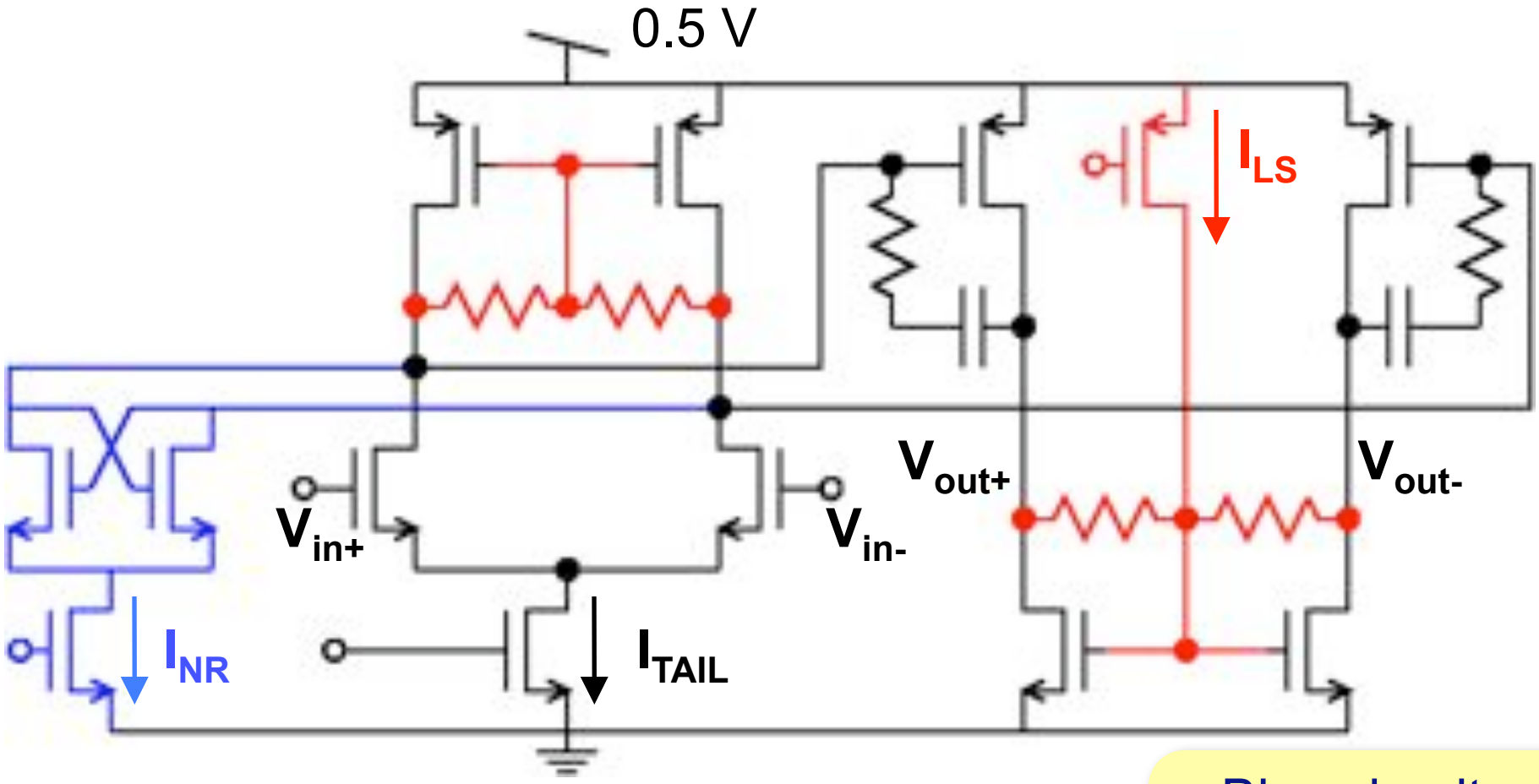
OTA (one stage)



DC CM bias



0.5V Two-Stage OTA in 90nm



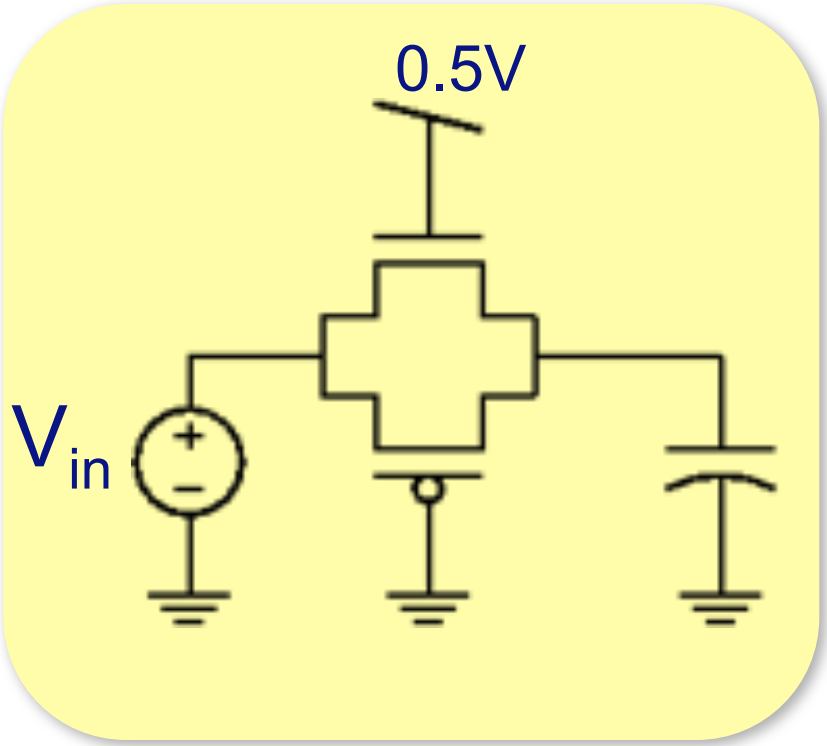
- $V_{T,nom}$=0.3V; CM_{in} 0.25V
- 8dB -G gain boost 1st stage; 45dB DC gain;
- 175MHz GBW; 4pF $C_{L,diff}$; 625uW

Bias circuits not shown
FBB not shown

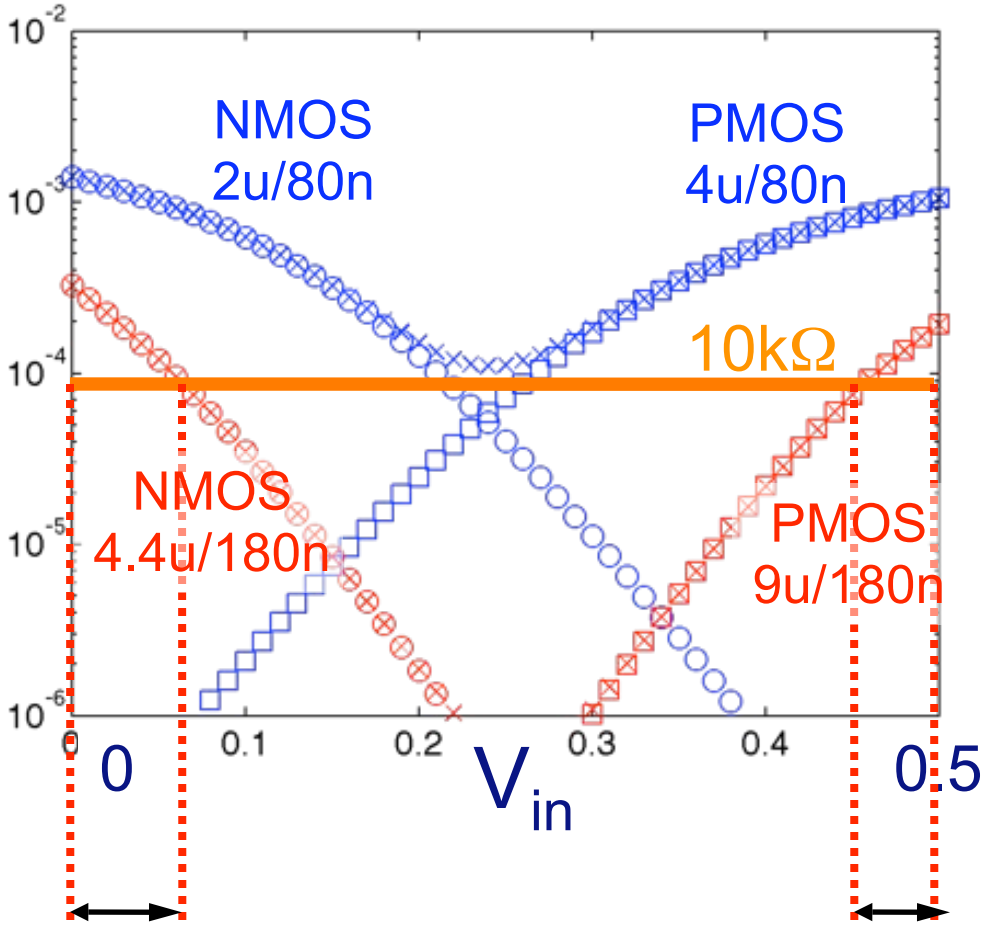
System Functions

- THA, ADCs
  - Floating switch problem
- RF Receivers & Synthesizers
- Continuous-time filters
  - Tuning challenge

Floating Switch Challenge



Conductance

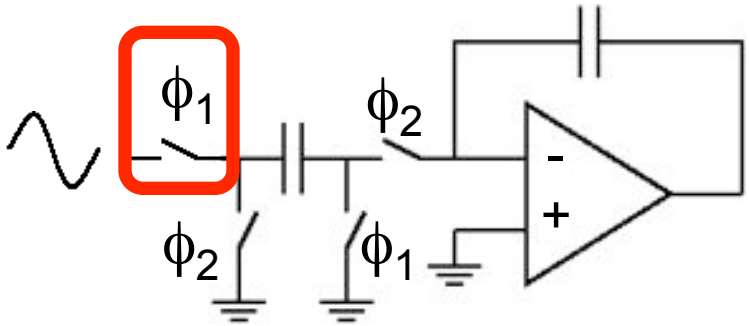


90nm: V_{TH} = 0.3V

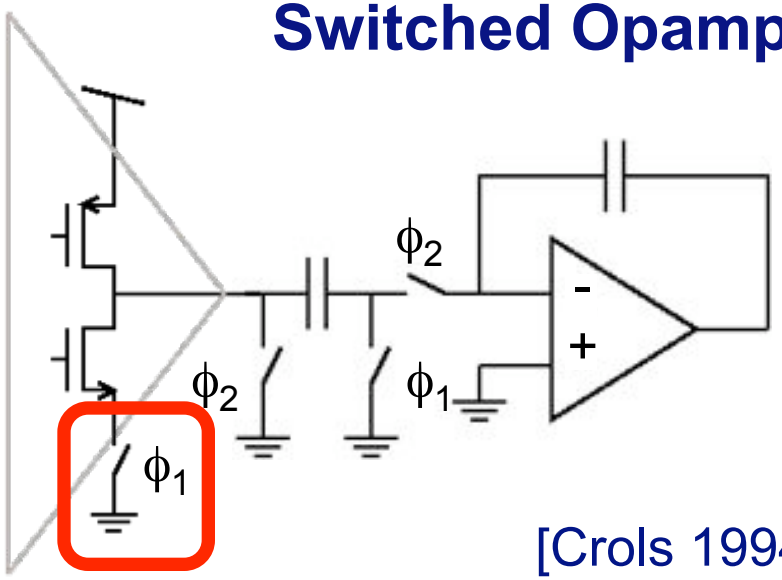
180nm: V_{TH} = 0.55V

Addressing Floating Switches

Low V_{TH} switch

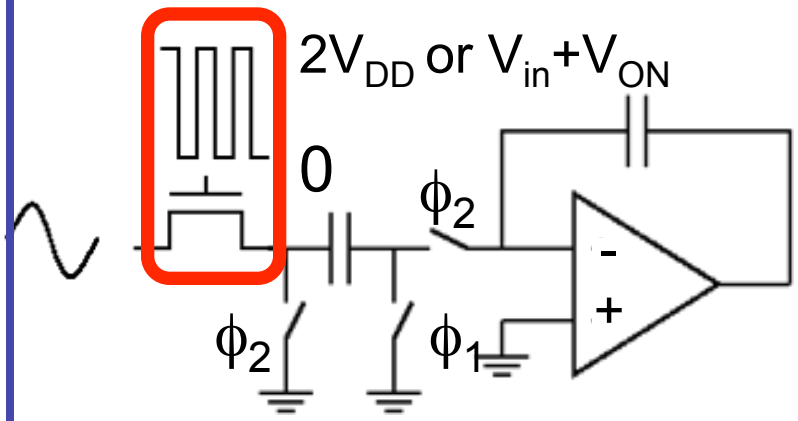


Switched Opamp



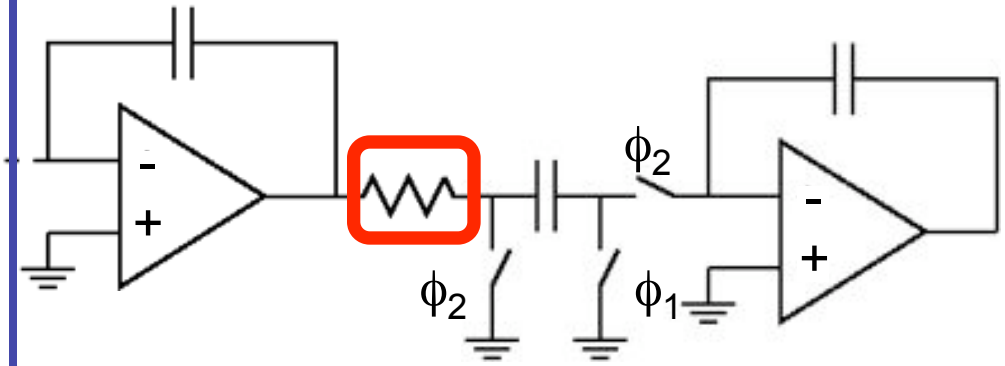
[Crols 1994]

CLK Boost or Bootstrap



[Nakagome 1991][Abo 1999]

Switched R-C



[Ahn 2005]

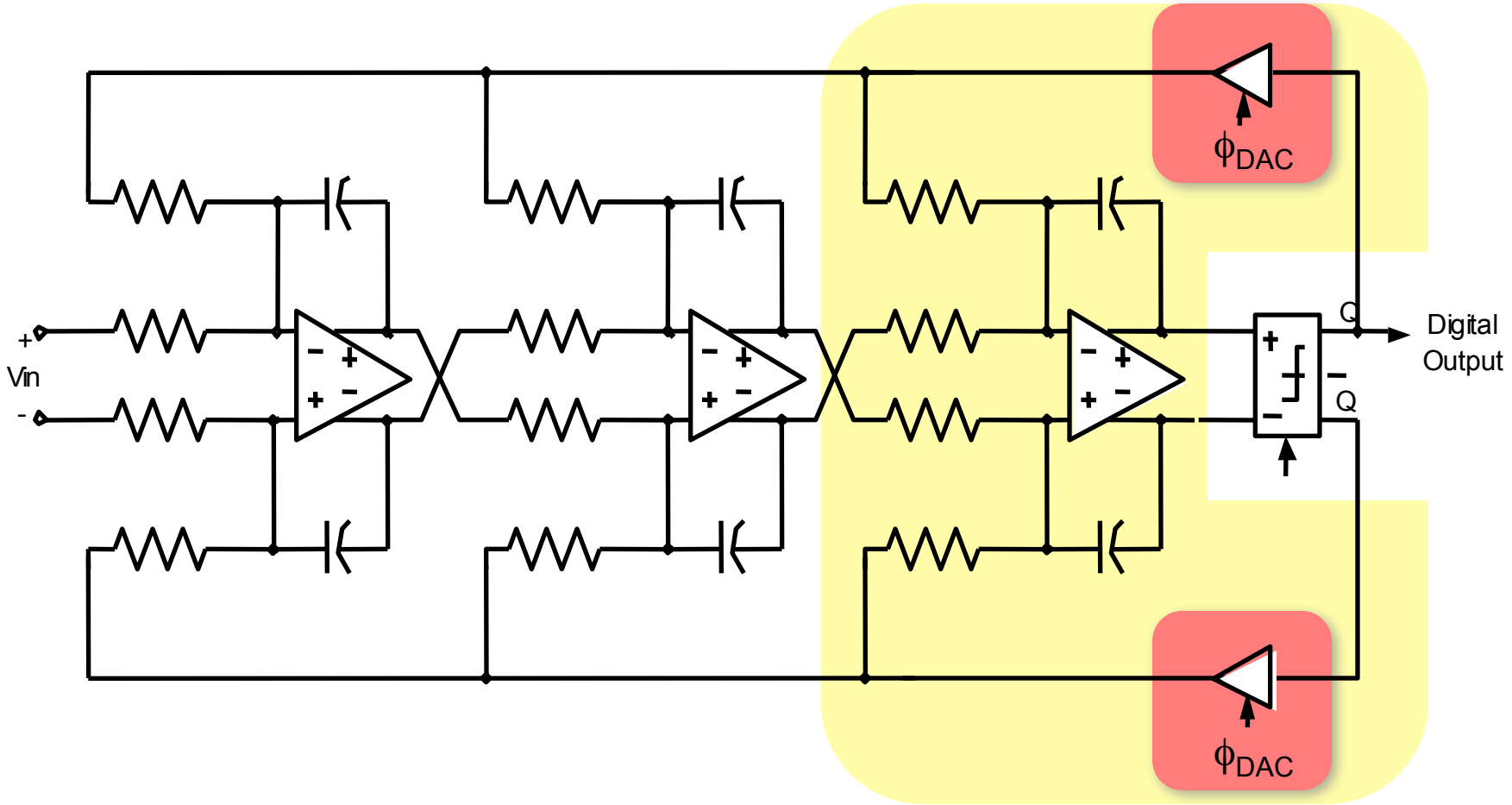
Addressing Floating Switches

- Low V_T switch devices
- Clock boosting or bootstrap
- Switched opamp
- Switched R-C

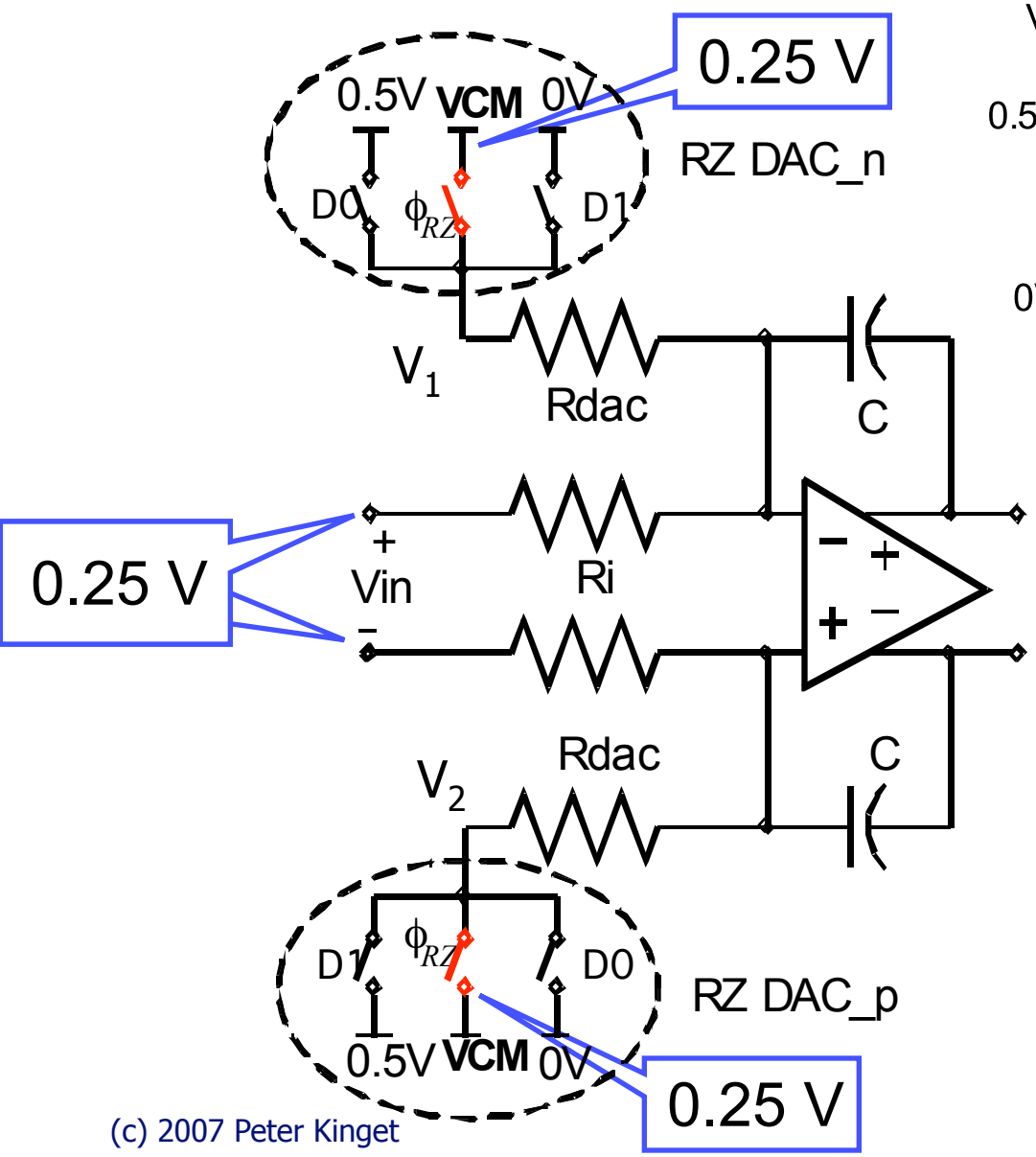
- RTO signaling for CT ΣΔ ADCs
- Cascaded sampling to reduce low-V_{TH} switch leakage
- Common-mode level shift

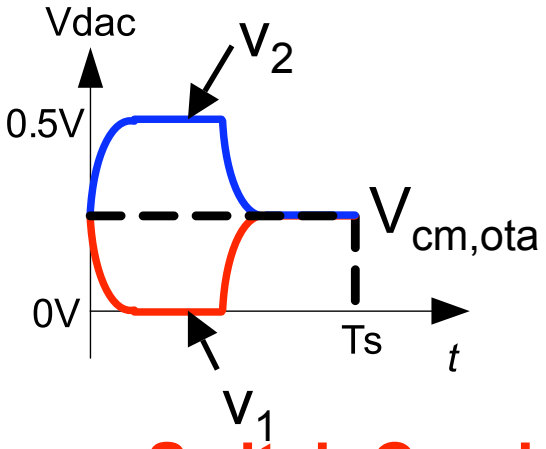
3rd order CT ΣΔ Modulator

Using Active RC integrators

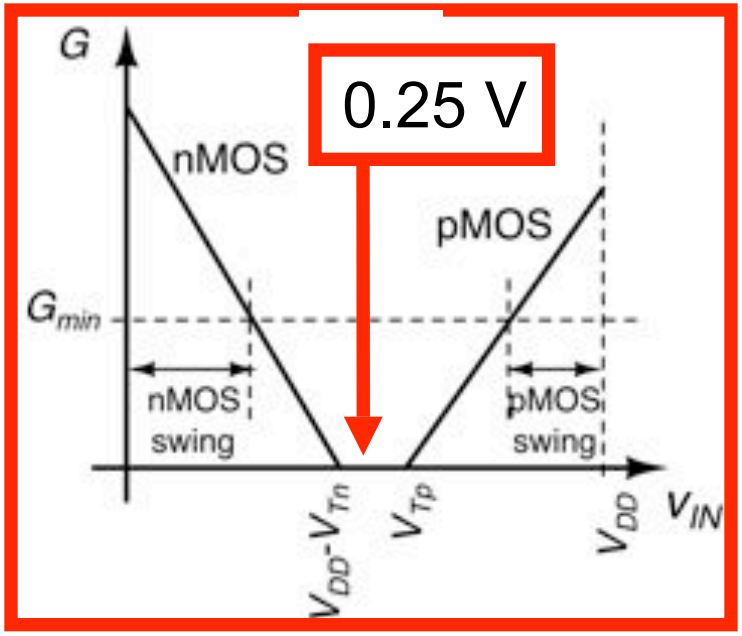


RZ Challenge: Switches at $V_{DD}/2$



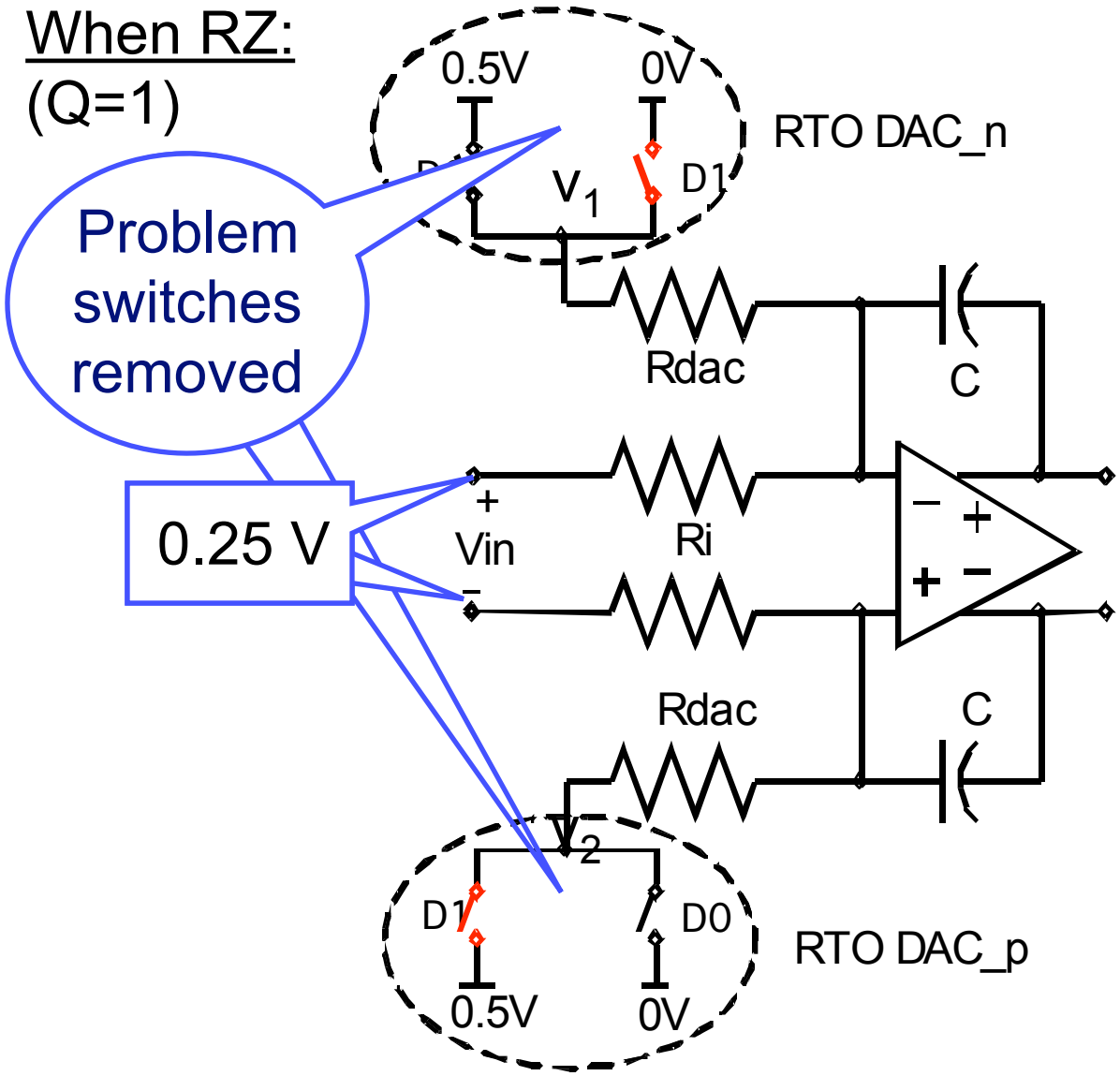


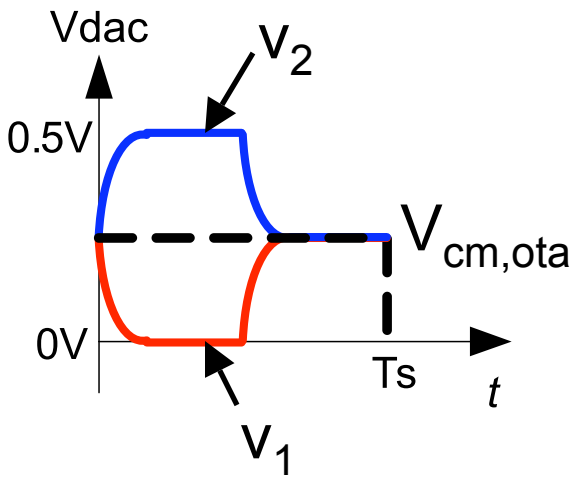
Switch Conductance

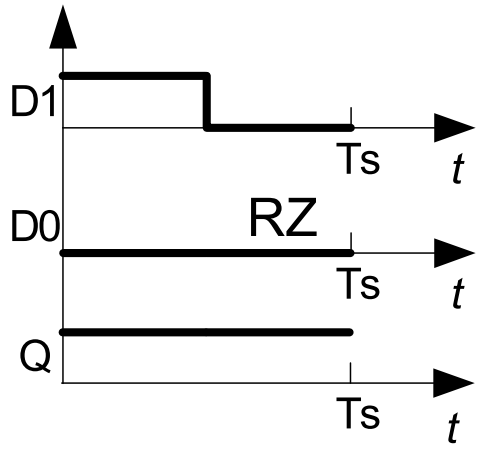


Solution: Return-to-Open

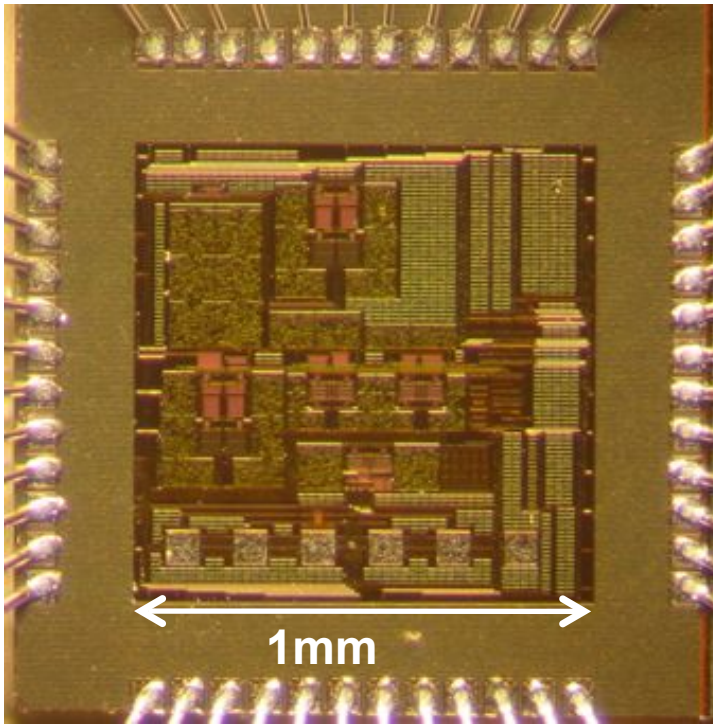
When RZ:
(Q=1)

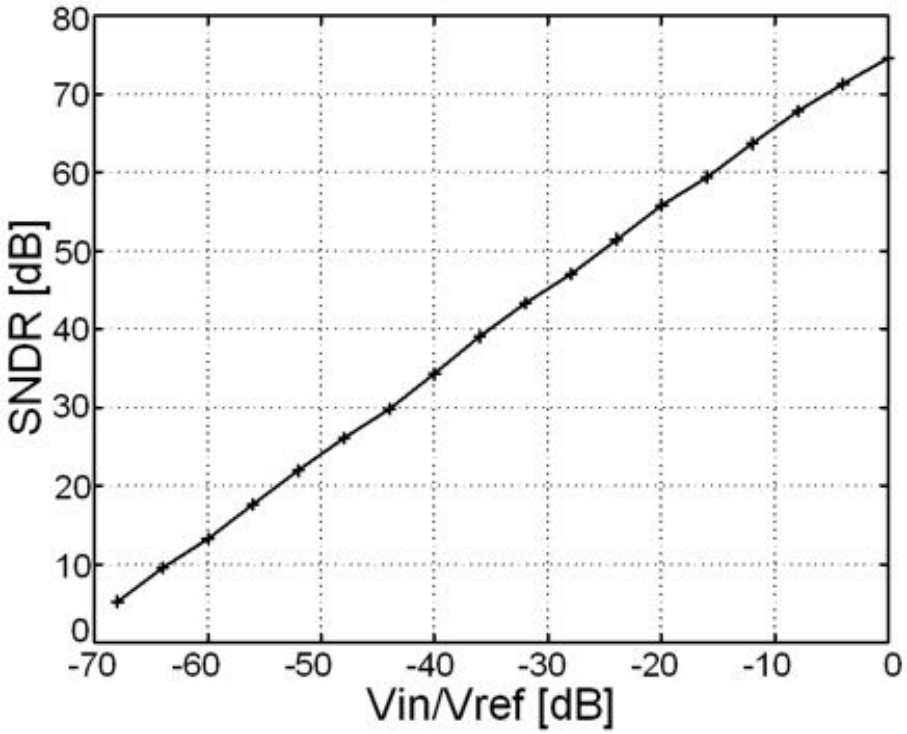






0.5V 74 dB SNDR 25kHz ΣΔ Modulator

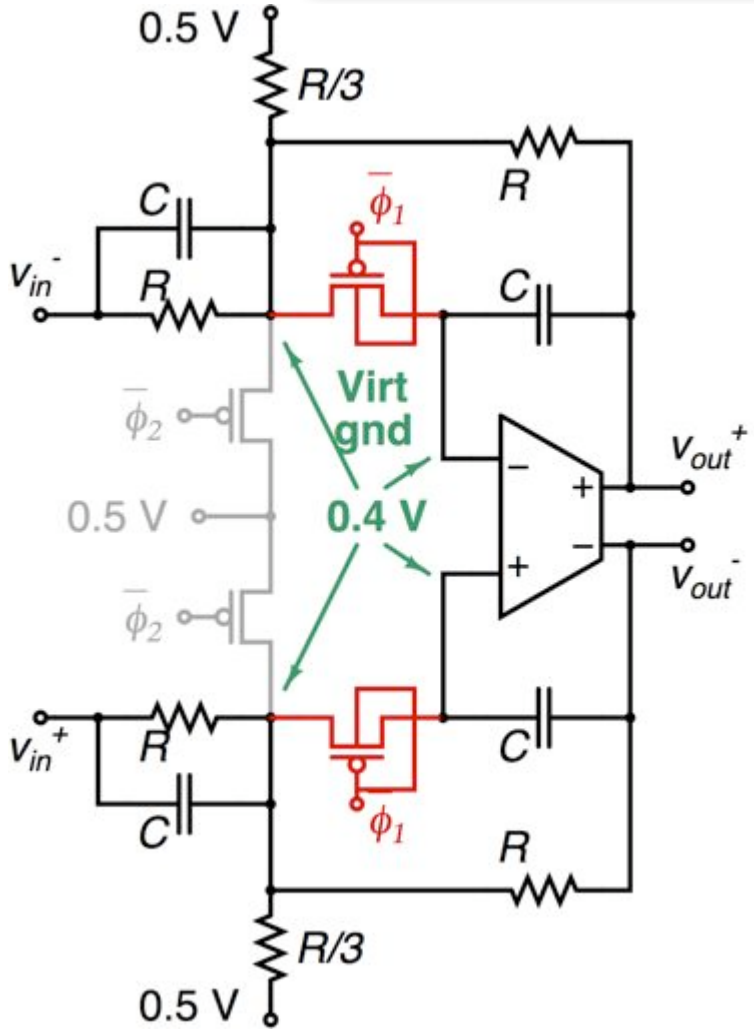




- Operation for V_{DD} = 0.45V to 0.8V
- Return-to-open architecture, body-input gate-clocked circuits
- 74dB SNDR, 25kHz, 64x OSR, 300µW, 0.18um CMOS
- [Pun, Chatterjee, Kinget, ISSCC 06, JSSC 07]

CM Level Shift & Switches

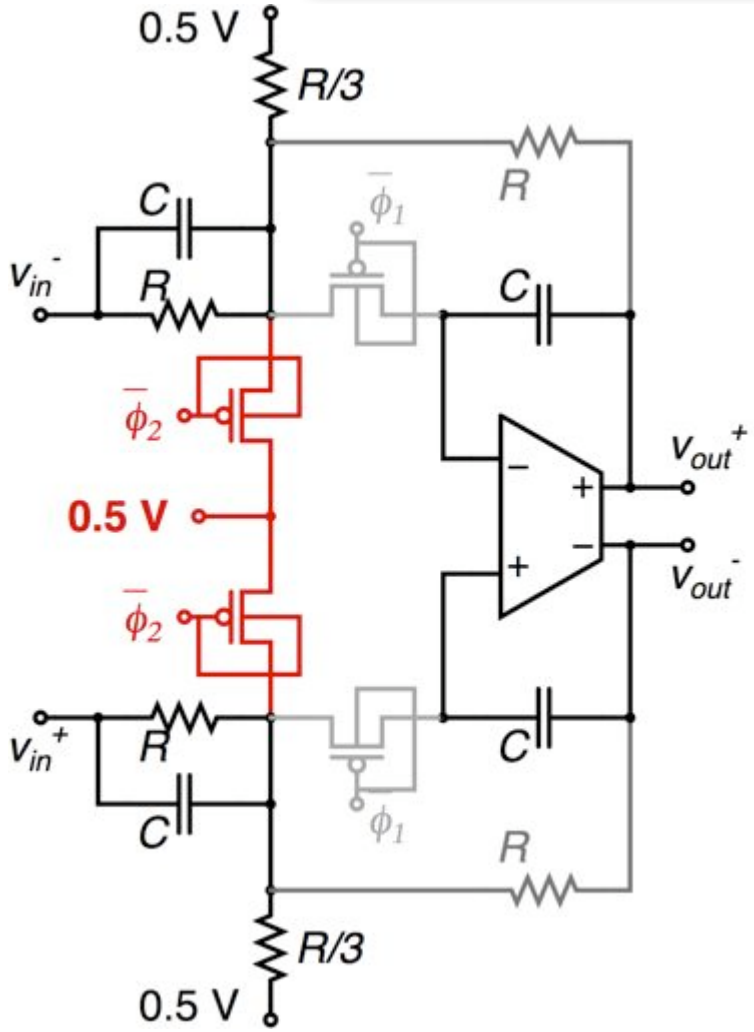
0.5V Differential Track and Hold



- TRACK Phase
- Switch @ 0.4V CM
- Switch @ virtual short no signal swing across
- Switch: clk gate & body!

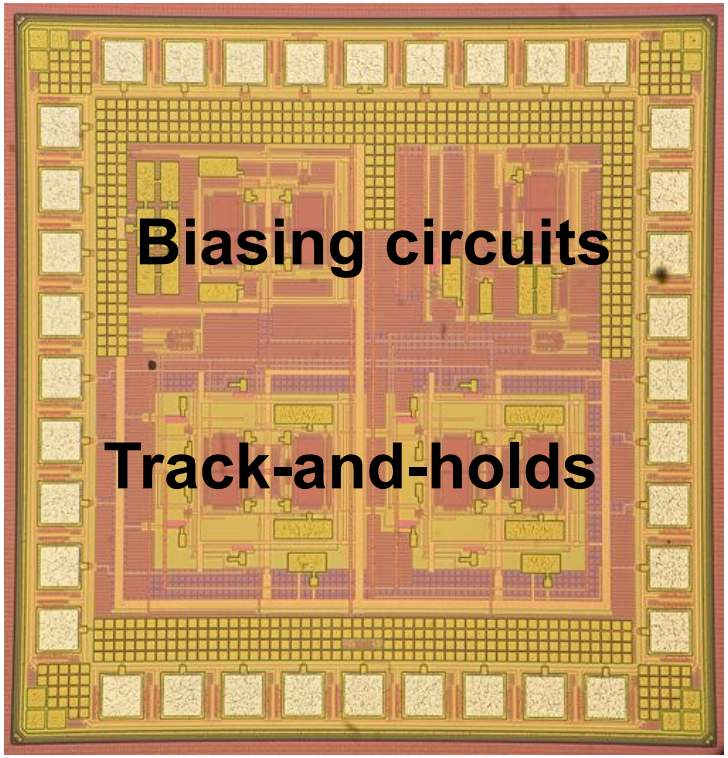
CM Level Shift & Switches

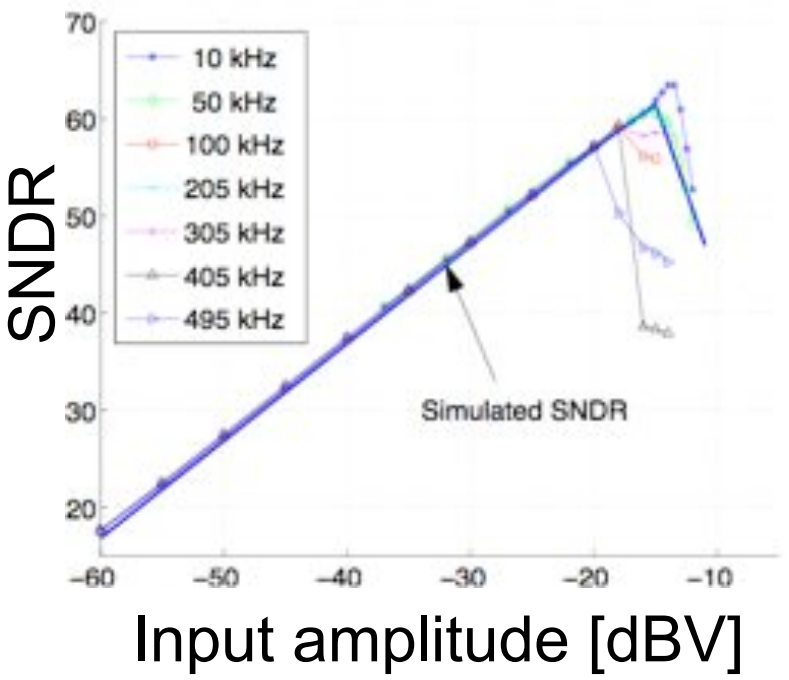
0.5V Differential Track and Hold



- HOLD Phase
- Switch @ 0.4V CM
- Switch: no signal swing across
- Switch: clk gate & body!

0.5V 1Msps 60dB T/H amplifier

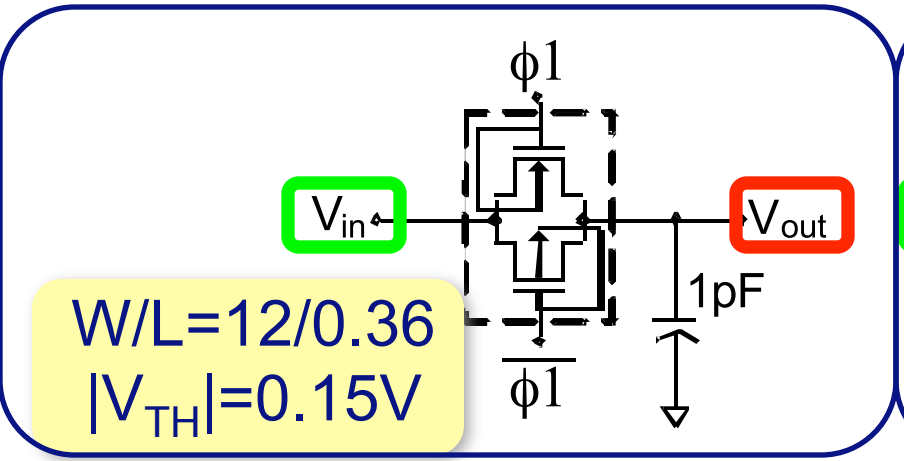


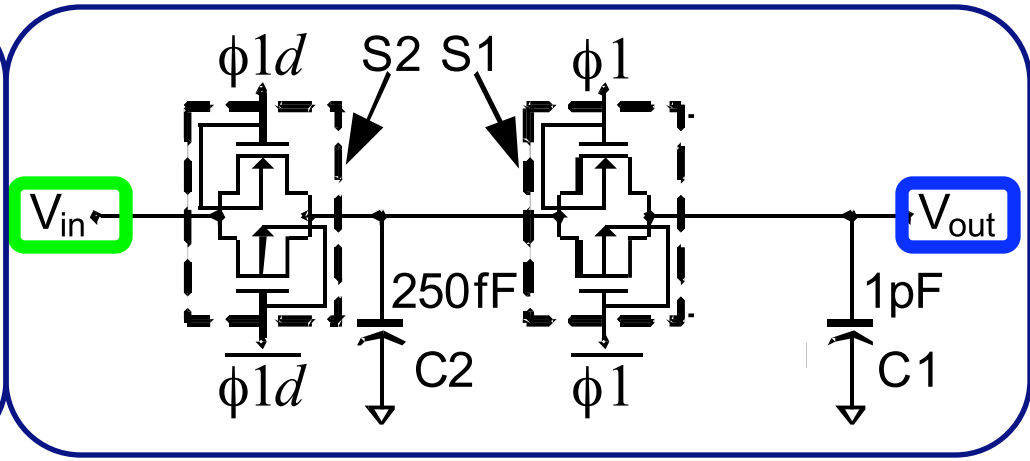


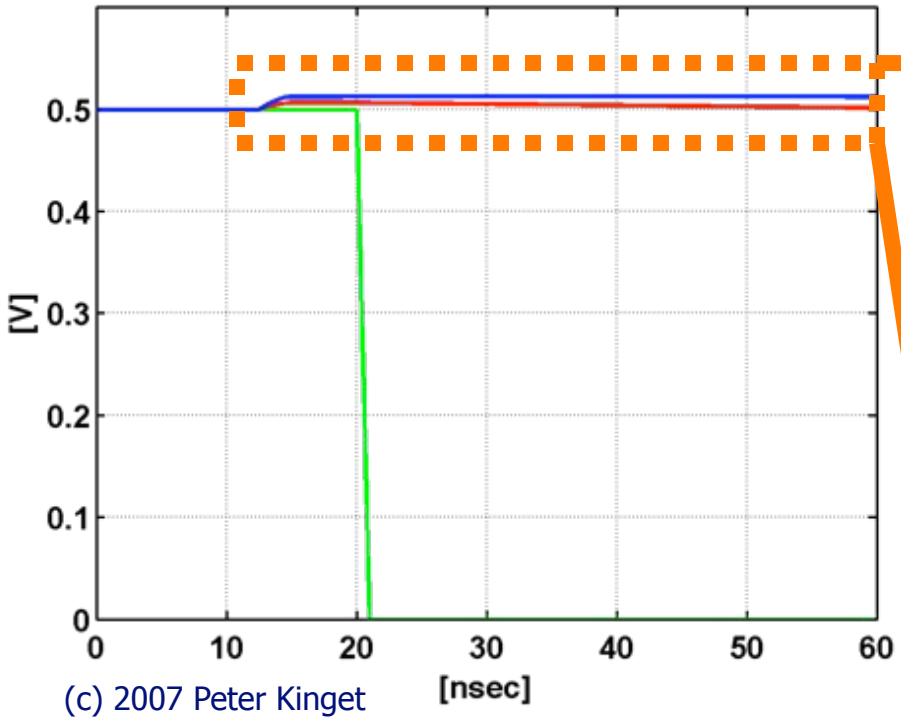
- True low voltage
- No CLK boosting
- [Chatterjee, Kinget, VLSI 06, JSSC07]

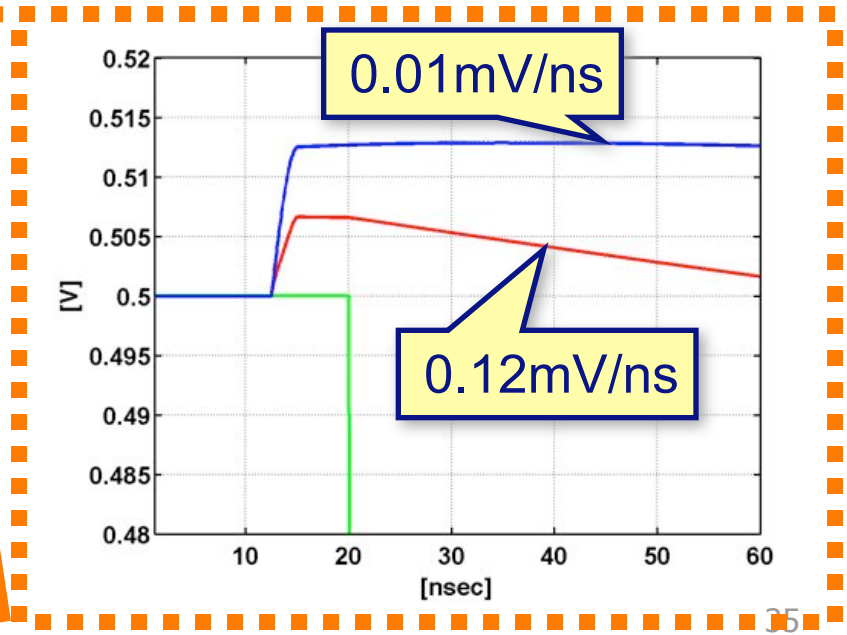
- 0.25µm CMOS
- $|V_{TH}|$= 0.6V
- 60dB SNDR
- 1Msps
- 0.6mA at 0.5V

'Low V_{TH}' switch leakage:

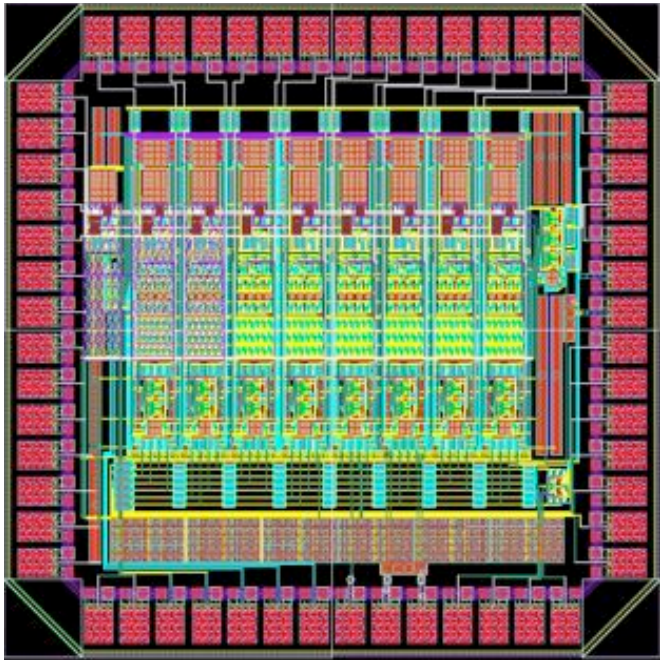


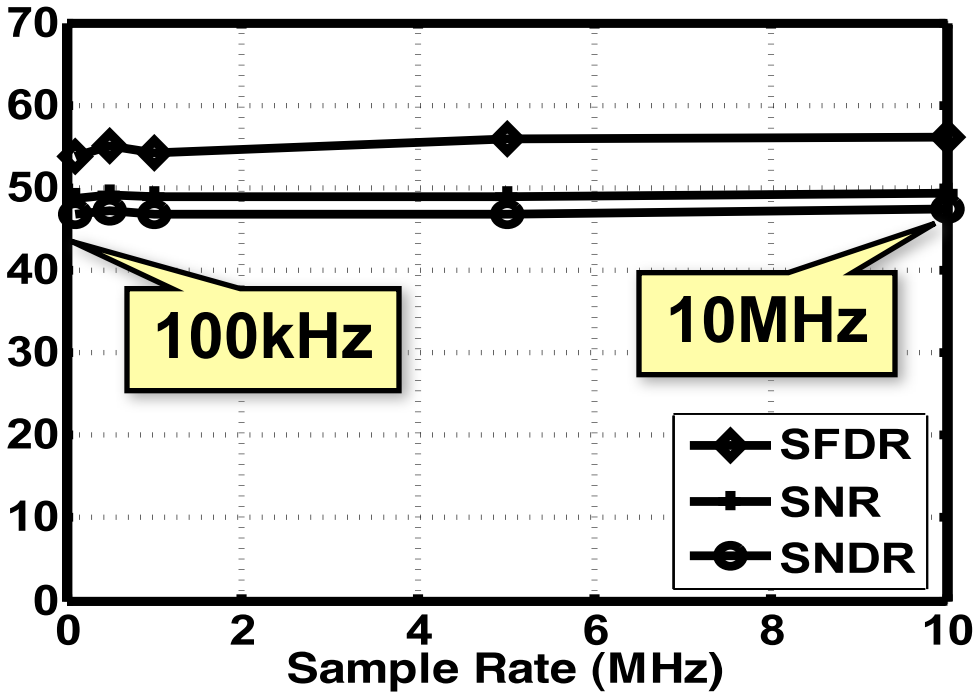






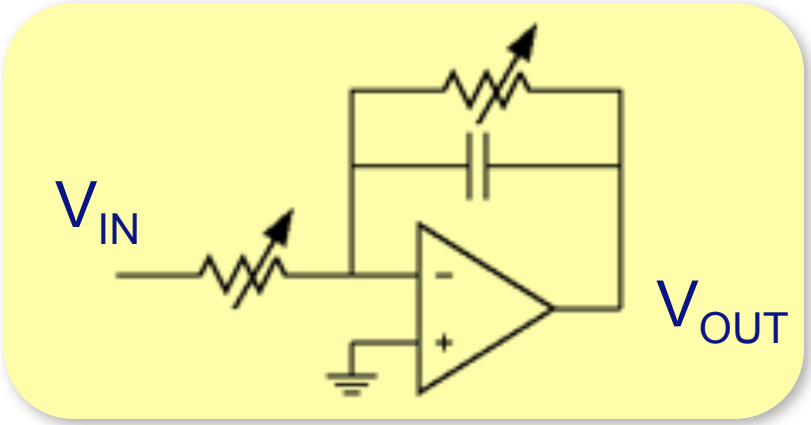
0.5V 8bit 10Msps Pipelined ADC





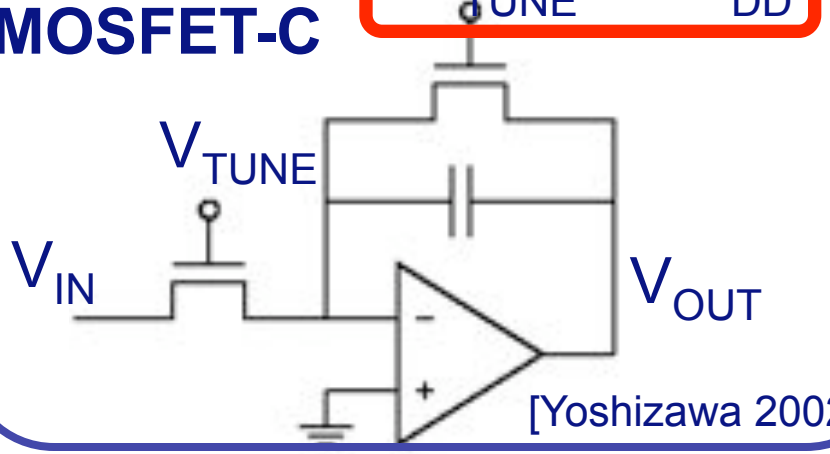
- No internal voltage or clock boosting; regular devices; cascaded sampling technique.
- Aux. S/H for the sub-ADC to eliminate front-end SHA.
- 10Msps: SNDR 48dB@101kHz, 43.3dB@4.9MHz.
- 2.4mW in 90nm CMOS [Shen, Kinget, VLSI07].

Tuneable Lossy RC Integrator



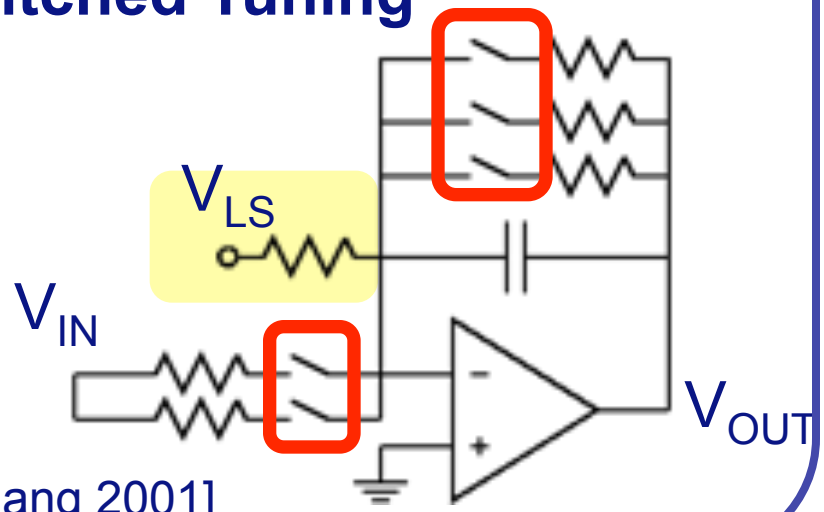
MOSFET-C

$V_{TUNE} >> V_{DD}$



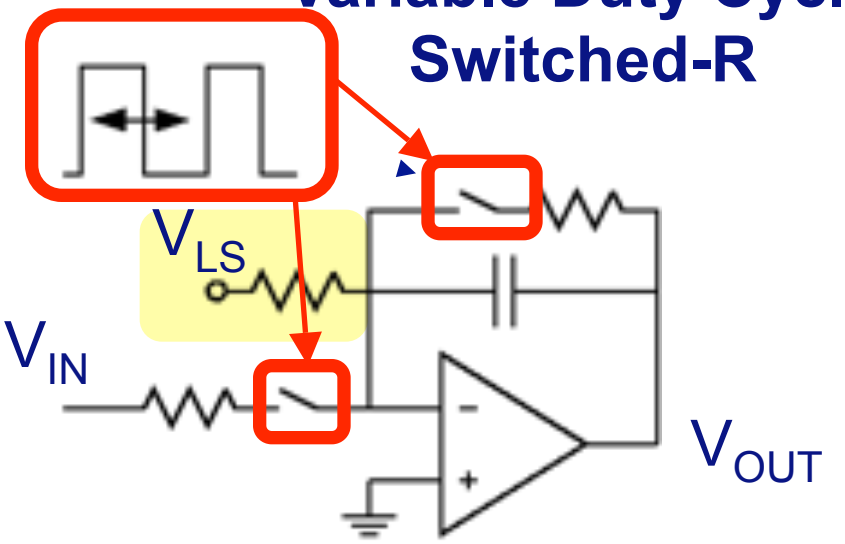
[Yoshizawa 2002]

CM Level Shift Switched Tuning



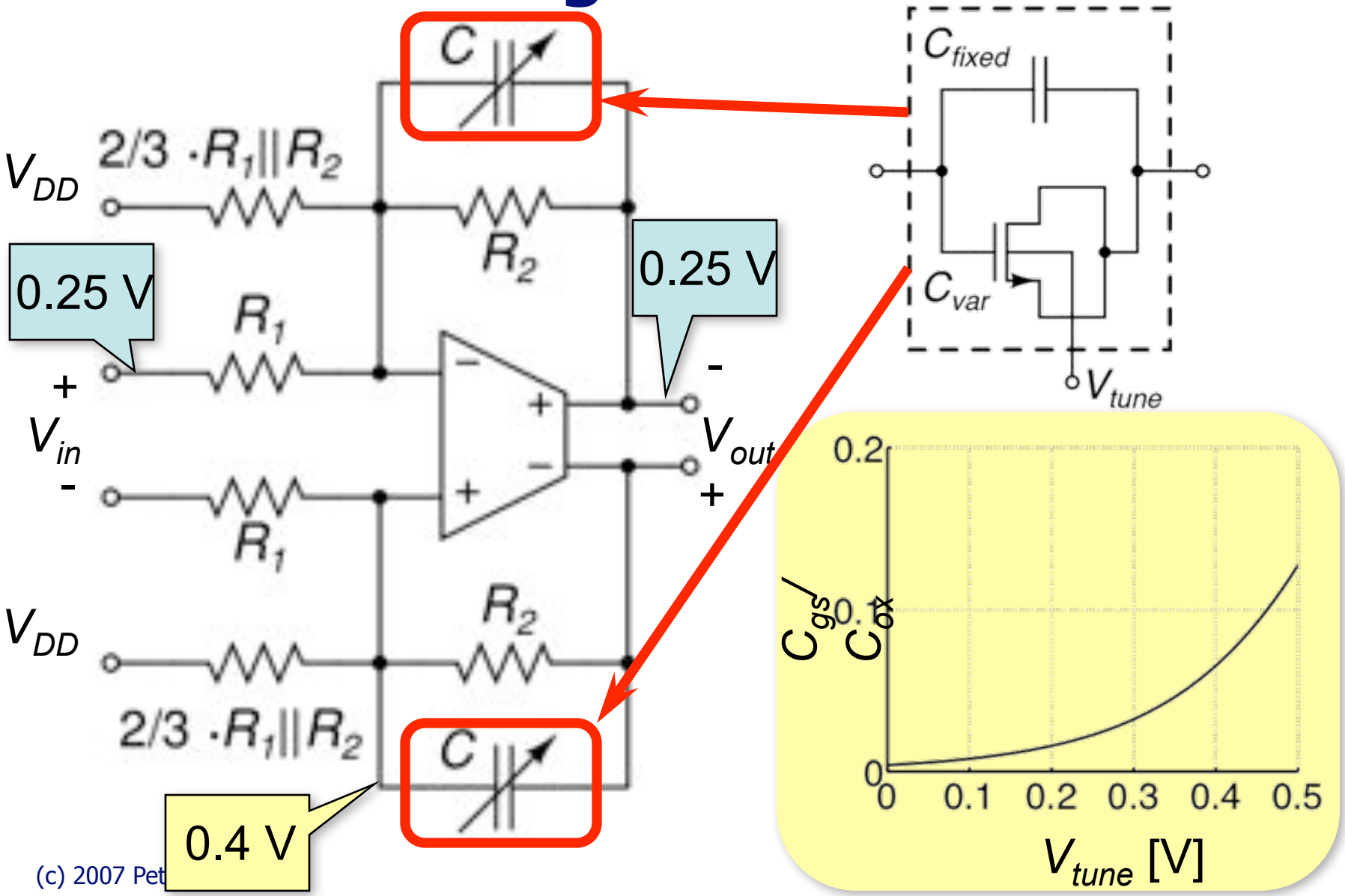
[Huang 2001]

Variable Duty Cycle Switched-R

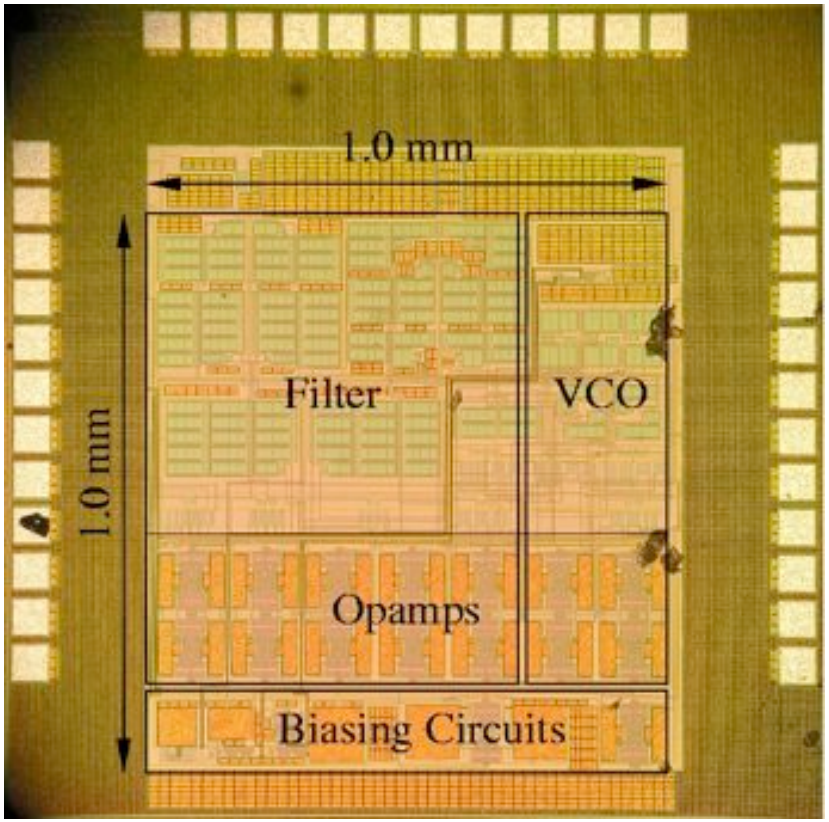


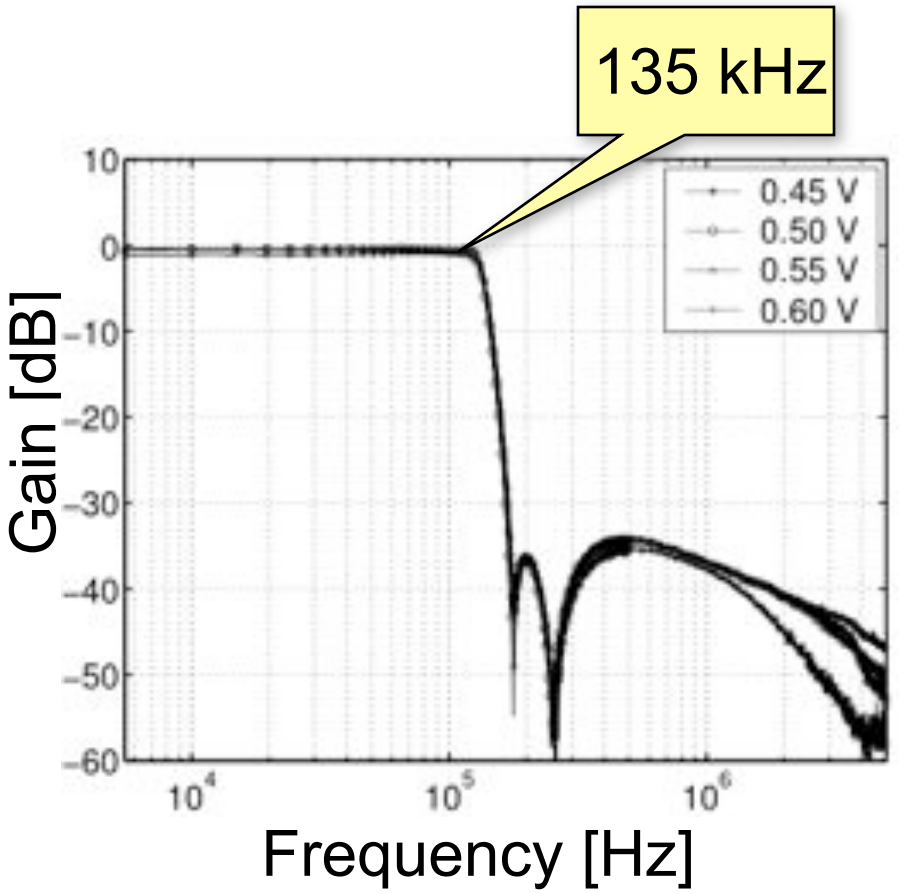
[Kurahashi 2006]

Low-voltage tunable integrator using varactor



0.5V Fully Integrated 5th Order LPF

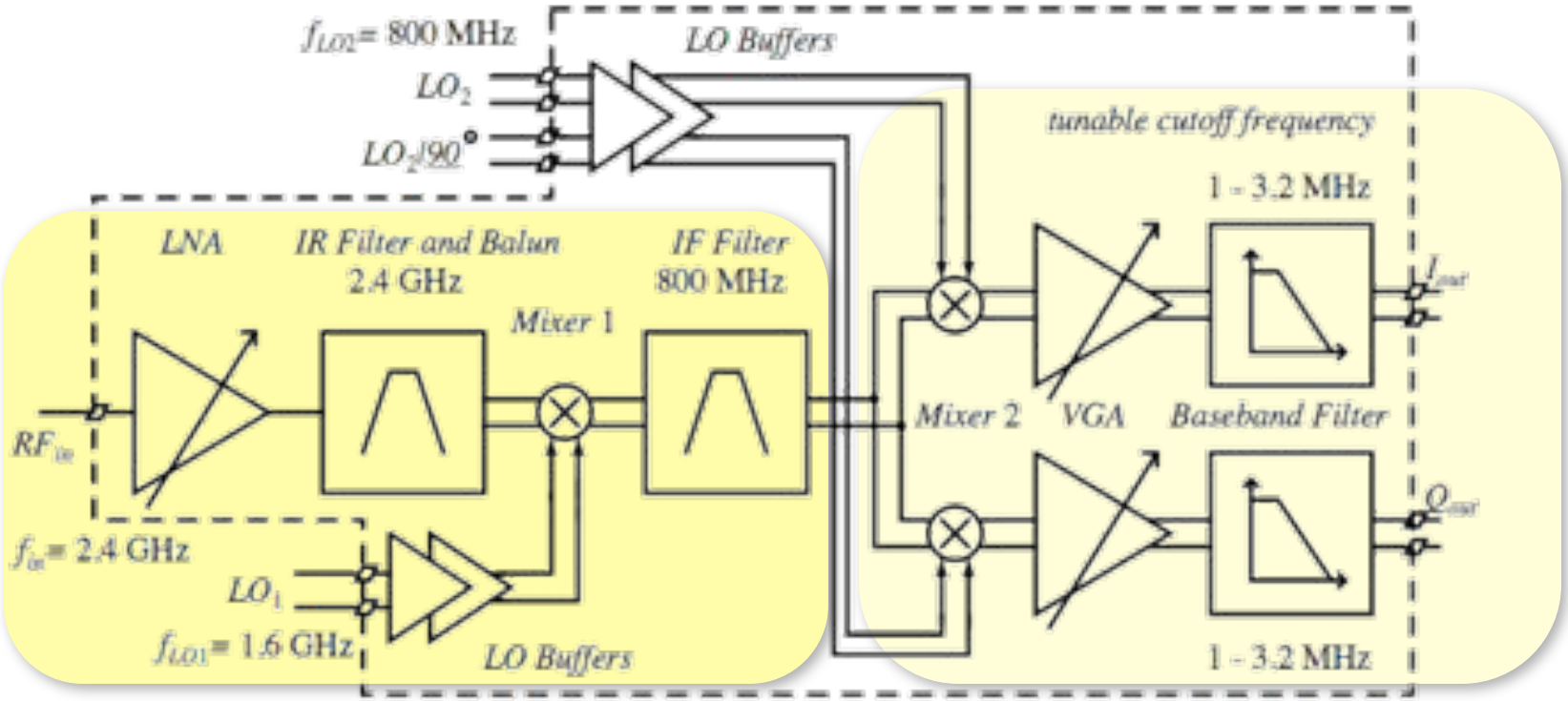




- Operation at 0.45 V to 0.6 V
- 1.1 mW power dissipation
- 57 dB dynamic range

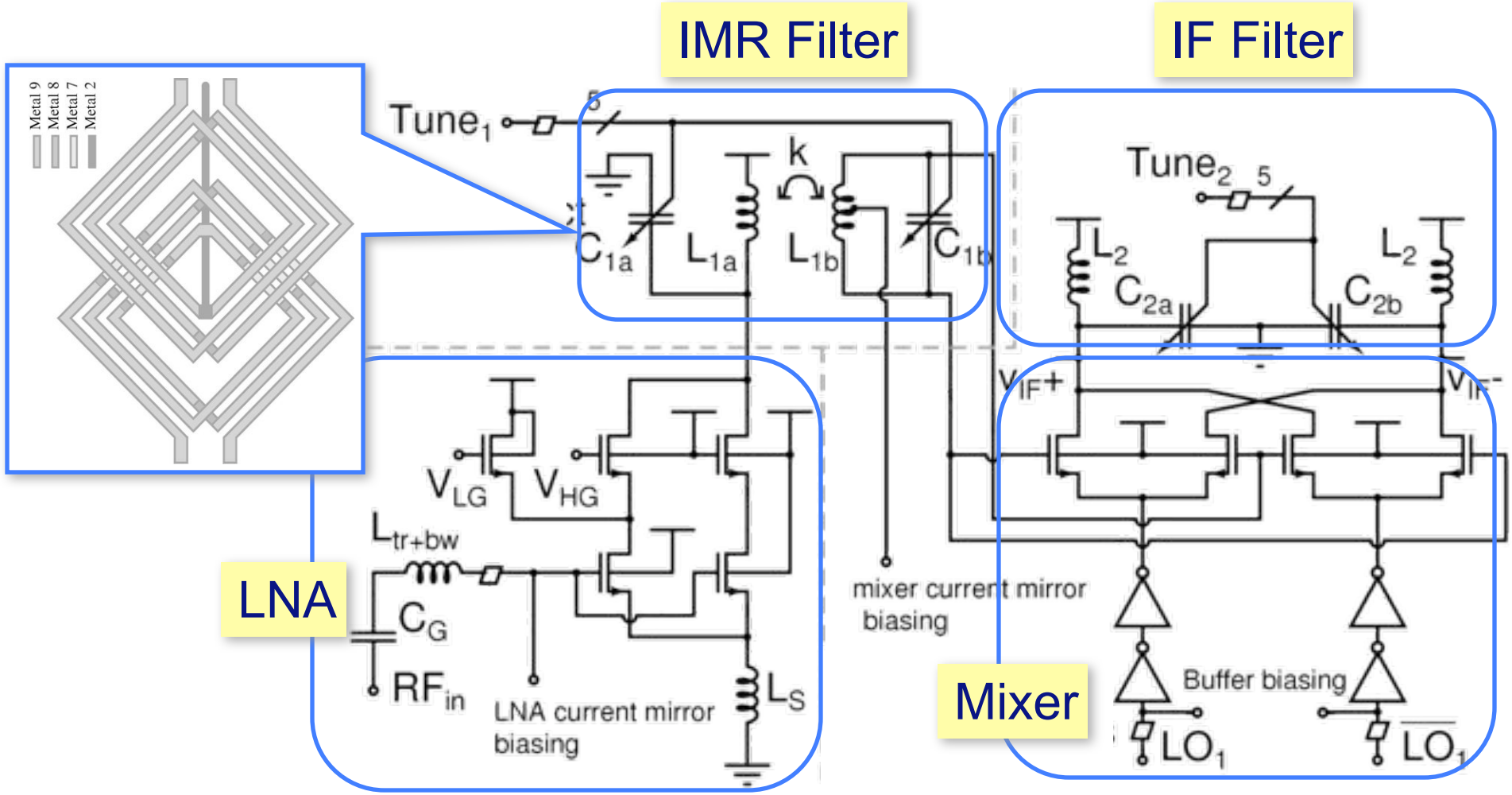
[Chatterjee, Tsividis, Kinget, ISSCC05, JSSC05]

A 0.5V 2.4GHz Receiver



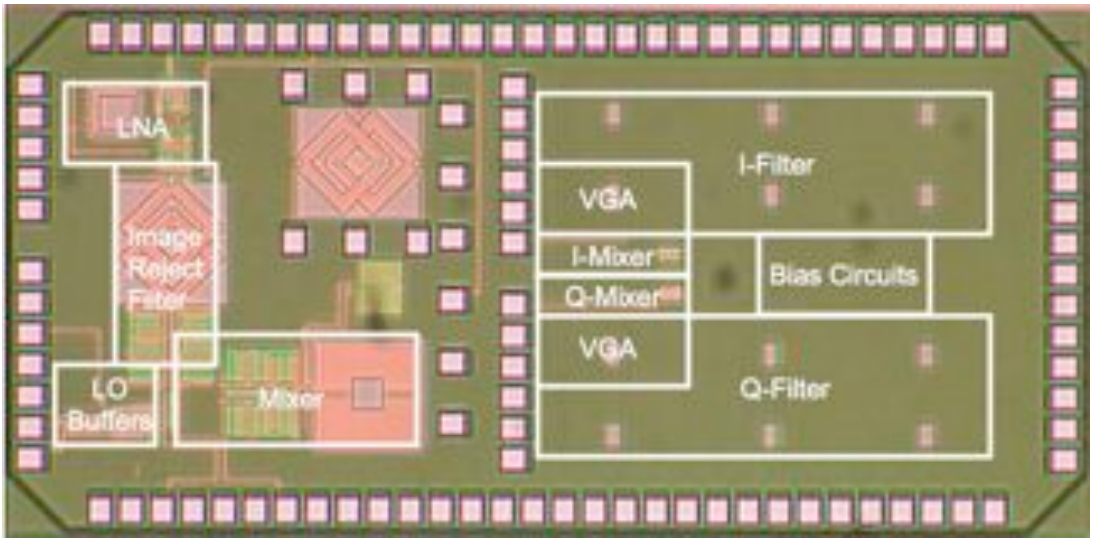
- ISM band applications
- Sliding IF topology: only 1 RF Mixer
- LNA, Mixers, VGA + on chip RF, IF & BB filtering

LNA, IMR, & RF Mix



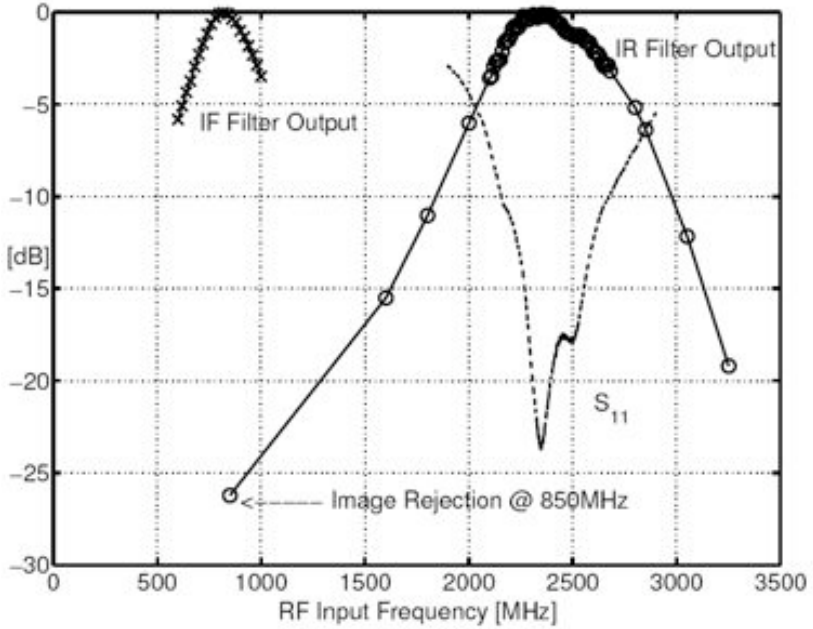
Switched Gm Mixer [Klumperink 2004]

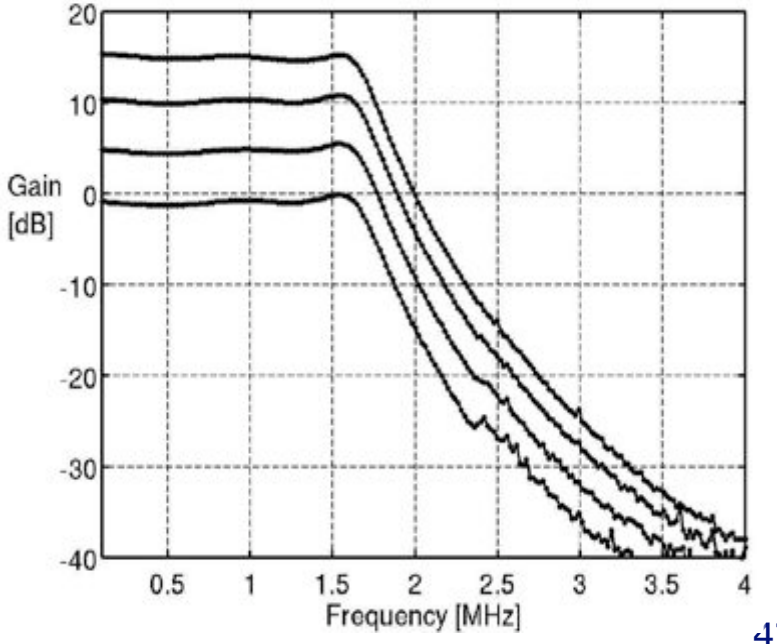
A 0.5V 2.4GHz Receiver



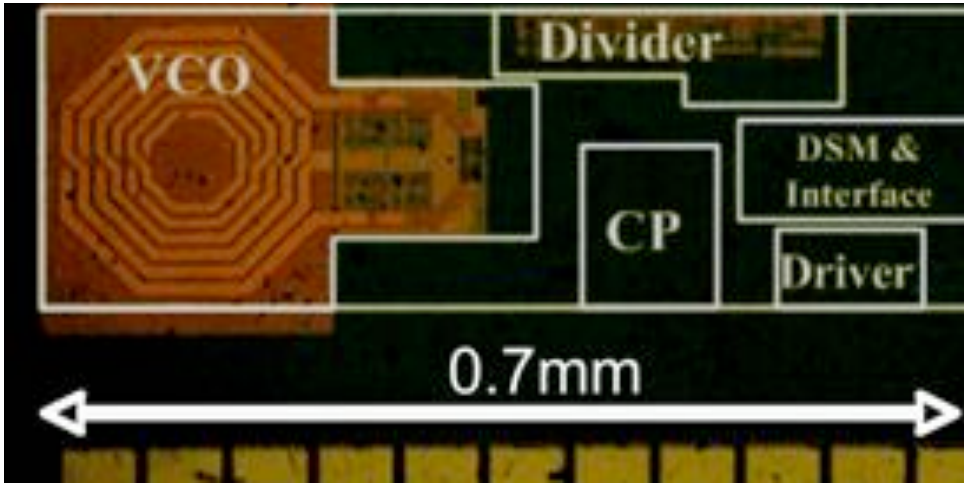
- Gain 30dB; NF 18dB; IIP3 -22dBm
- 90nm CMOS
- 8.5mW

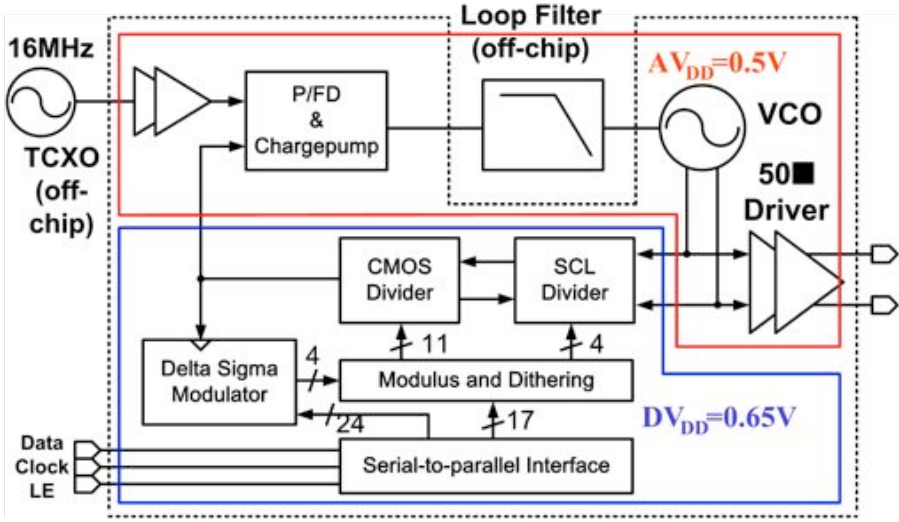
[Stanic, Balankutty, Kinget, Tsividis, RFIC07]





0.65V/0.5V 2.4-2.6GHz Fractional-N Synthesizer in 90nm CMOS





- VCO swing within the supply rails for reliability.
- Fractional-N DSM dithering shifted to later divider stages to *prevent noise injection into forward biased body*.
- Staggered clock to prevent jittering caused by simultaneous switching.
- ISM Band applications: -120dBc/Hz @ 3MHz for 6mW

[Yu, Kinget, ISSC07]

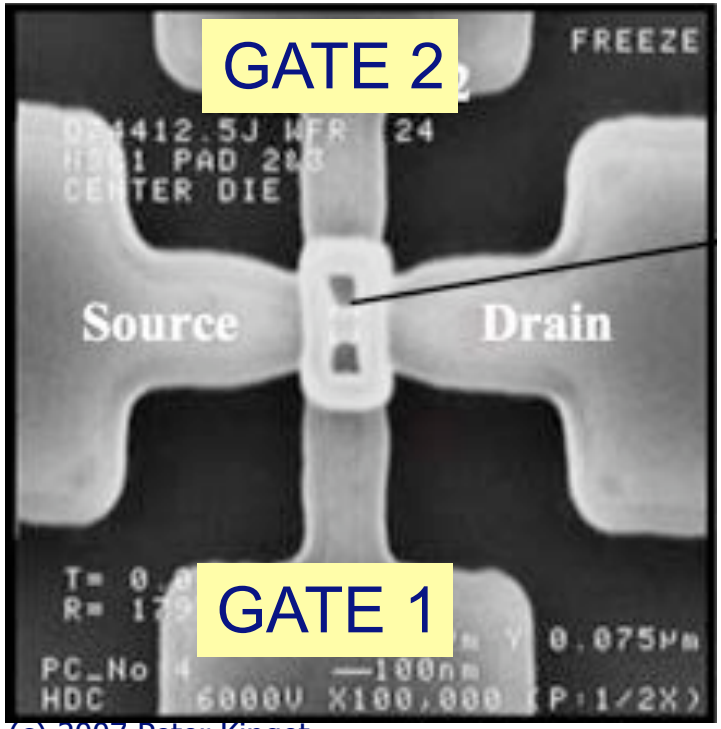
Outlook

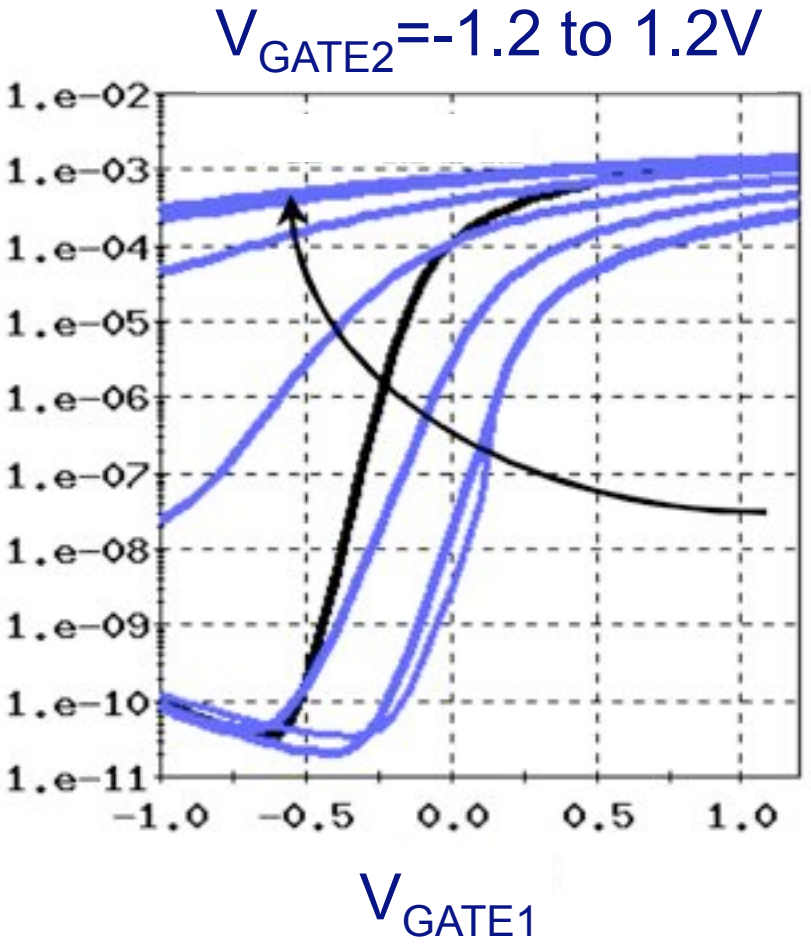
Where do we go from here…

- Other nanoscale challenges:
  - Smaller g_m/g_o.
  - Gate & subthreshold leakage.
  - Reduced body effect: $g_{m,b}$ ↓ for L ↓.
- Opportunities:
  - Device speed significantly improves.
  - Calibrate using abundant digital gates.
  - FinFETs, dual gate devices, ….

Nanoscale Opportunities

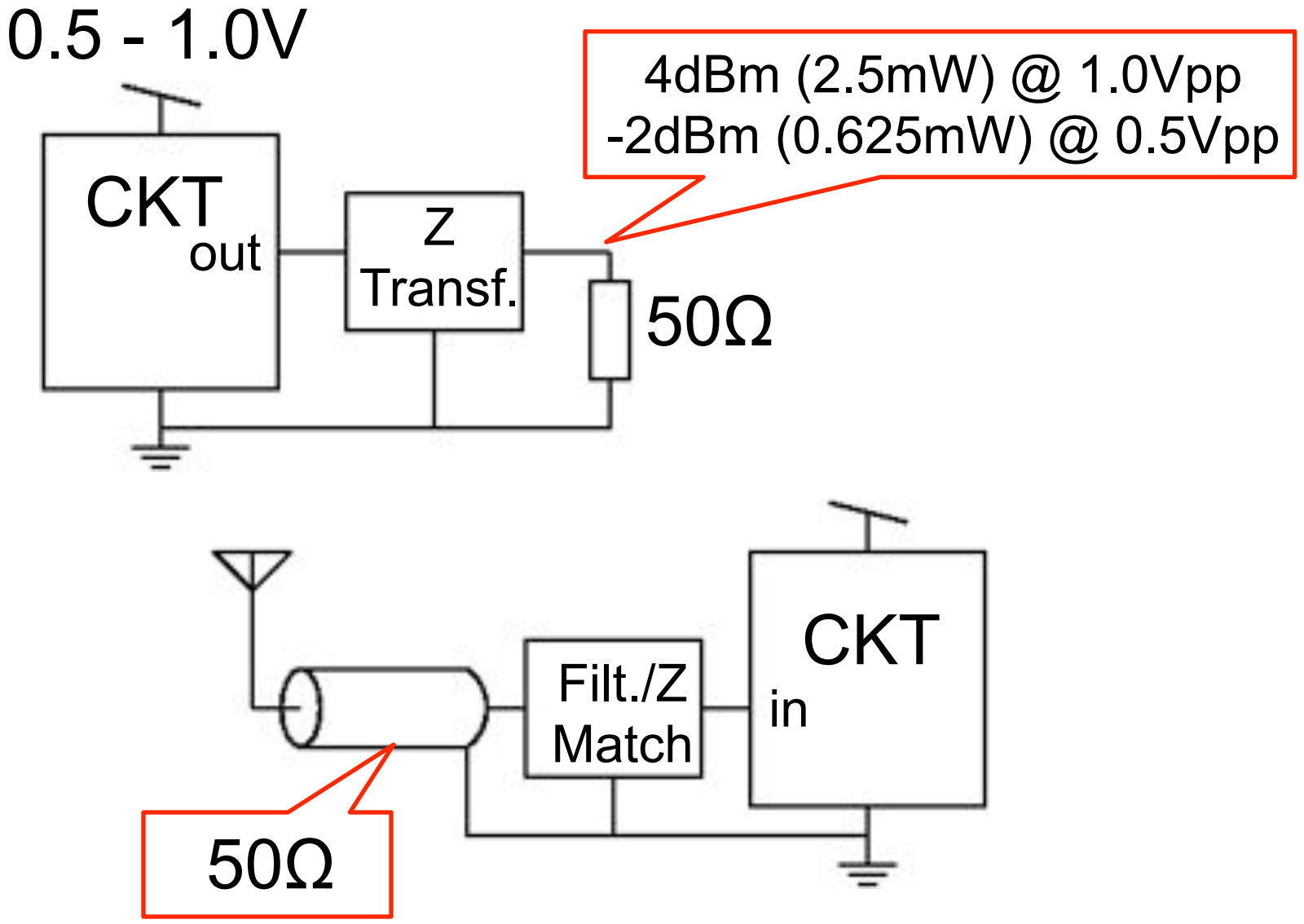
- FinFETs,
- dual gate devices, ….



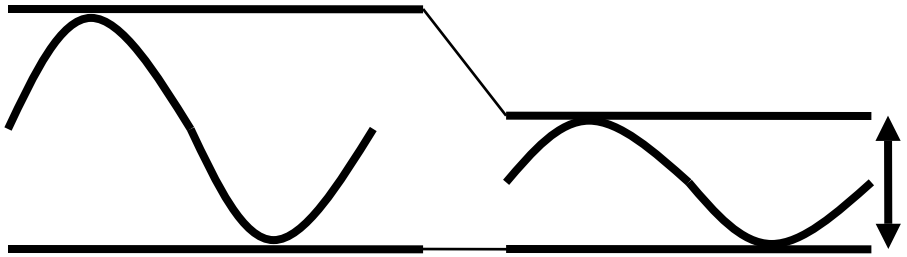


[Mathew 2005]

LV Challenge: Interfaces



Power Dissipation Limits



$$V_{DD} = 2\sqrt{2}\,V_{RMS}$$

- Noise limited circuits [Vittoz90]:

$$SNR = \frac{V_{RMS}}{\sqrt{v^2_{n,RMS}}} \qquad \overline{v^2_{n,RMS}} = \frac{kT}{C} \qquad I_{DC} = 2f\,C\sqrt{2}V_{RMS}$$

$$P \geq 8\,kT\,f\,SNR^2$$

ideal class B

- Mismatch limited circuits [Kinget96]:

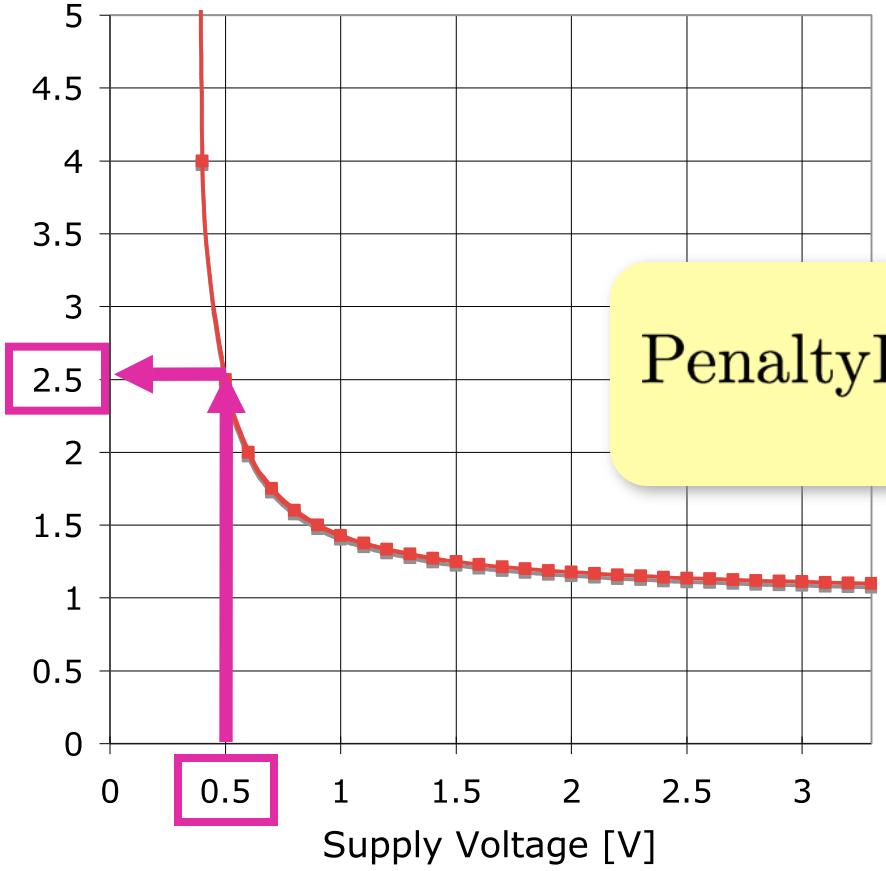
$$Acc = \frac{V_{RMS}}{3\sigma(V_{os})} \qquad \sigma^2(V_{os}) = \frac{C_{ox}A^2_{VT}}{C} \qquad I_{DC} = 2f\,C\sqrt{2}V_{RMS}$$

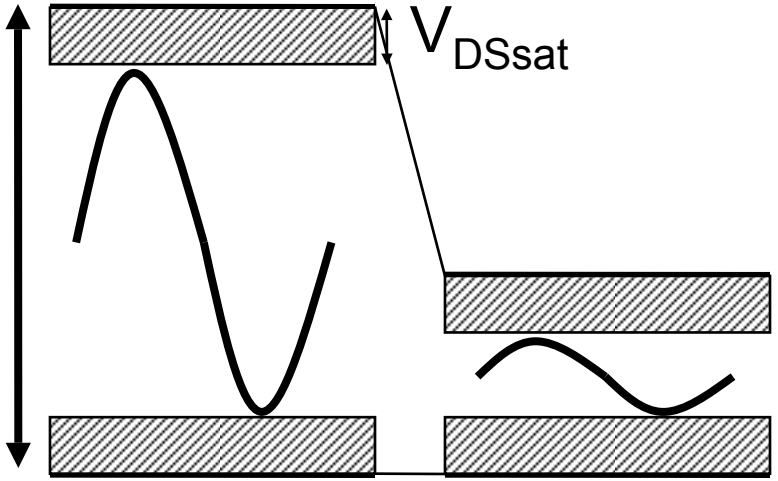
$$P \geq 24\,C_{ox}\,A^2_{VT}\,f\,Acc^2$$

Low Voltage Power Penalty

- Finite V_{DSsat}:

$$V_{DD} = 2\sqrt{2}\,V_{RMS} + 2V_{DSsat}$$

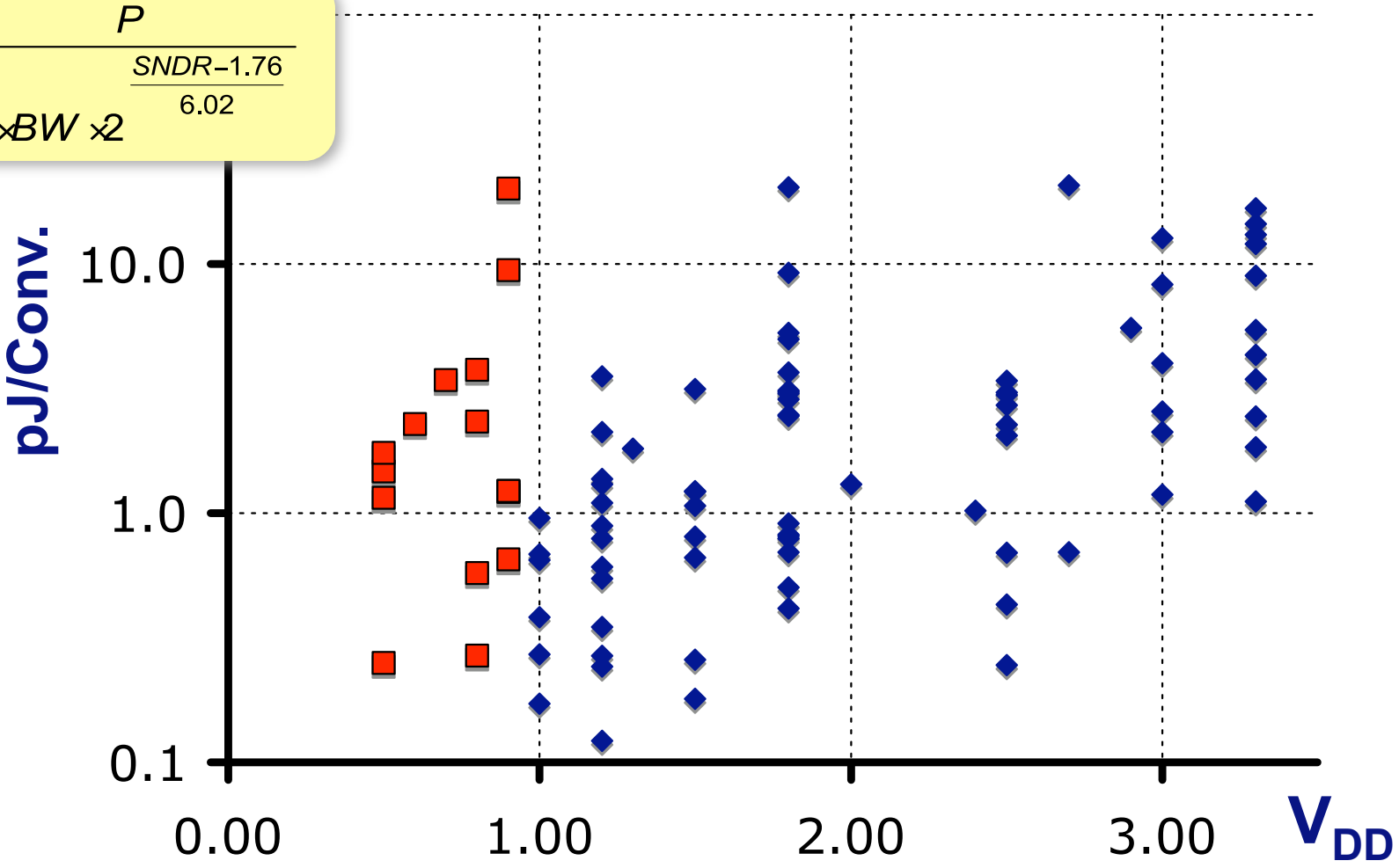




$$\text{PenaltyFactor} = 1 + \frac{2V_{DS,sat}}{V_{DD} - 2V_{DS,sat}}$$

ADC FOM vs V_{DD}

$$\text{FOM} = \frac{P}{2 \times BW \times 2^{\frac{SNDR - 1.76}{6.02}}}$$



Most data taken from B. Murmann,
"A/D Converter ISSCC Performance Data"

Ultra-low Voltage Analog & RF Design Techniques

- Exploit full device characteristics
  - RSCE, Body-bias
- Rethink your topologies
  - Eliminate stacks, LCMFB, CMFF, Neg. G
- Revise your architectures
  - Eliminate switches, address leakage, revise tuning paradigms

Plenty of open opportunities!!

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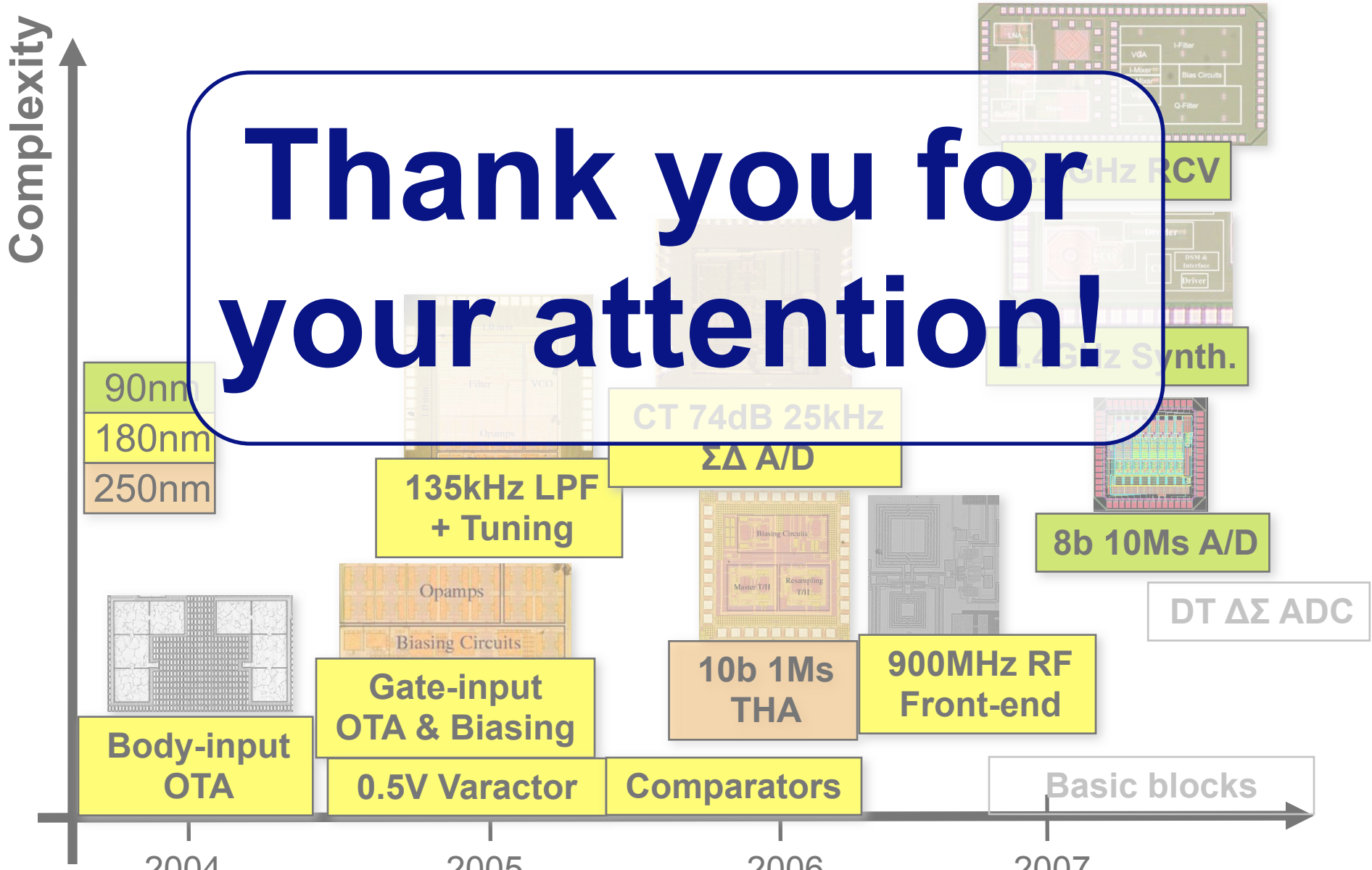
- Europractice, Philips (now NXP) and UMC for fabrication support.
- Integrand Software for EMX software.

0.5V Analog Roadmap



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