Designing Analog and RF Circuits for Ultra-low Supply Voltages

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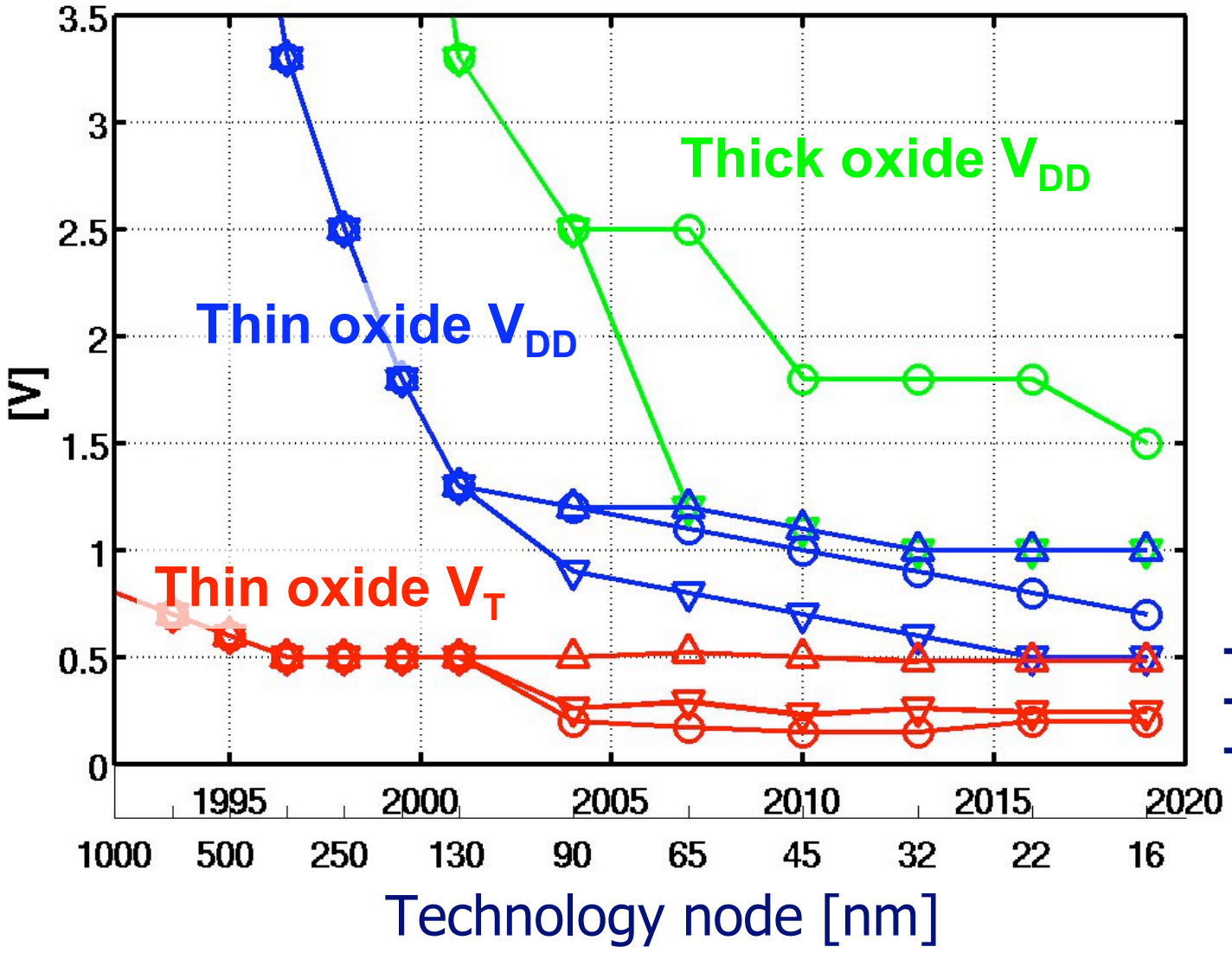
Nano CMOS : Supply Voltage



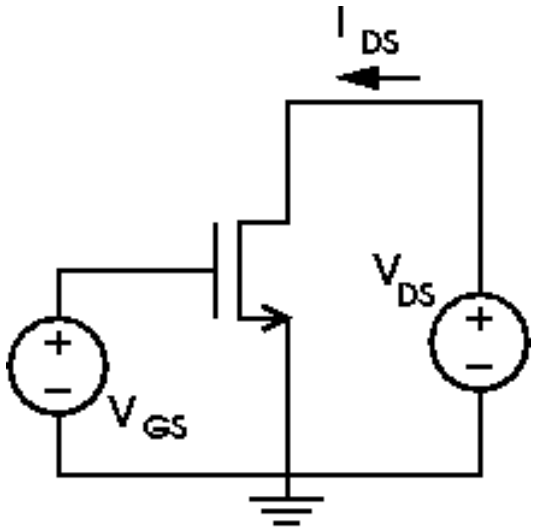
[ITRS'05]

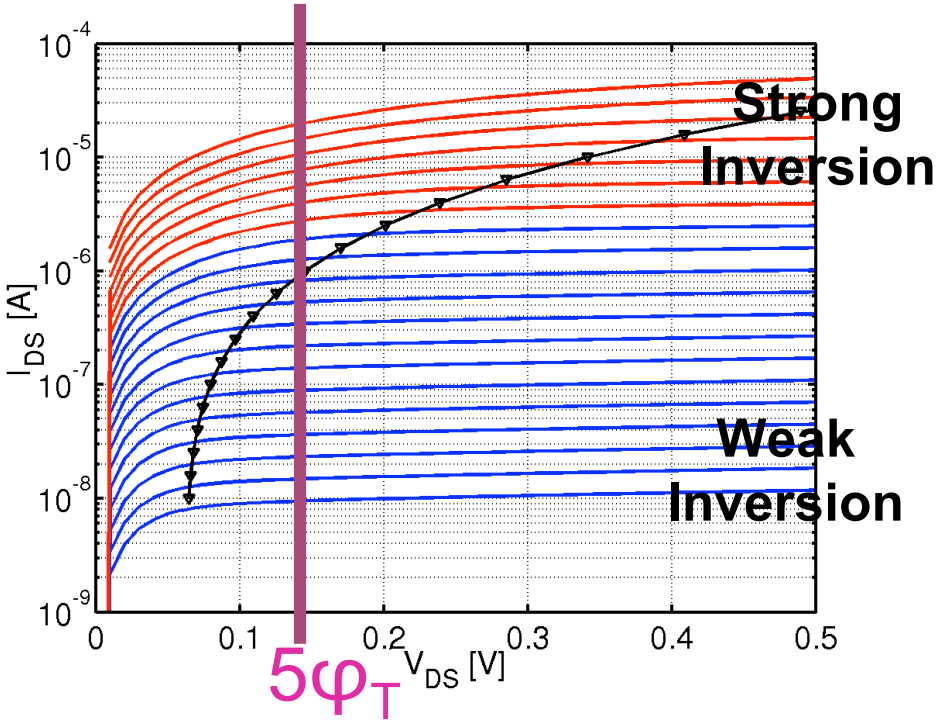
–O– High Perf.
–Δ– Low Standby
–V– Low Power

Ultra-low Voltage Analog/RF

- What analog/RF is possible in core nanoscale digital?
- Scavenging applications
  - E.g., single solar cell V_{DD} 0.4-0.5V
- Ultra-low energy digital systems
  - Optimal DV_{DD} is 0.3-0.5V
  - Analog support functions for digital
- SOC designs
  - Analog/RF powered from on-chip LDO
  - AV_{DD} is 0.2V below DV_{DD}
- Interesting research…
  - Explore boundaries, develop design techniques

MOST Biasing: CS or VCCS

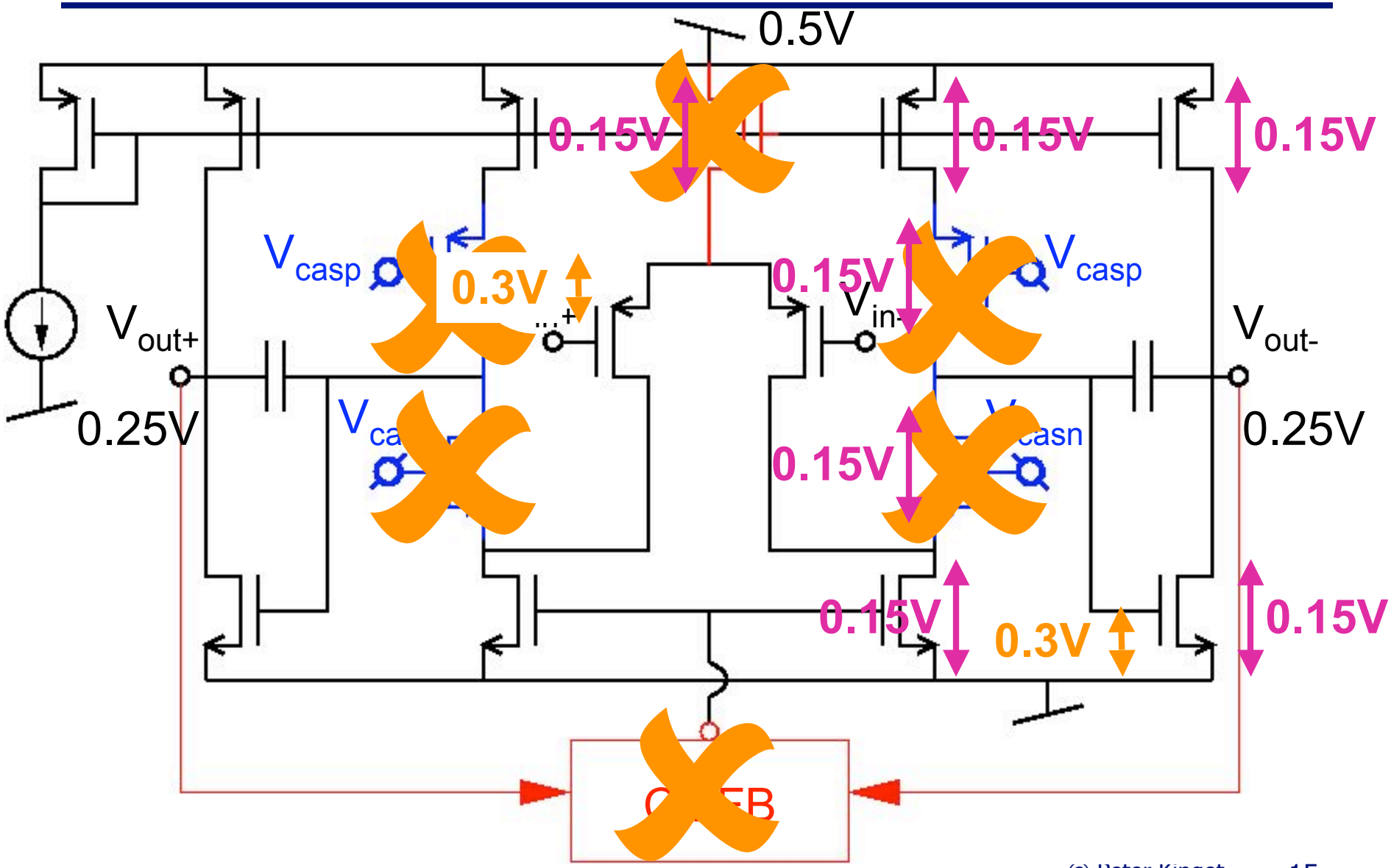




- Transconductor or Current Source
  V_{DS} > 0.15 V (for V_{GS}-V_T ≤ 0.2 V)

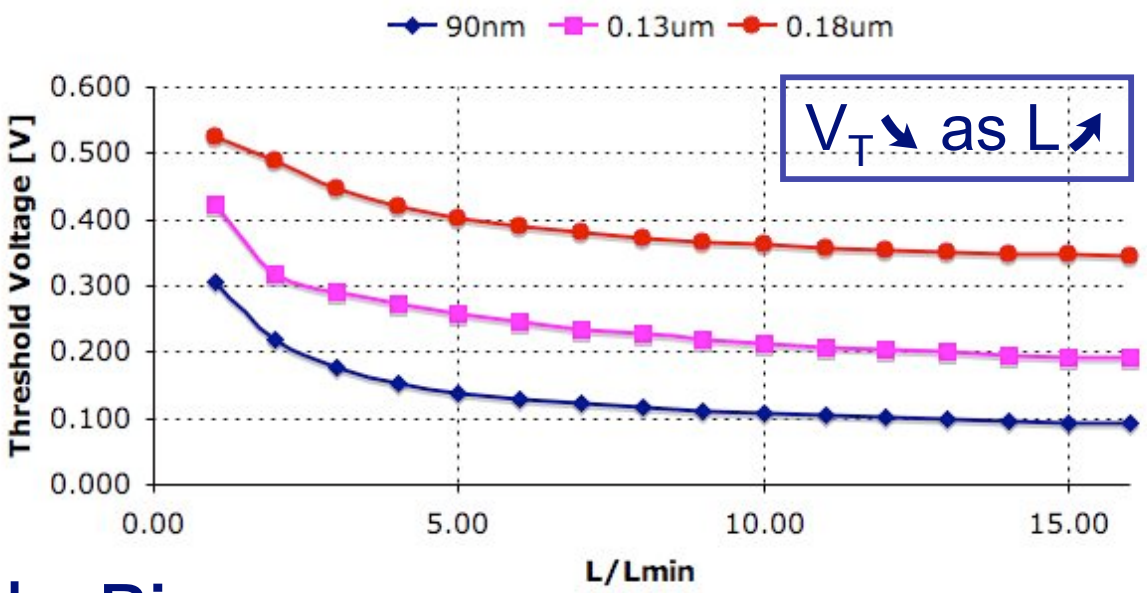
- Moderate to Strong Inversion
  (V_{GS}-V_T) ≈ 0.15 V & V_T = 0.15V → V_{GS} = 0.3V

Ultra-LV Challenges in OTAs

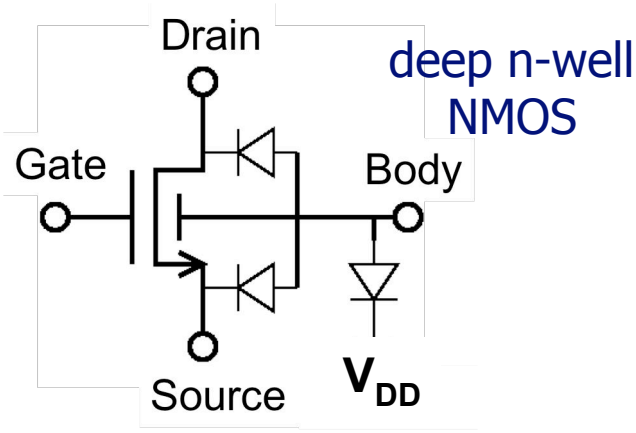


Device Level

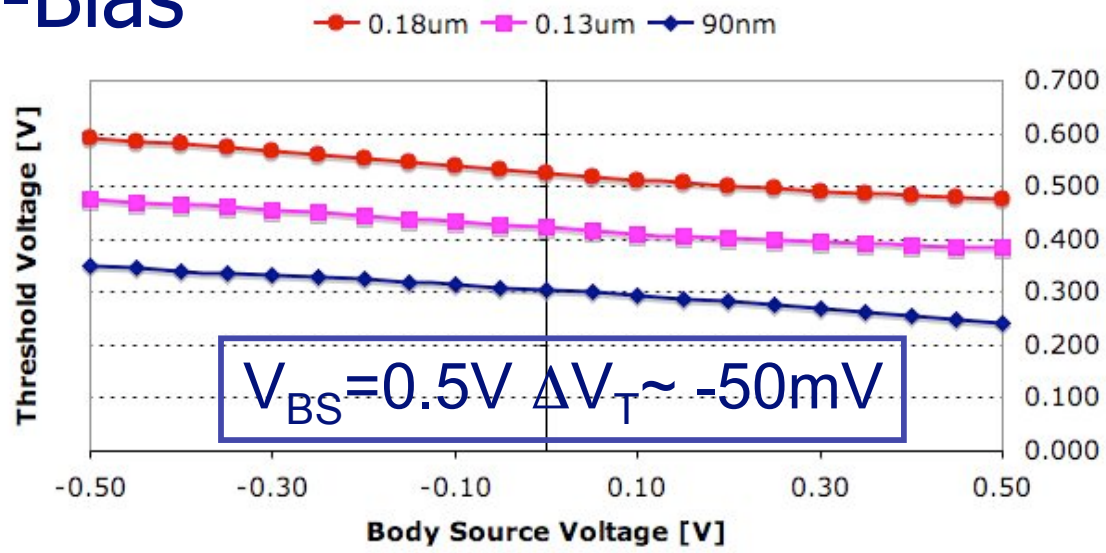
- RSCE



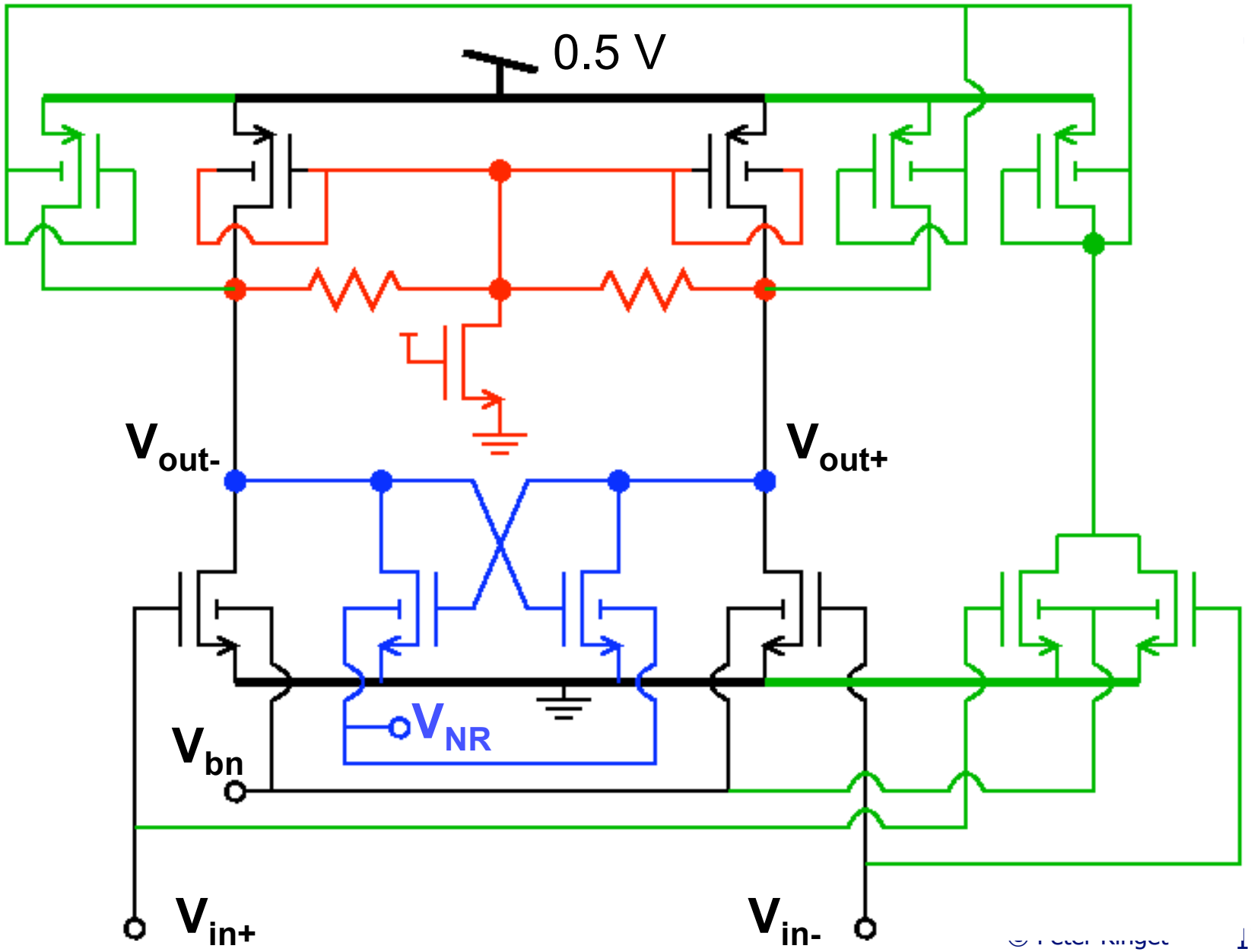
- Forward Body-Bias



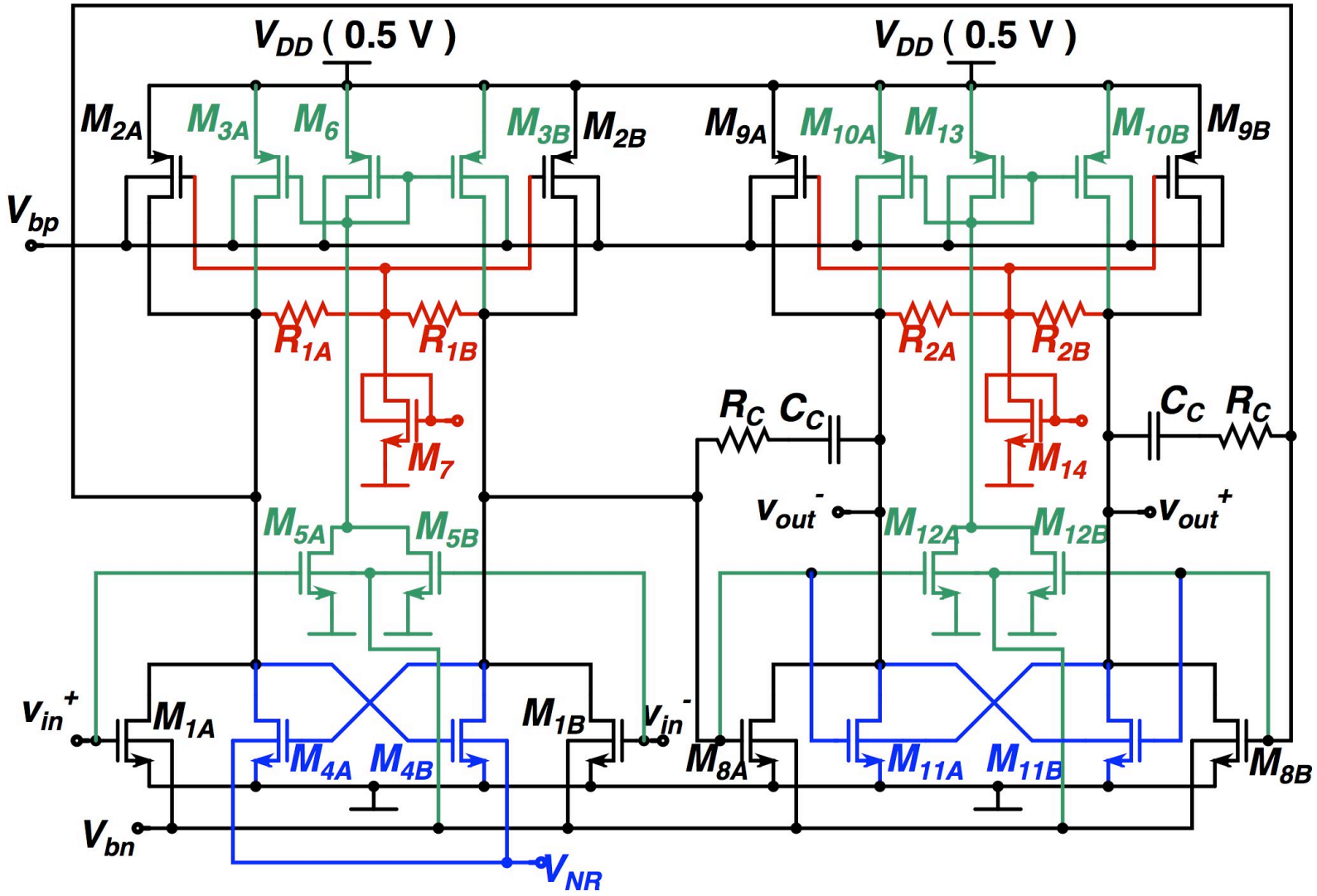
deep n-well NMOS



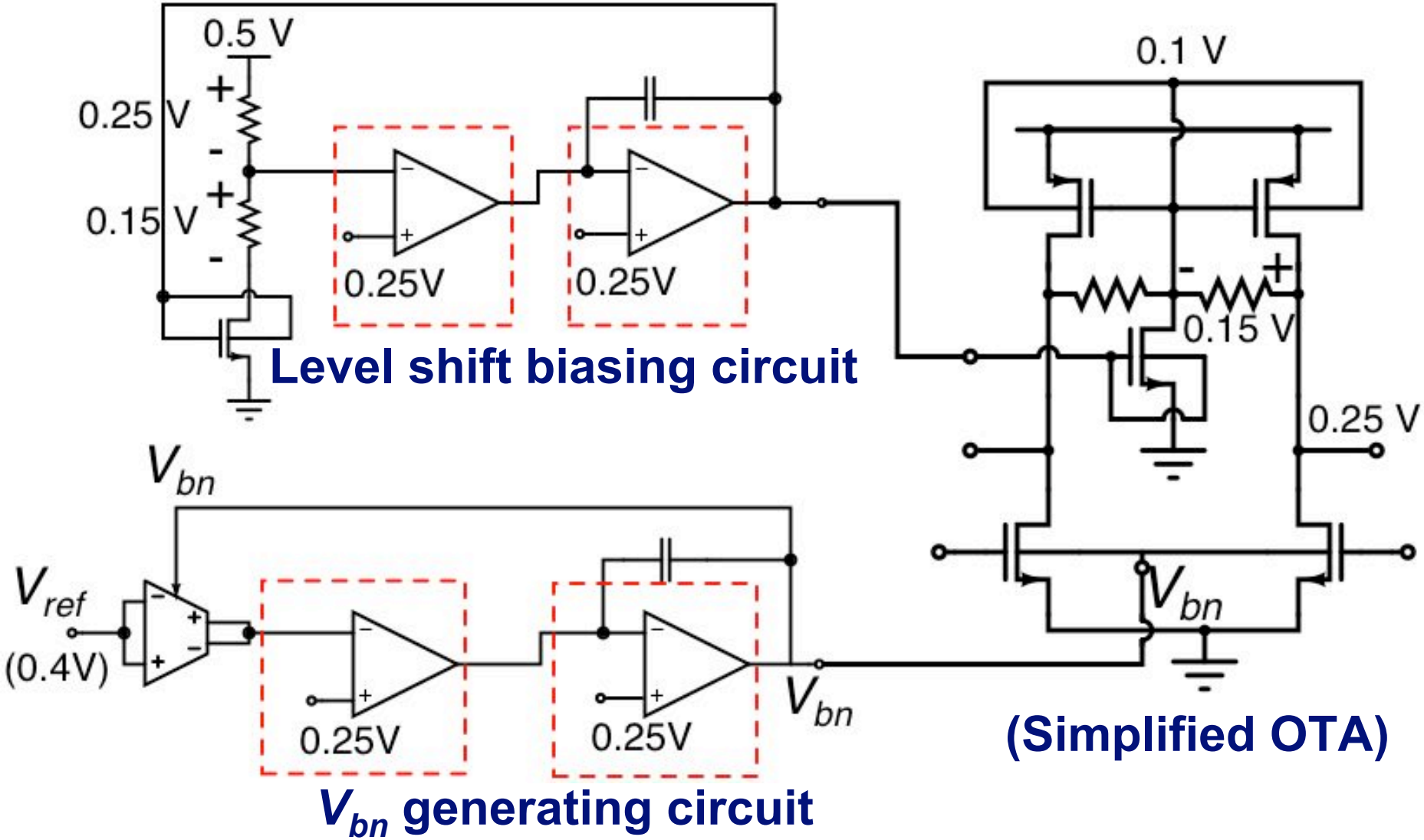
0.5 V Gate-input OTA stage



0.5 V OTA in 0.18um CMOS



On-chip biasing circuits

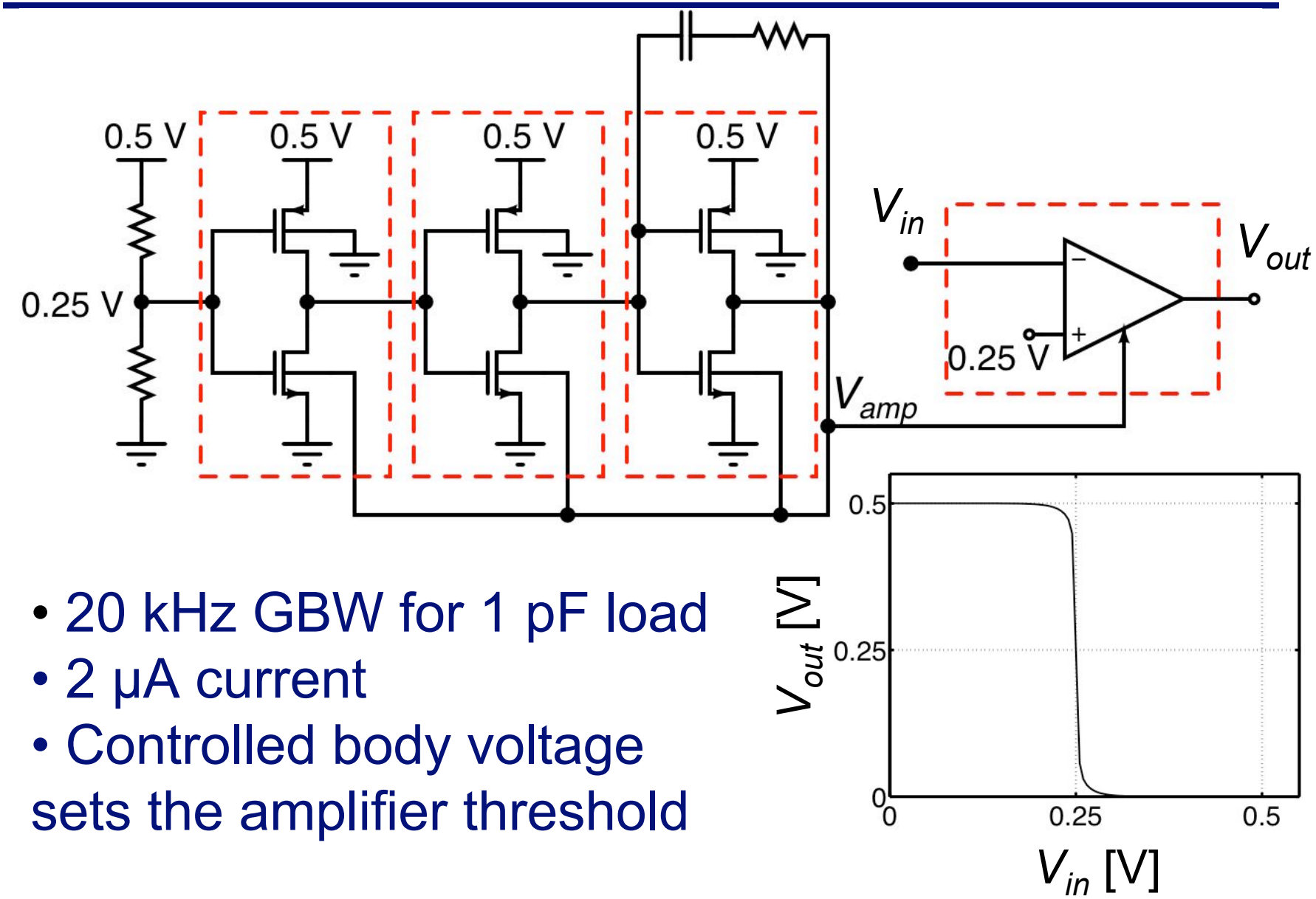


Level shift biasing circuit

(Simplified OTA)

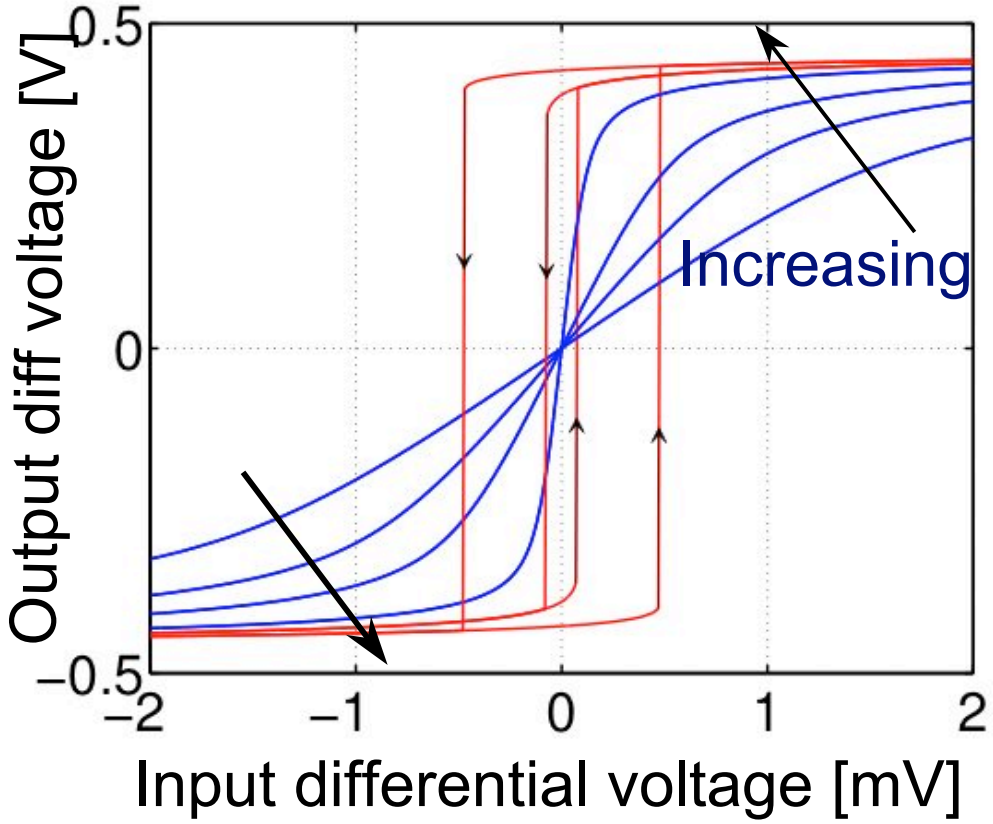
V_{bn} generating circuit

Error amplifier for biasing

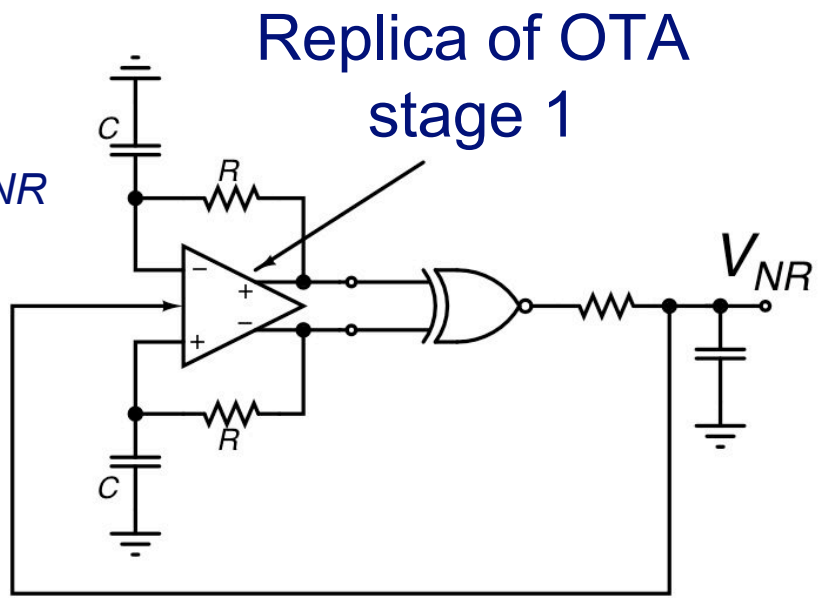


- 20 kHz GBW for 1 pF load
- 2 µA current
- Controlled body voltage sets the amplifier threshold

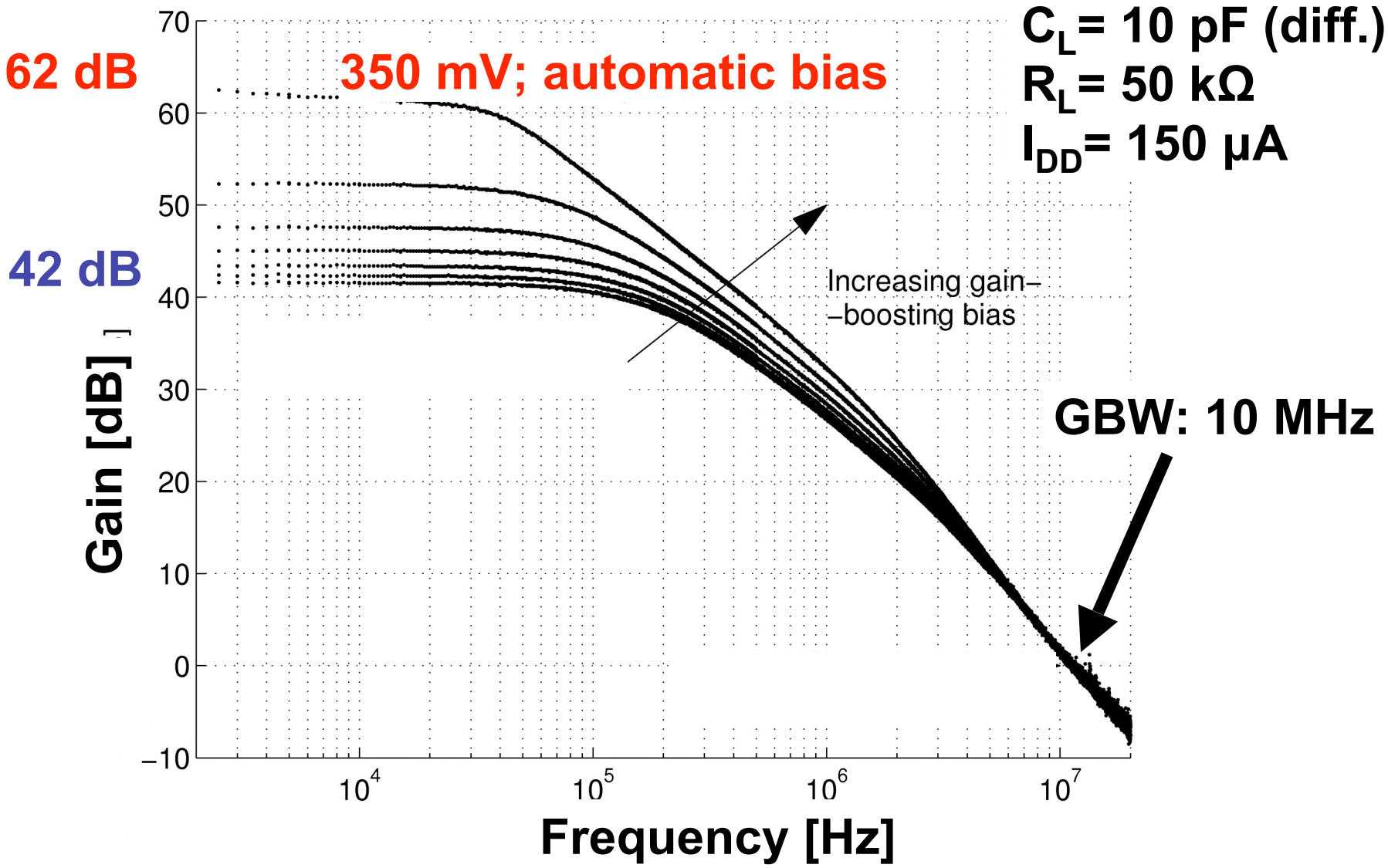
OTA DC transfer characteristics and V_{NR} generation



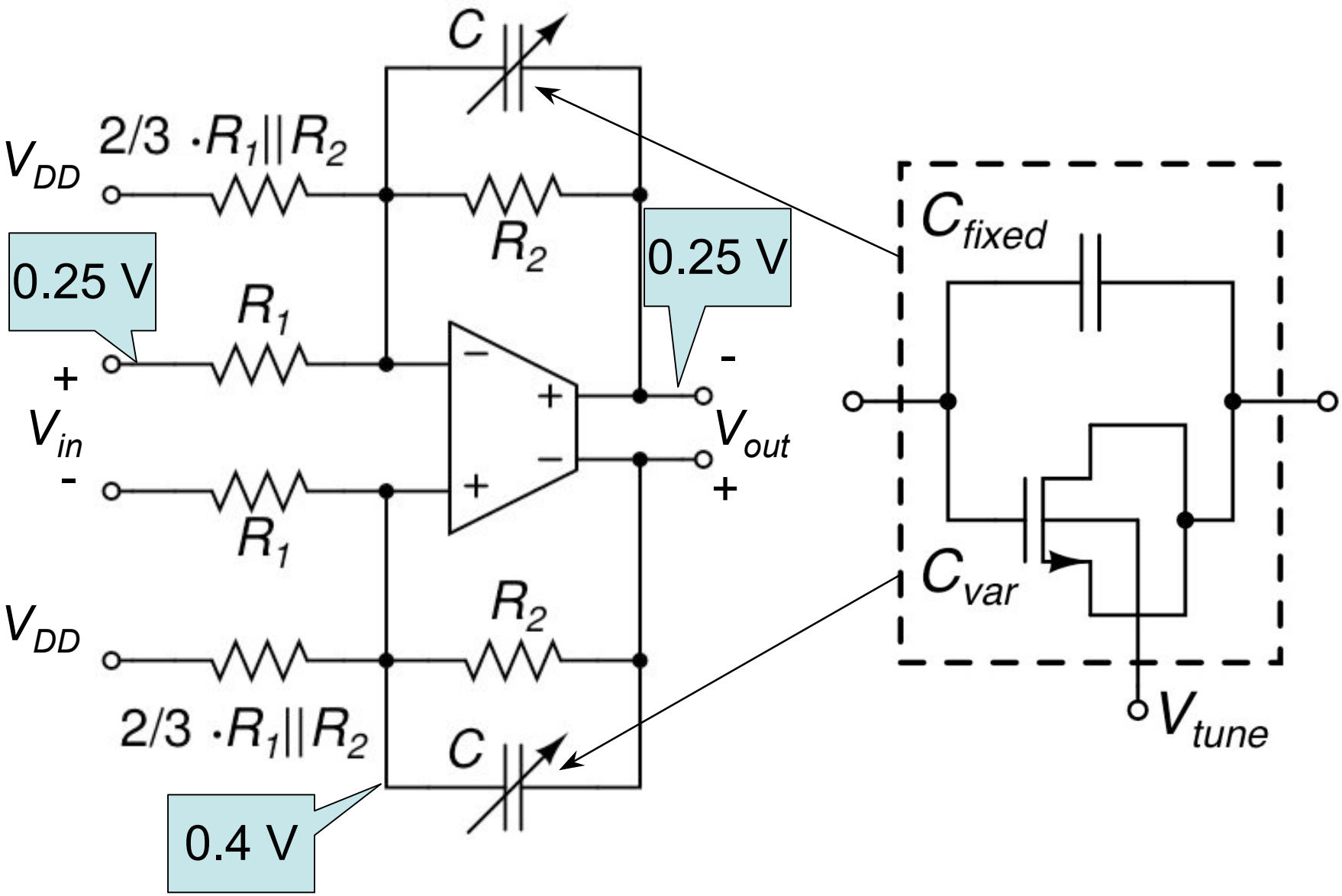
V_{NR} generating circuit



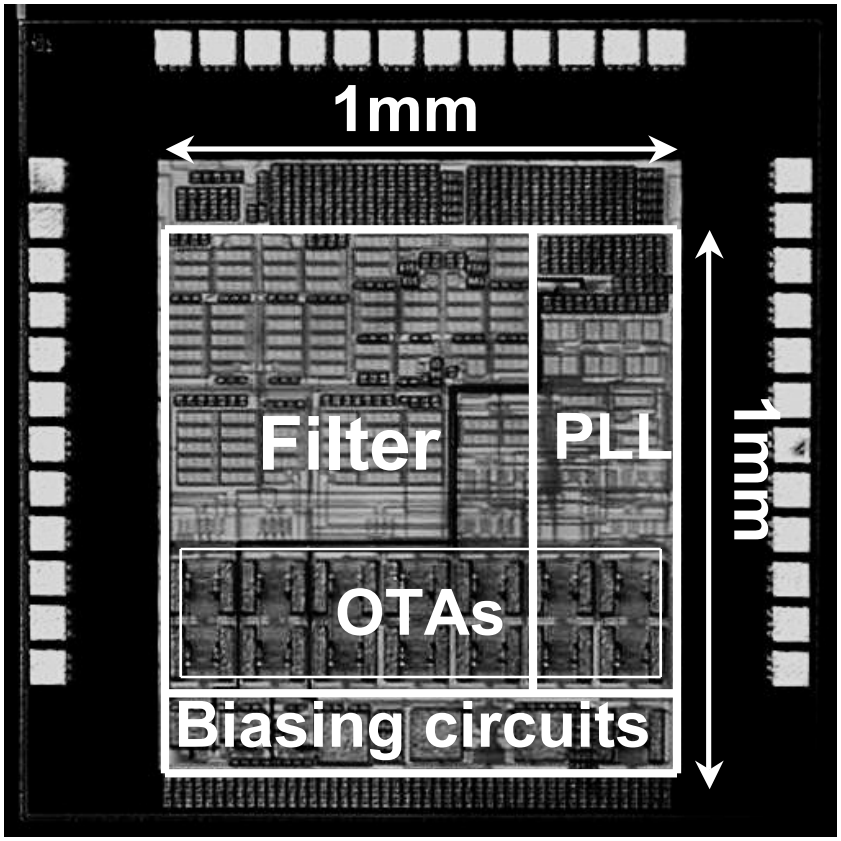
Open loop performance (meas.)

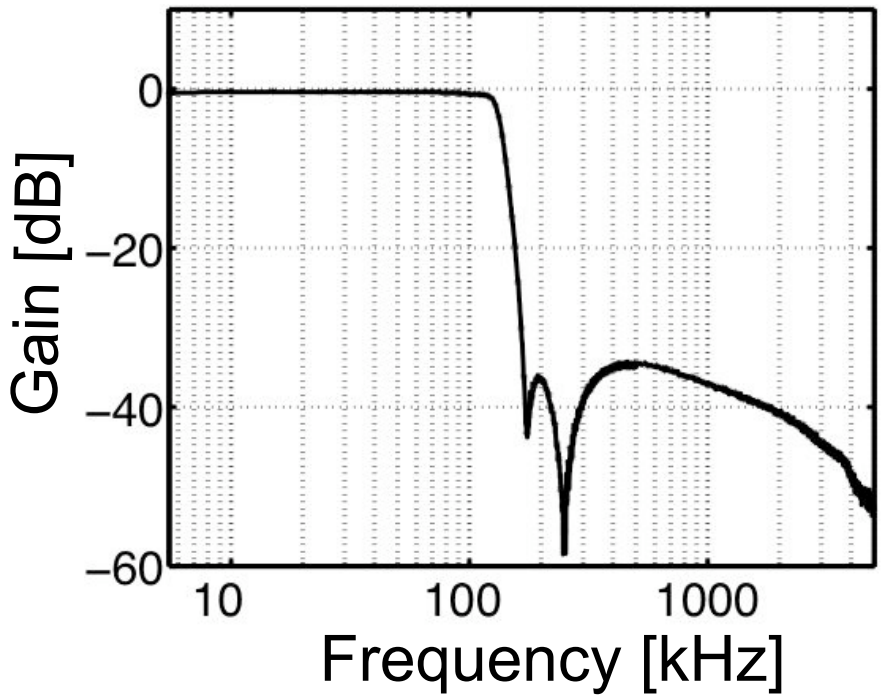


Low-voltage tunable integrator



0.5 V Fully integrated 5th order LPF





- Operation at 0.45 V to 0.6 V
- 1.1 mW power dissipation
- 57 dB dynamic range

[Chatterjee, ISSCC05, JSSC05]

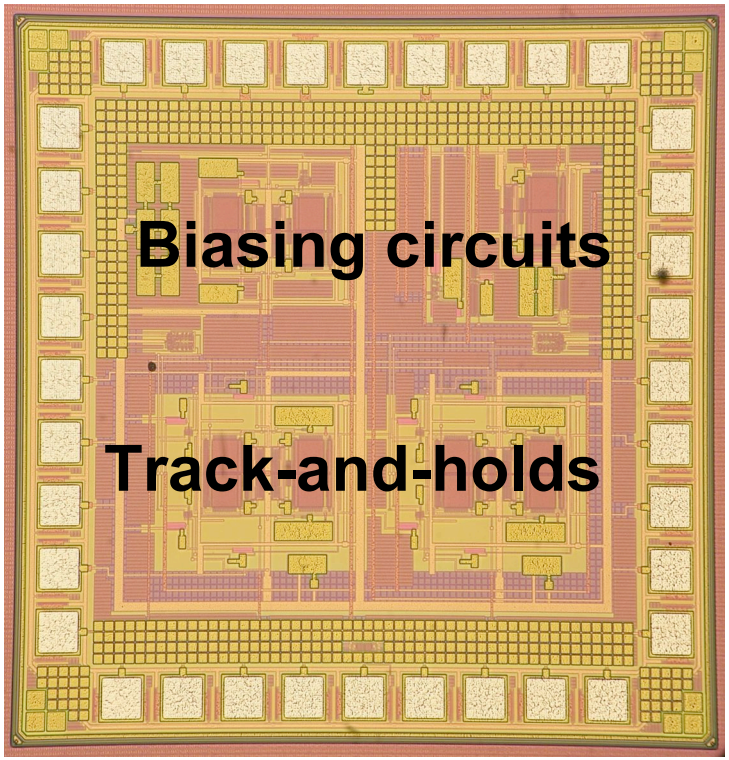
Performance summary at 27C

V_{DD} [V]	0.45	0.50	0.55	0.60
-3 dB cut-off frequency [kHz]	135.0	135.0	135.0	135.0
Total current [mA]	1.5	2.2	3.3	4.3
Noise [µV rms]	87	74	68	65
Input [mV rms] (100kHz / 1% THD)	50	50	50	50
In-band IIP_3 [dBV]	-5	-3	-3	-3
Out-of-band IIP_3 [dBV]	3	5	3	5
Dynamic range [dB]	55	57	57	58
Tuning range [kHz] $V_{tune} = V_{DD}$	96.5	88.0	84.5	69.0
Tuning range [kHz] $V_{tune} = 0.0$ V	153.0	154.5	148.0	150.5
VCO feed-thru @280kHz [µV rms]	104	85	72	72

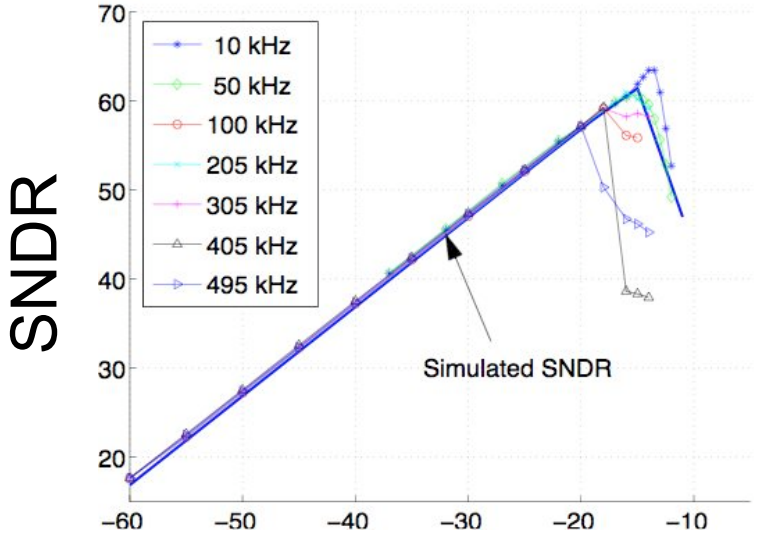
- Measured CMRR (10 kHz common mode tone): 65 dB
- Measured PSRR (10 kHz tone on power supply): 43 dB

Functionality tested from 5C to 85C at 0.5 V

0.5V 1Msps 60dB T/H amplifier

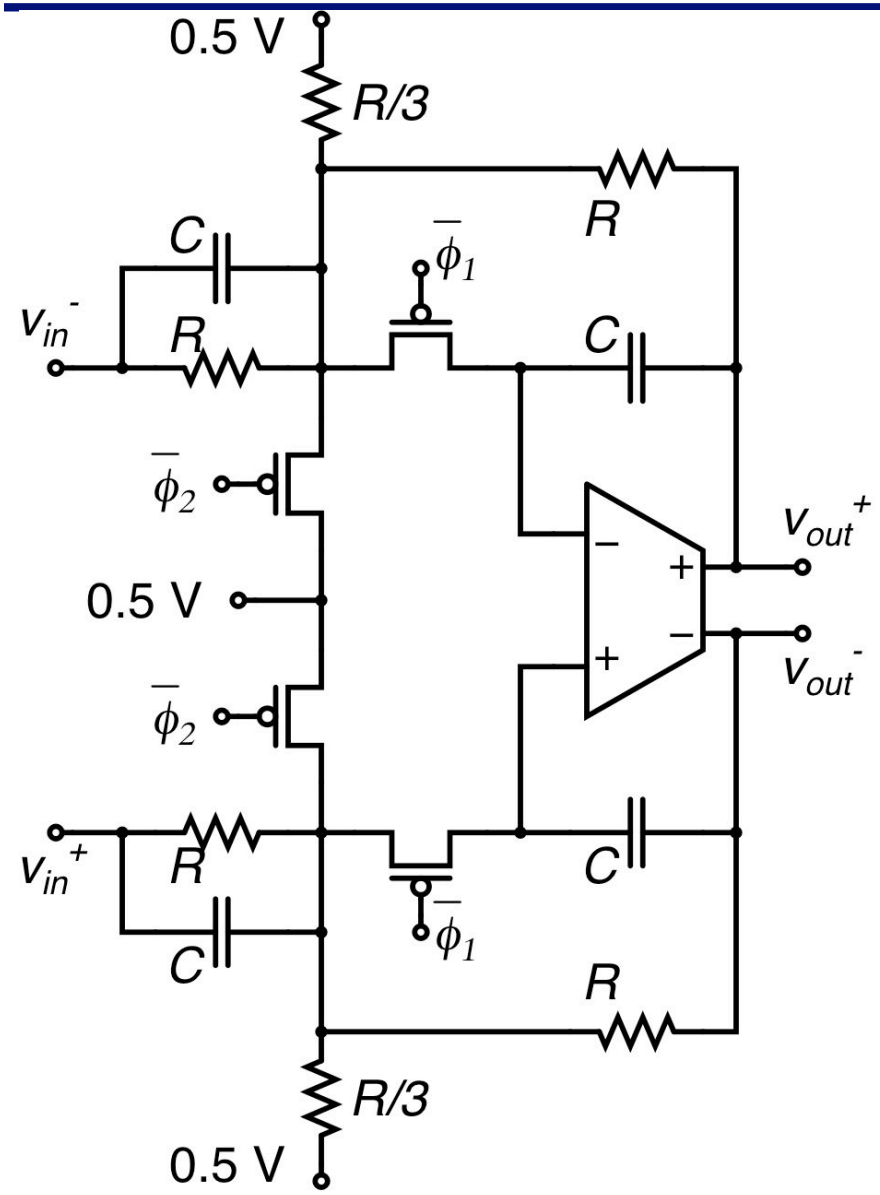


- 0.25µm CMOS
- $|V_t|$= 0.6V
- 60dB SNDR
- 1Msps
- 0.6mA at 0.5V



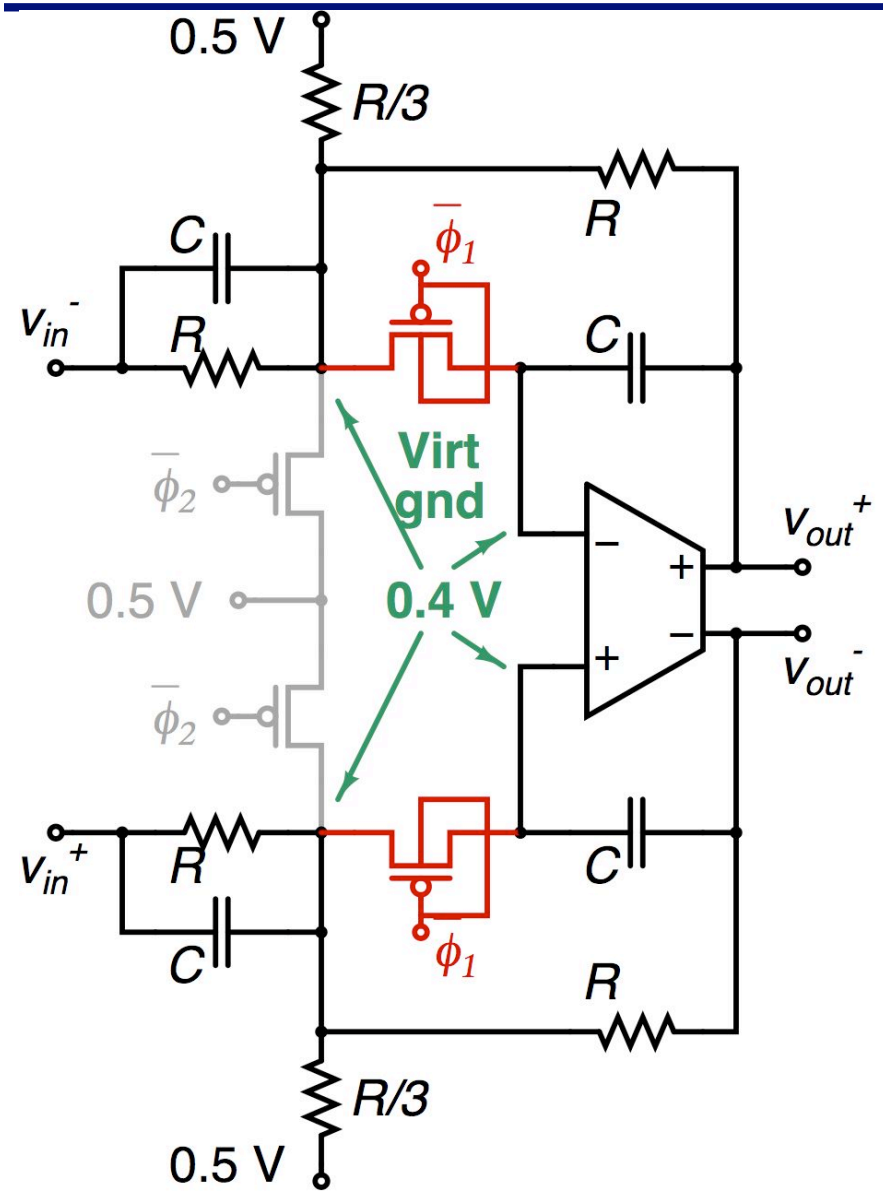
- True low voltage
- No clk boosting
- [Chatterjee, VLSI 06, JSSC07]

0.5V Differential Track and Hold



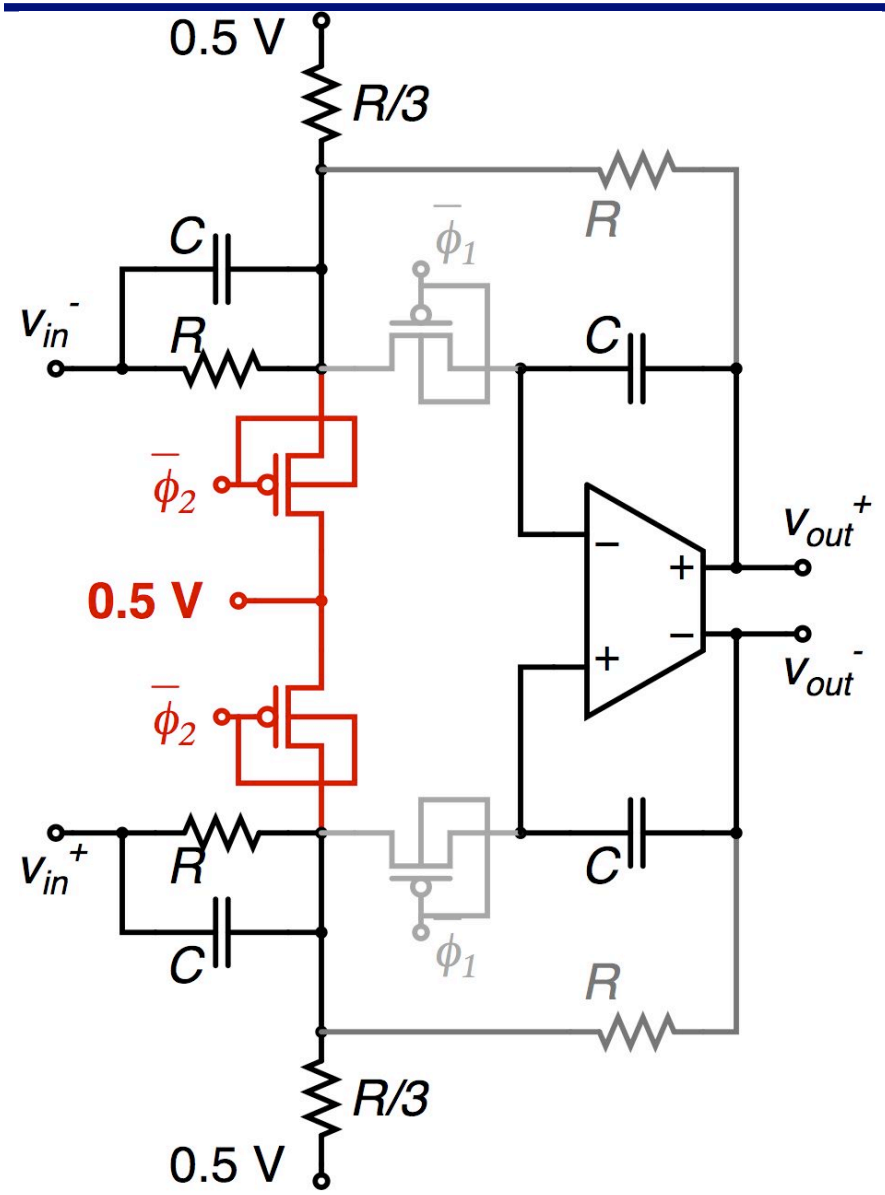
- Gate-input OTA used.
- Track phase during ϕ_1, hold phase during ϕ_2.
- During track phase, pole and zero cancel out to enable fast response.
- pMOS switches have V_T of about 0.5V.

Track mode operation



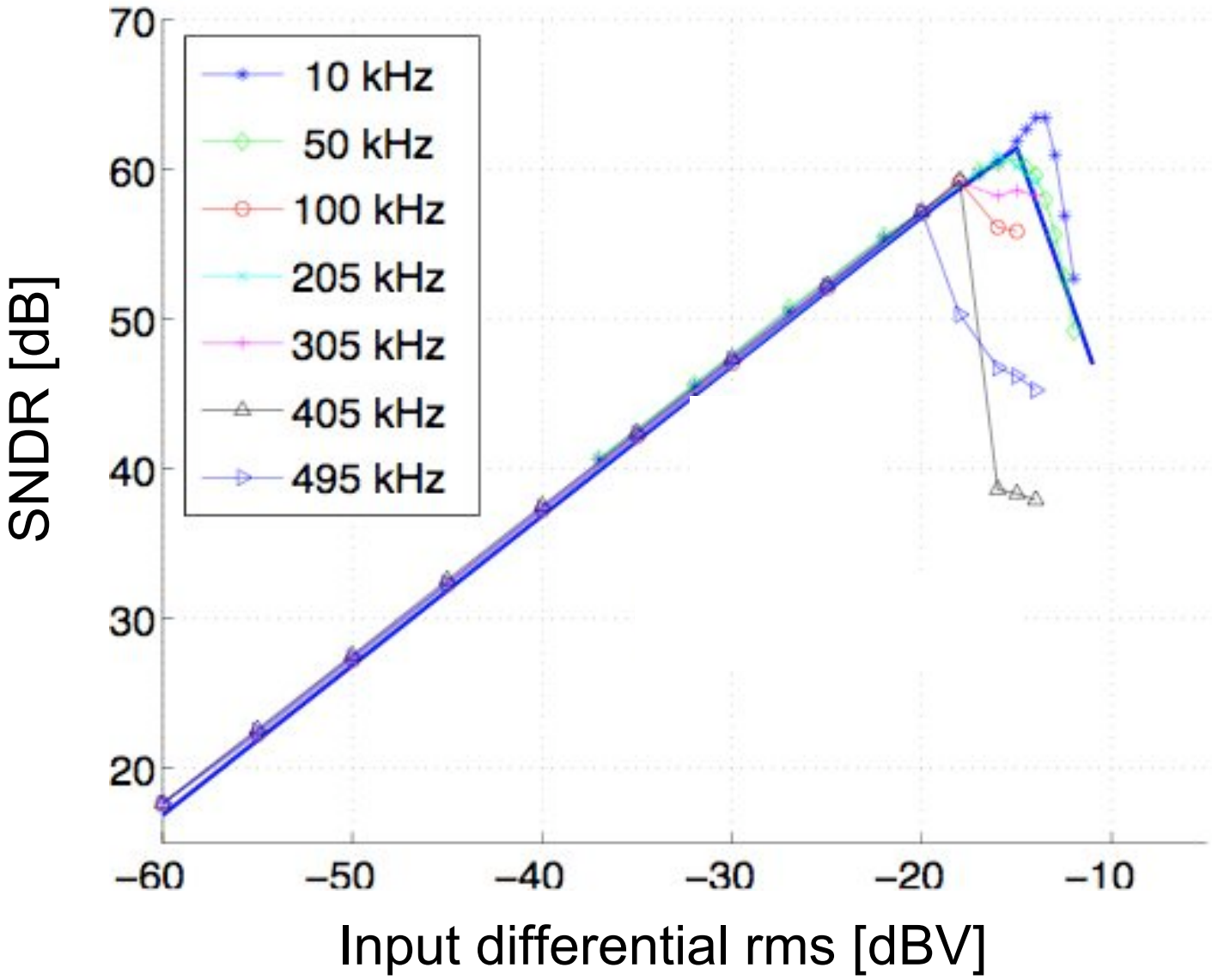
- Resistors to 0.5V maintain required OTA input CM voltage of 0.4V.
- To enable better switching, both gate and body of the switch are used.
- No voltage swing on either side of the switches.

Hold mode operation



- Gate and body of the switch used for better switching.
- No signal swing on both sides of the switches.
- OTA input voltages held constant.

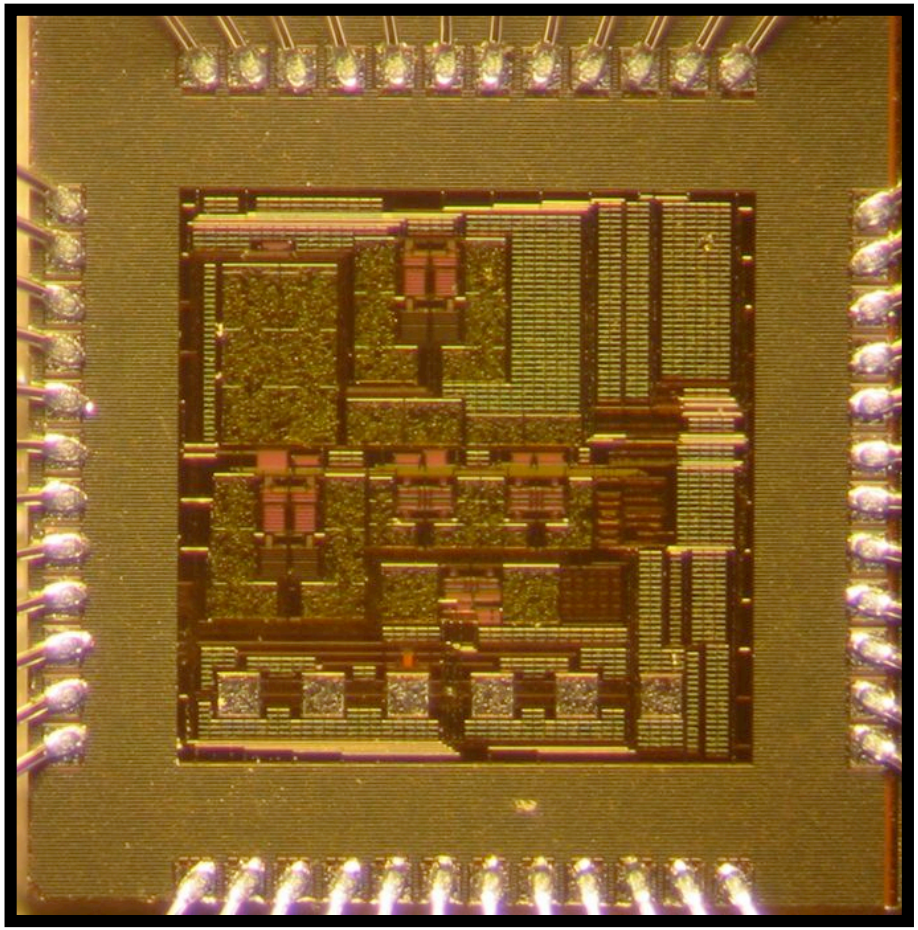
Measured SNDR



Measured performance

Power supply	0.5V
Current consumption	600µA
Sampling rate	1Msps
Diff. input refd. integrated noise	$188\mu V_{RMS}$
Peak SNDR f_{IN}=50kHz; $V_{in,diff}$=$178mV_{RMS}$	60dB
Peak SNDR f_{IN}=495kHz; $V_{in,diff}$=$100mV_{RMS}$	57dB
Hold mode droop rate on diff. output	7.6µV/µV
Pedestal on diff. output	0.8mV
Track mode bandwidth	3.9MHz

0.5 V 74 dB SNDR 25kHz ΣΔ Modulator



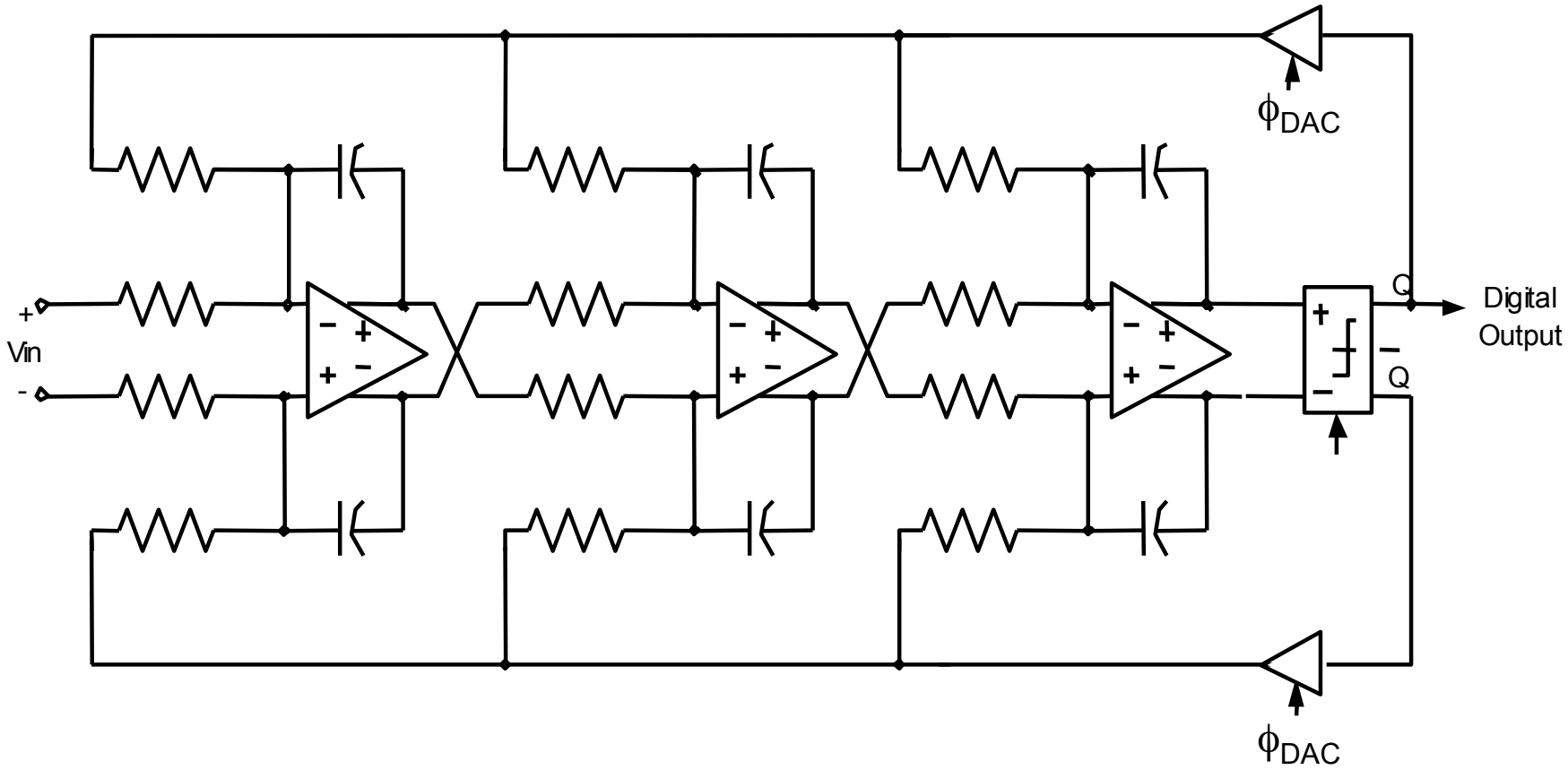
- 0.18 µm CMOS
- MIM caps
- Triple-well devices
- High-res resistors

- Body-input, gate-clocked logic
- Return-to-open feedback

- [Pun, Chatterjee, Kinget, ISSCC 06]

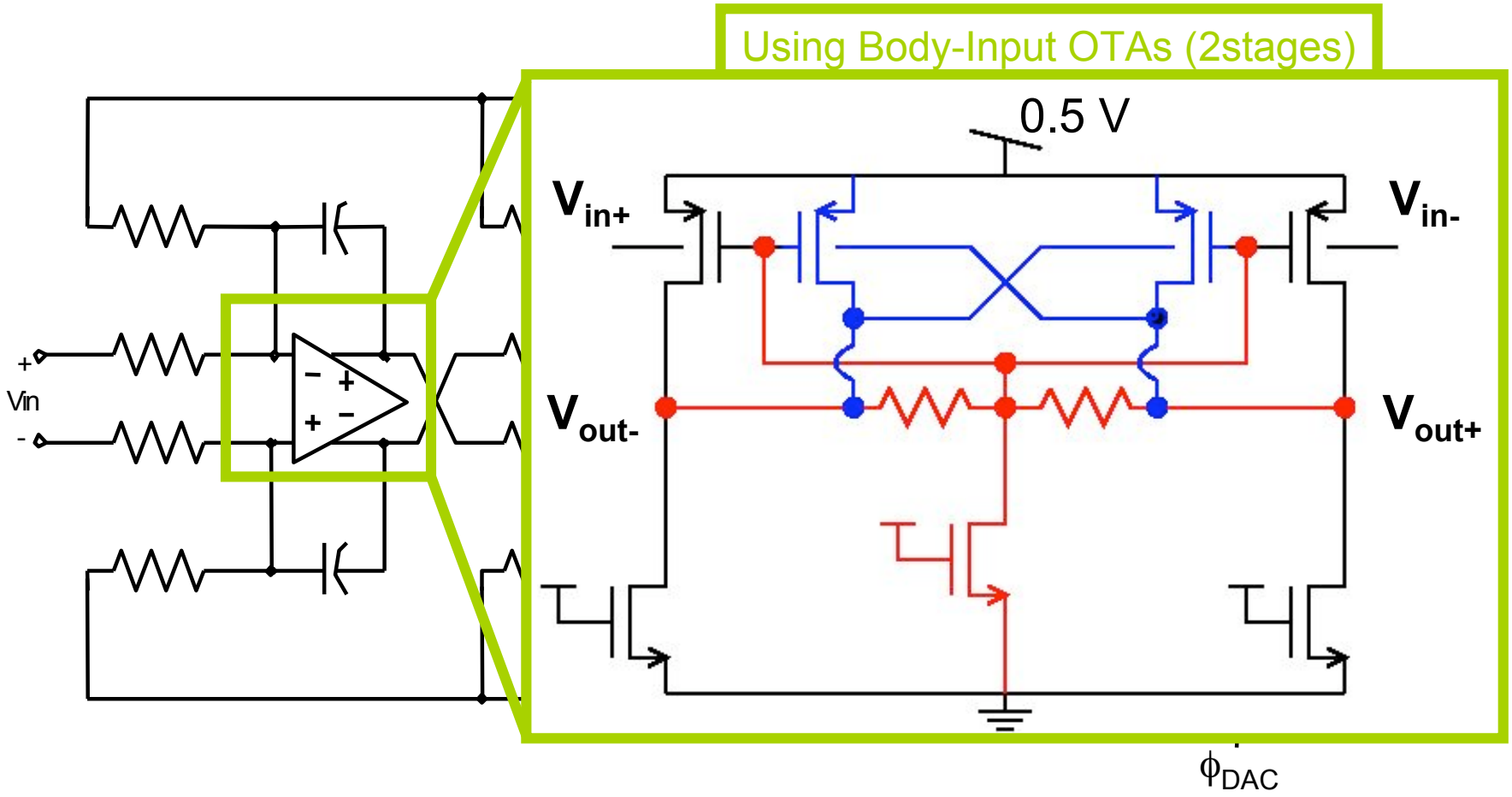
3rd order CT ΣΔ Modulator

Using Active RC integrators



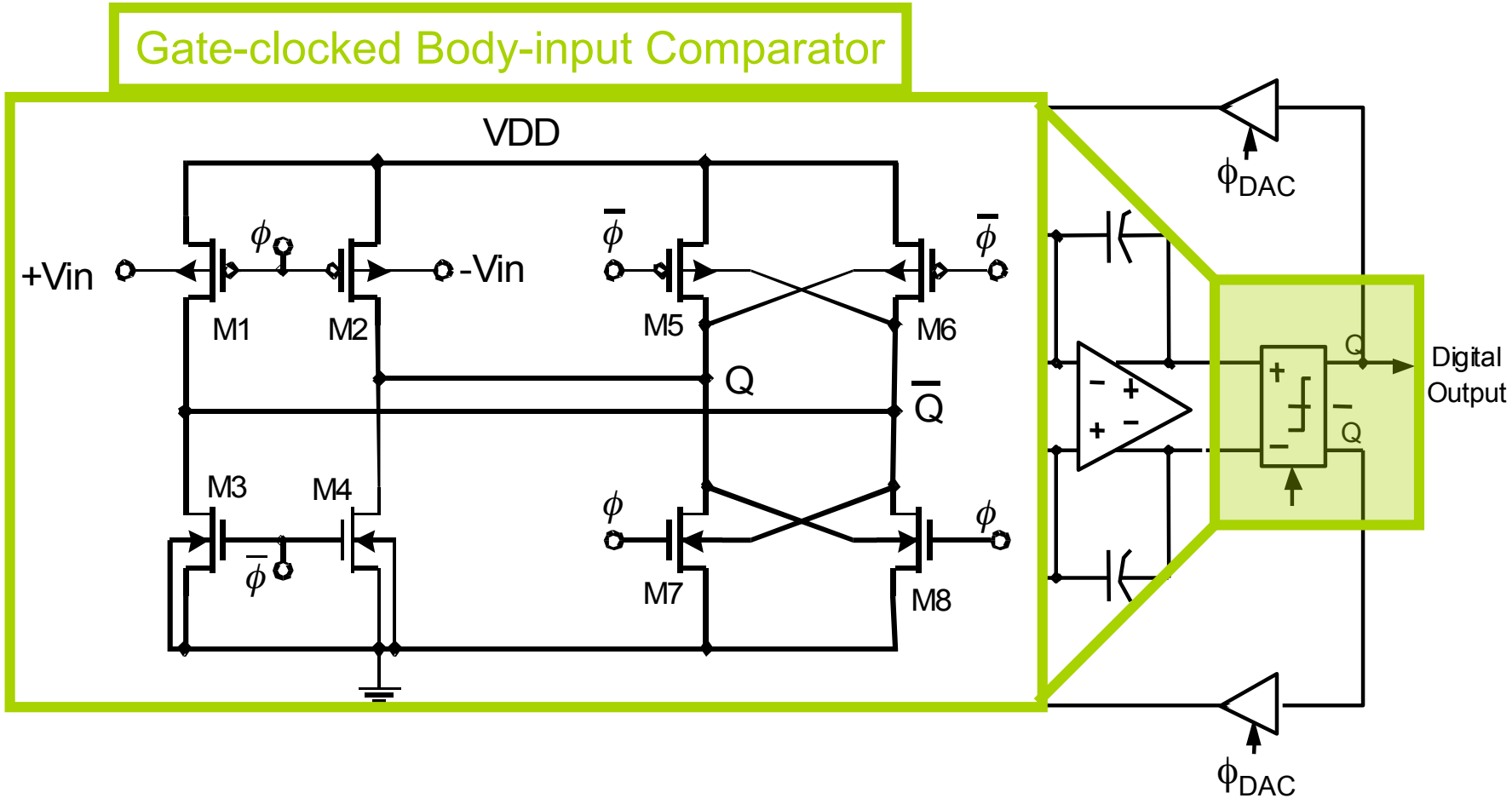
3rd order CT ΣΔ Modulator

Using Active RC integrators



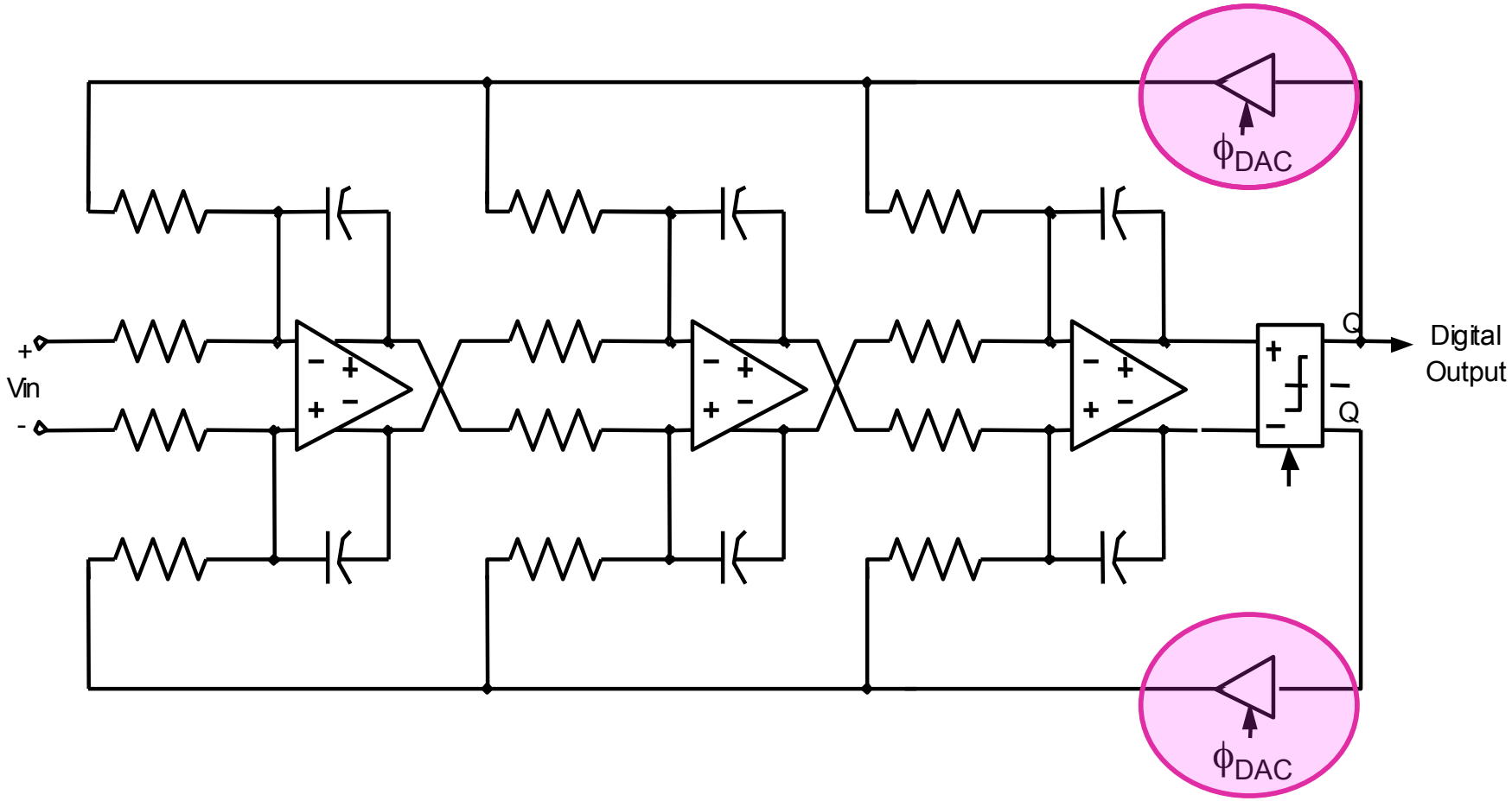
3rd order CT ΣΔ Modulator

Using Active RC integrators

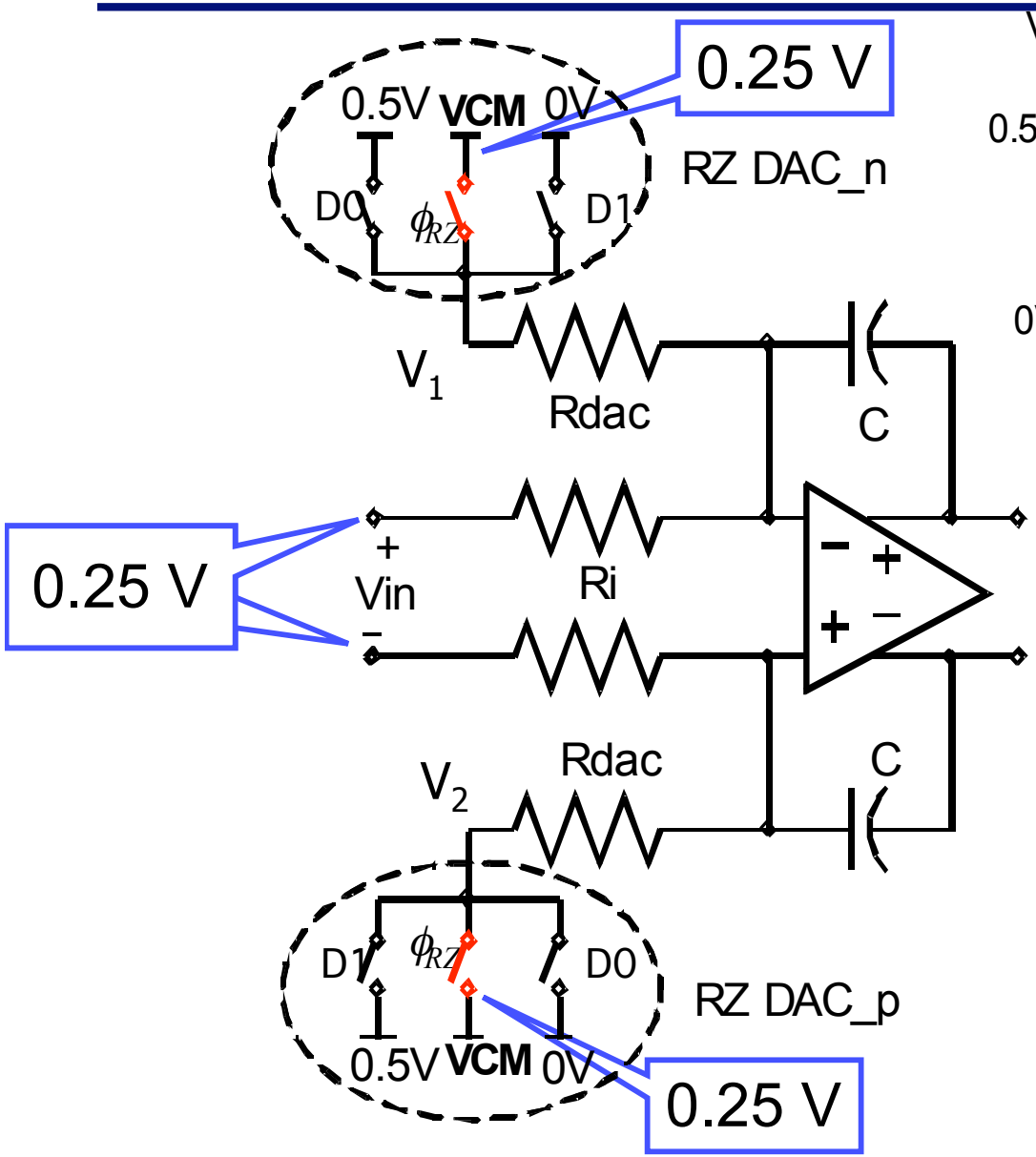


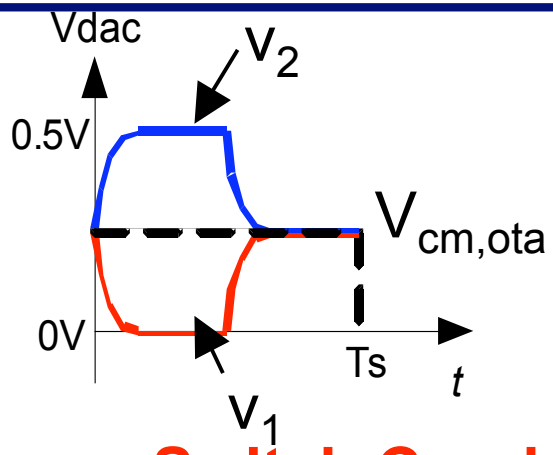
3rd order CT ΣΔ Modulator

Using Active RC integrators

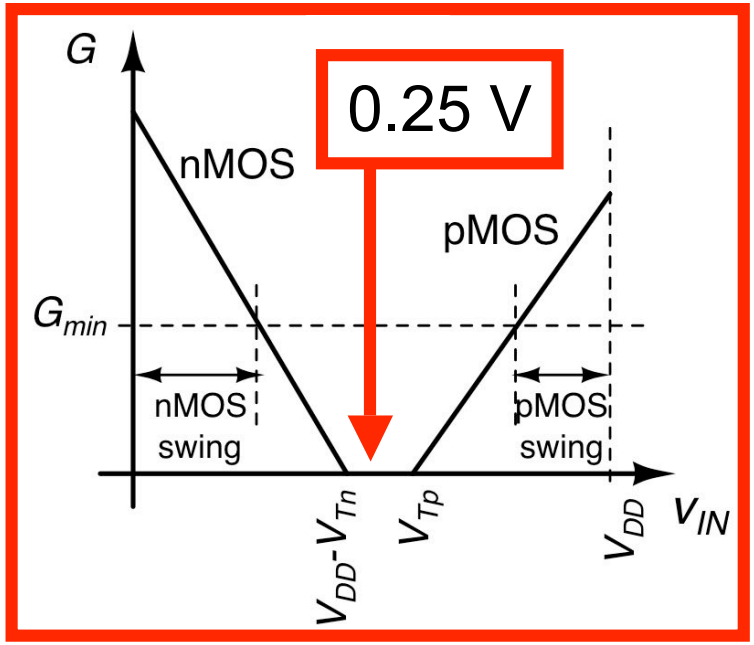


RZ Challenge: Switches at $V_{DD}/2$



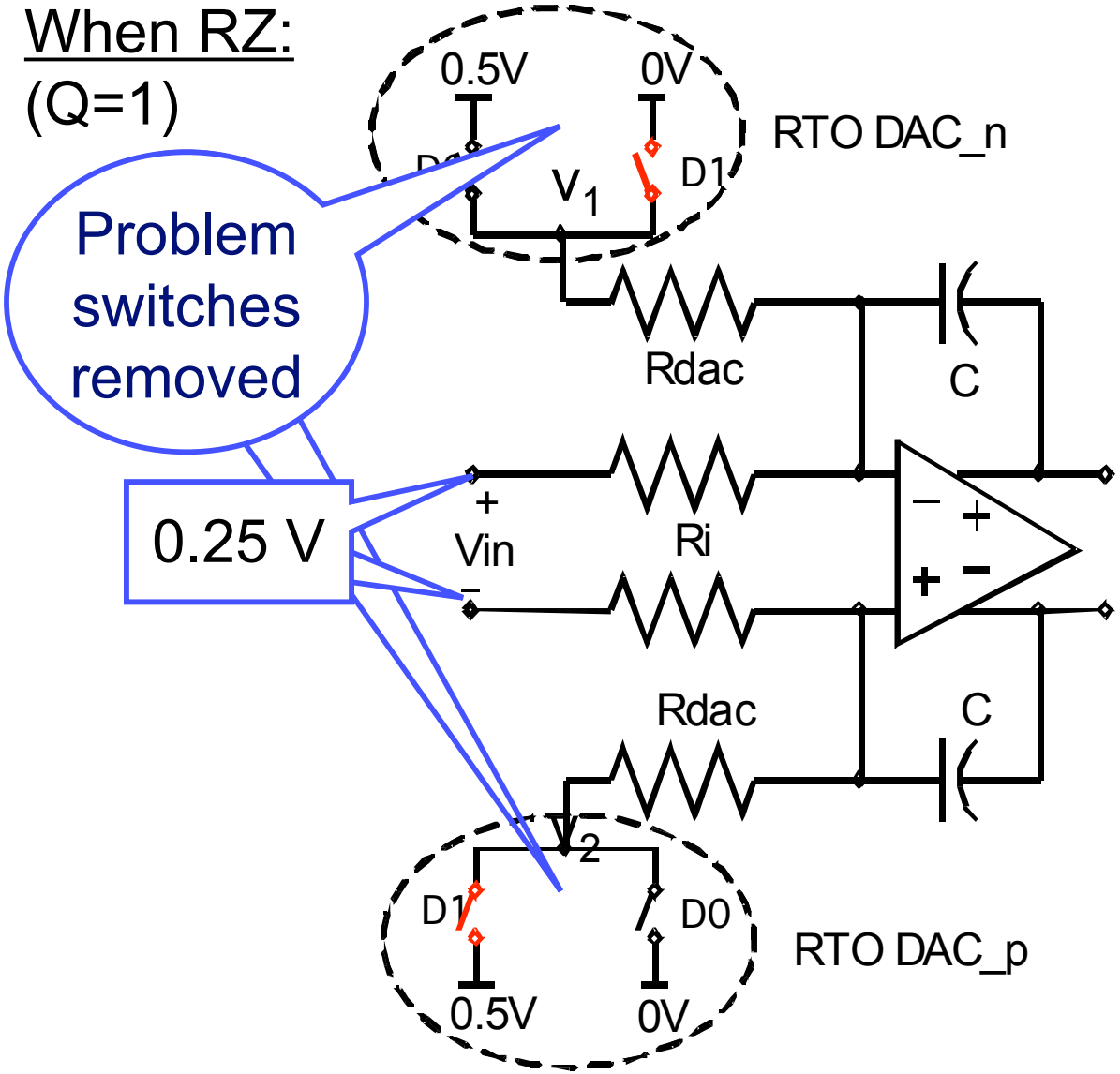


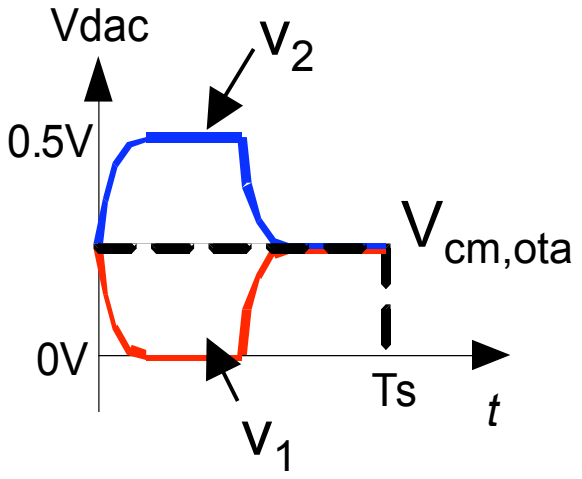
Switch Conductance

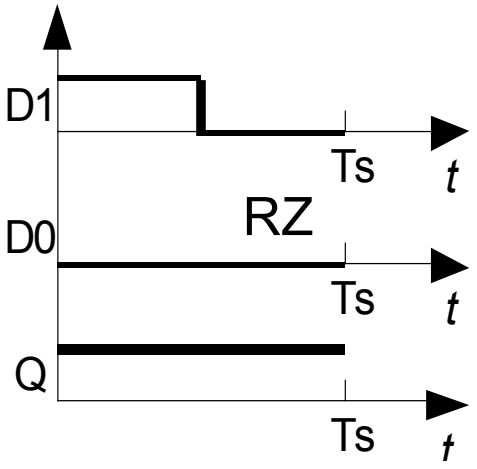


Solution: Return-to-Open

When RZ:
(Q=1)







Solution: Return-to-Open

When RZ:
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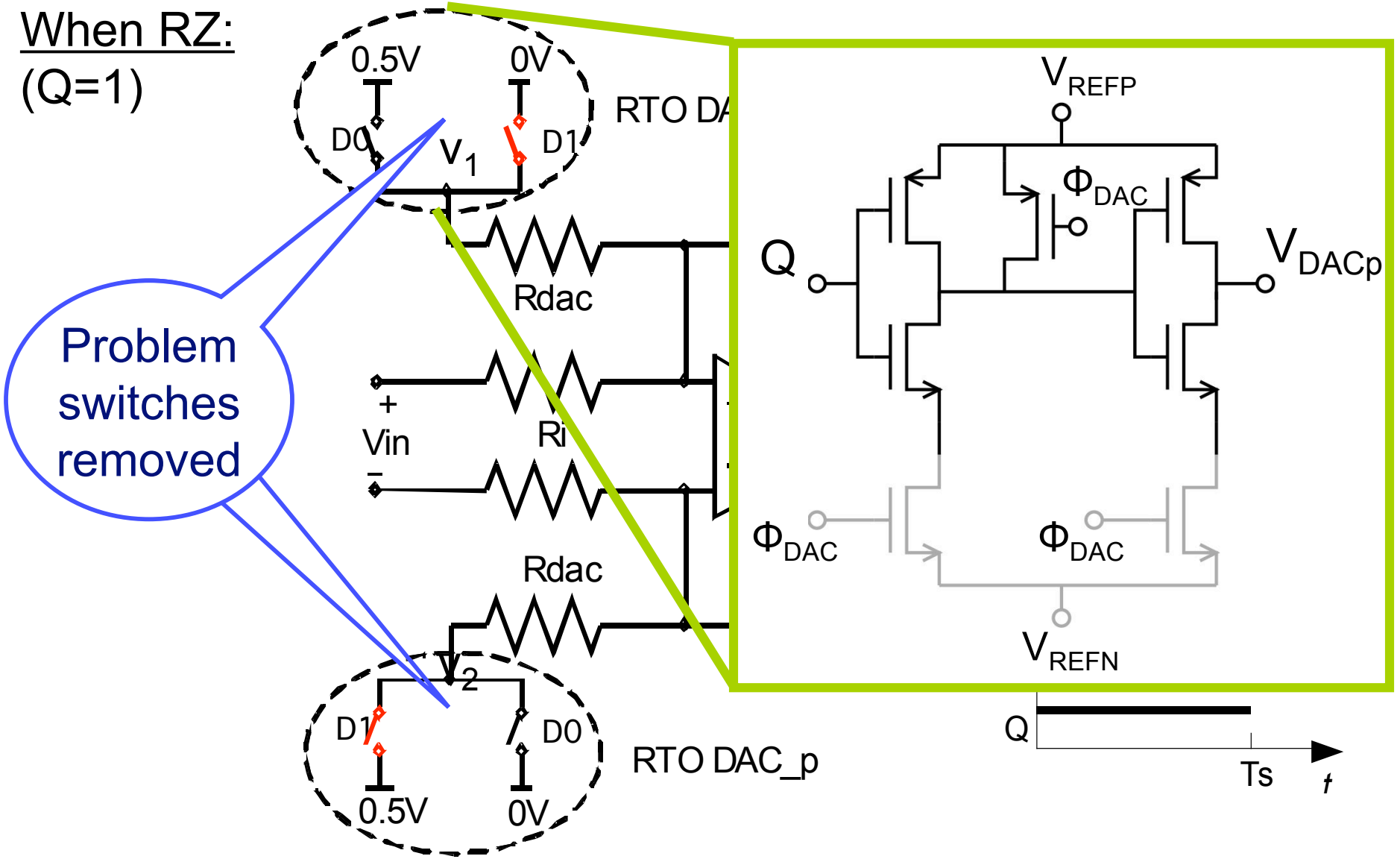
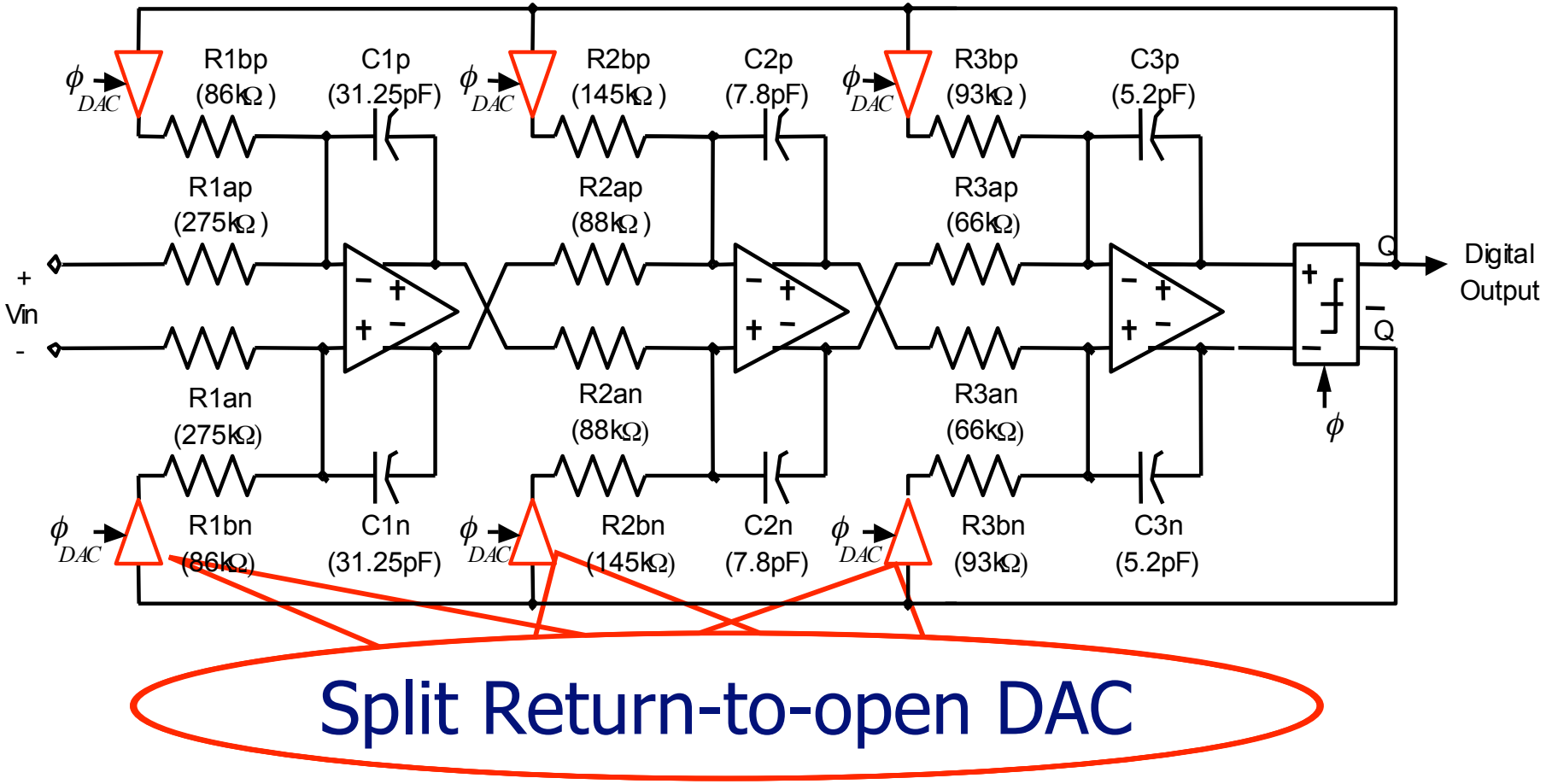


Return-to-open CT SDM



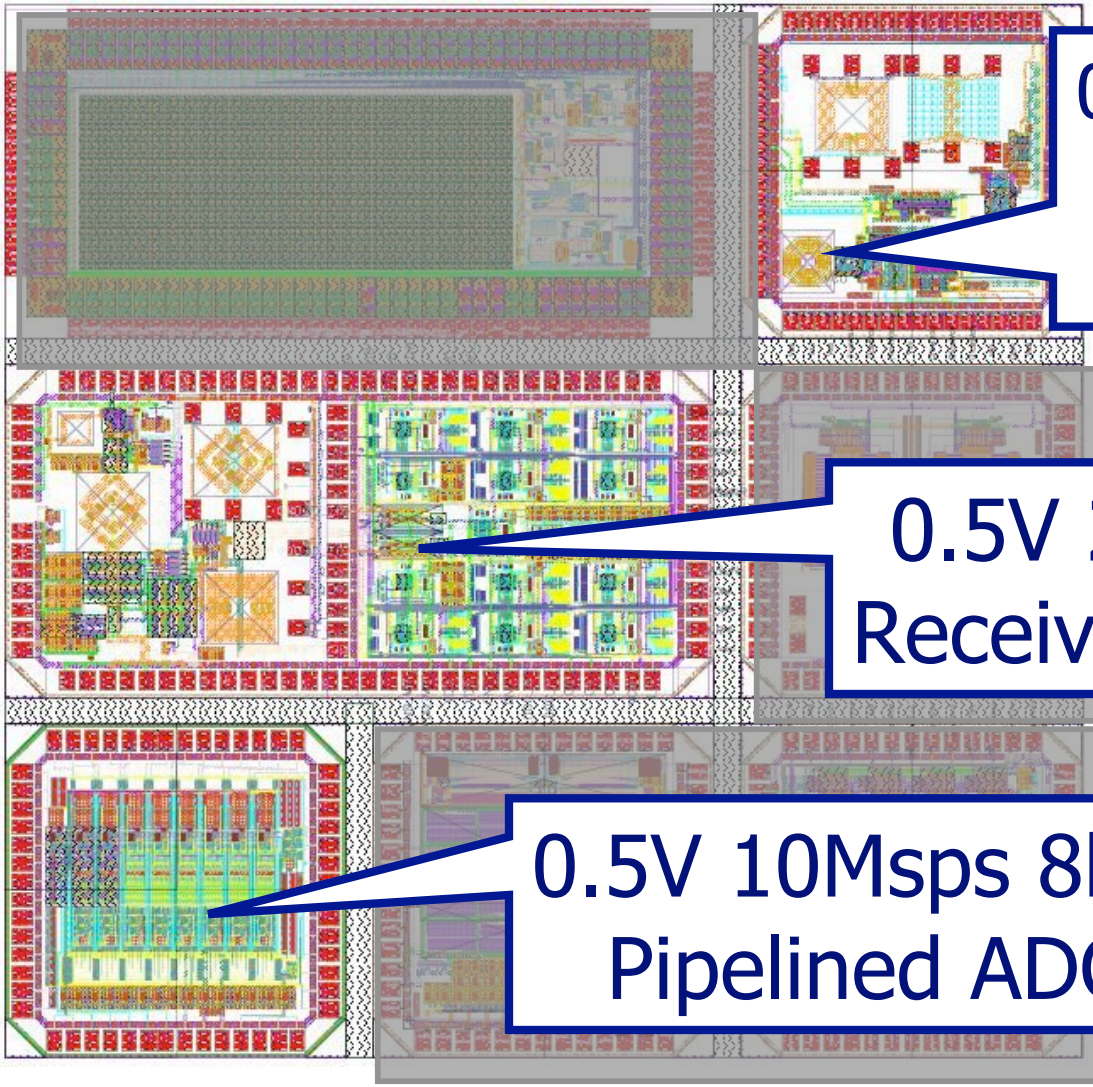
Only switches to VDD or VSS

BW = 25kHz, fs = 3.2MHz,
Vin,max = 1Vppdiff.

Performance Summary at 25°C

Modulator type	1-bit, 3rd order, continuous-time		
Signal bandwidth	25 kHz		
Sampling frequency / OSR	3.2 MHz / 64		
Input range	1 Vppdiff.		
Supply Voltage	0.45V	**0.5V**	0.8V
SNDR @ Vin = 1Vppdiff.	71 dB	**74 dB**	74 dB
SNR @ Vin = 1Vppdiff.	76 dB	**76 dB**	74 dB
Power consumption (total) Sigma Delta Modulator Output buffers		**370 μW** **300 μW** **70 μW**	
Active die area	0.6 mm^2		
Technology	0.18 μm CMOS (standard V_T, triple-well, MIM, and HiRes Poly)		

Recent Work in 90nm CMOS

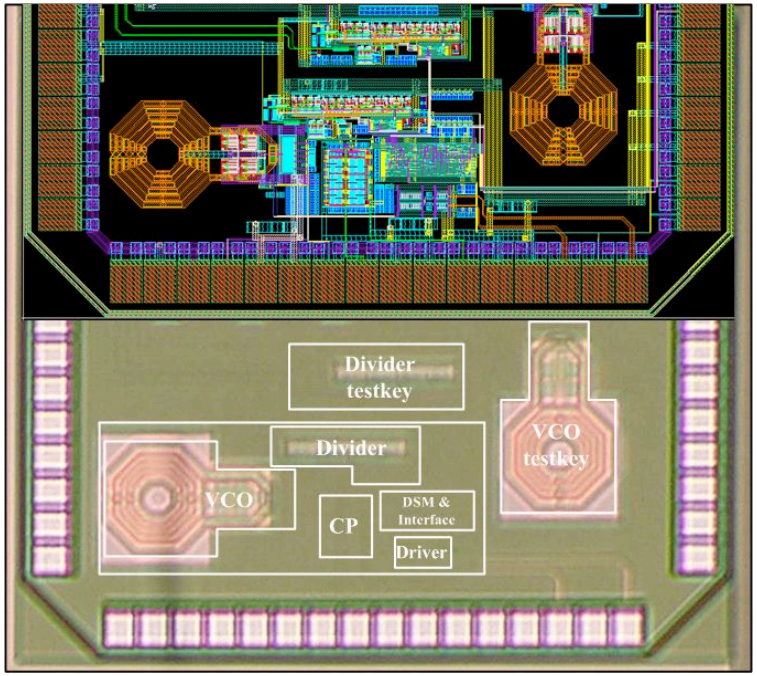


0.65/0.5V 2.4-2.6GHz
Fractional N
Freq. Synthesizer

0.5V 2.4GHz Sliding-IF
Receiver + I/Q Baseband

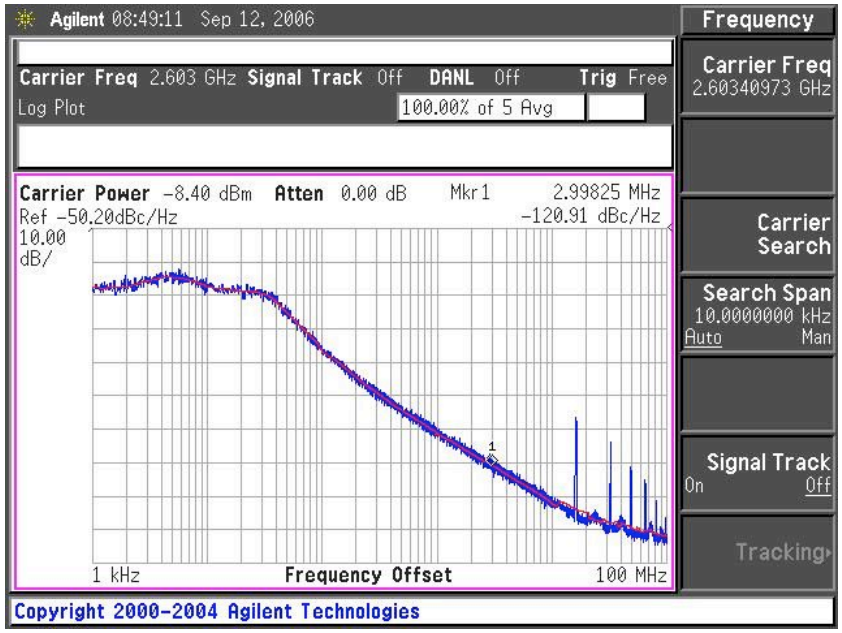
0.5V 10Msps 8bit
Pipelined ADC

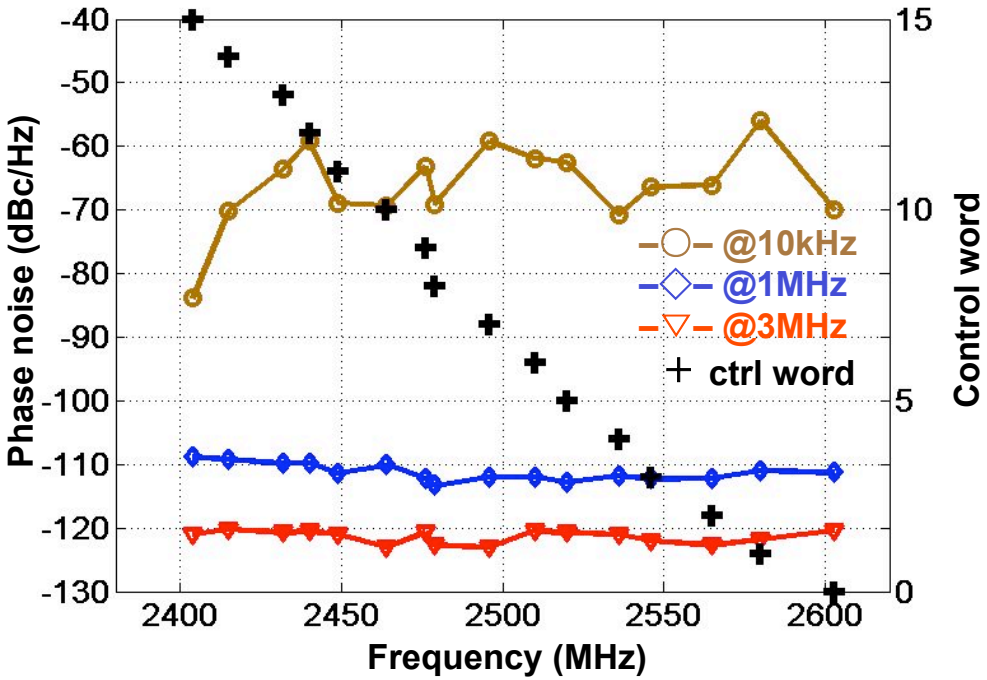
0.65V/0.5V 2.4-2.6GHz Fractional-N Synthesizer



- Swings on all VCO nodes are kept within the supply rails for reliability.
- Forward body bias to enhance the divider speed.
- Fractional-N DSM dithering shifted to later divider stages to prevent noise injection into forward biased body.
- Staggered clock to prevent jittering caused by simultaneous switching.
- 90nm CMOS
- [S. Yu & P. Kinget, ISSC07]

Performance Summary

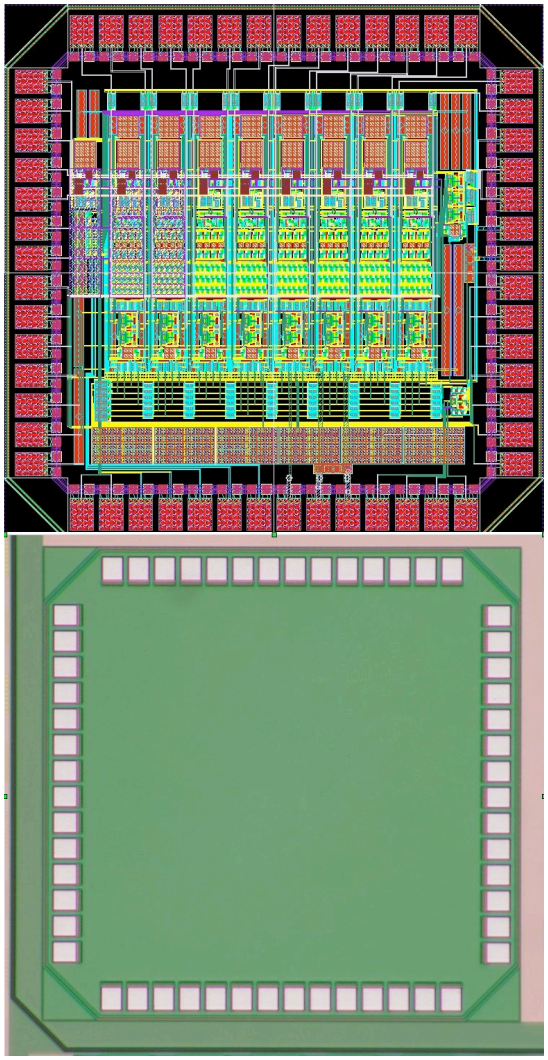




- AVDD 0.5V - 2.5mW
- DVDD 0.65V - 3.5mW
- 0.14mm^2 - 90nm CMOS
- RVT devices

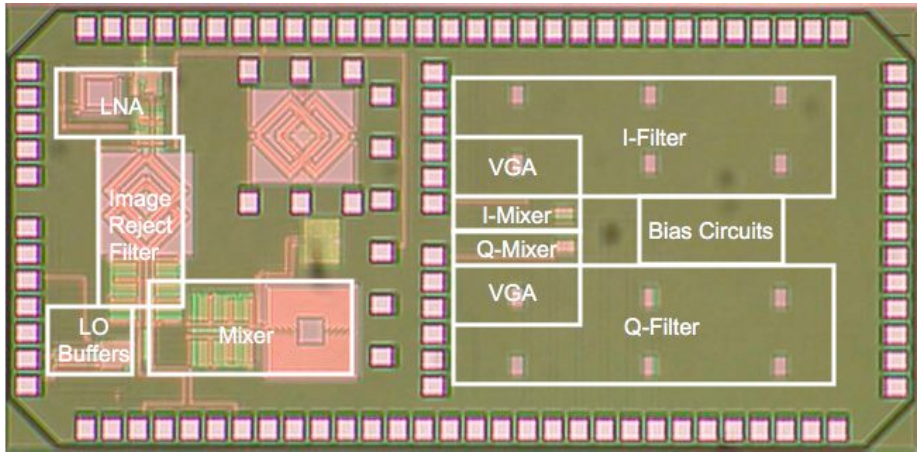
- 2.4-2.6GHz
- Phase noise:
  -120dBc/Hz @ 3MHz
- Spurs: -52dBc

A 0.5V 8bit 10Msps Pipelined ADC in 90nm CMOS

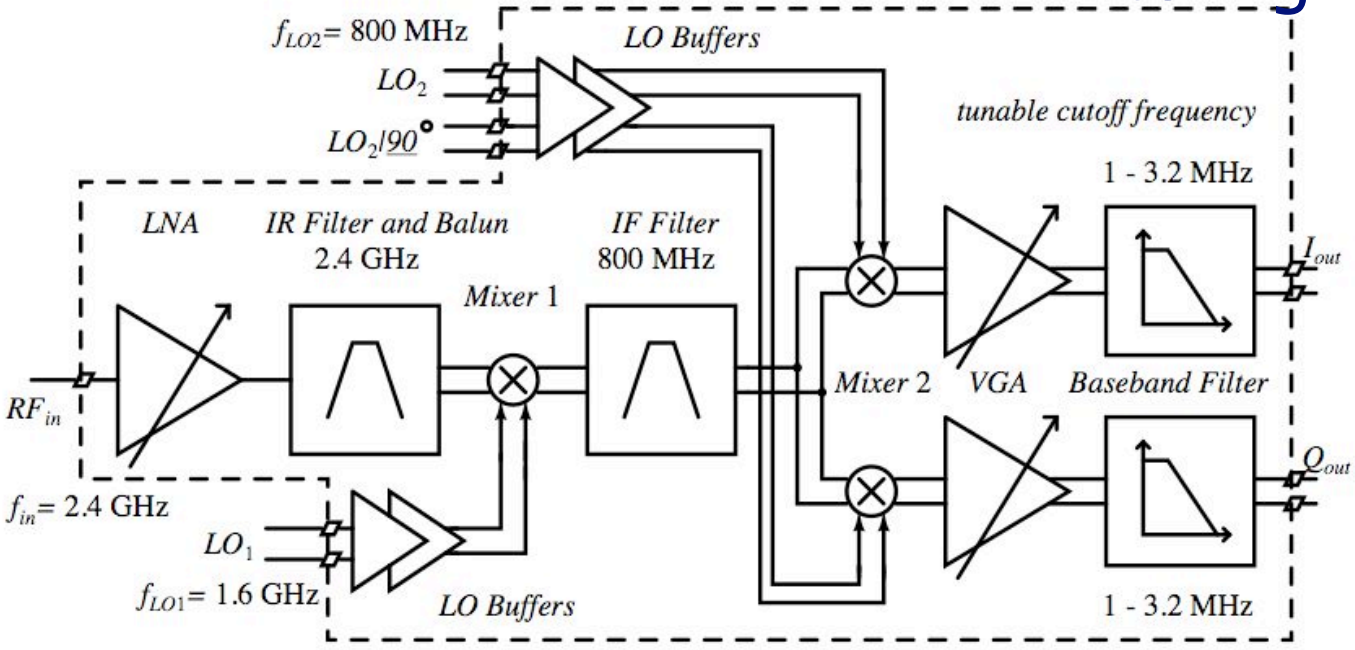


- No internal voltage or clock boosting
- Regular devices
- Cascaded sampling technique to reduce the channel leakage of the switches
- 1.5bit/stage (remark: stages identical, stages scaling not exploited)
- Front-end S/H amplifier eliminated by with an S/H for the sub-ADC.
- 0.5V OTAs with local CMFB
- 90nm CMOS
- [J. Shen & P. Kinget, VLSI07]

A 0.5V 2.4GHz Receiver

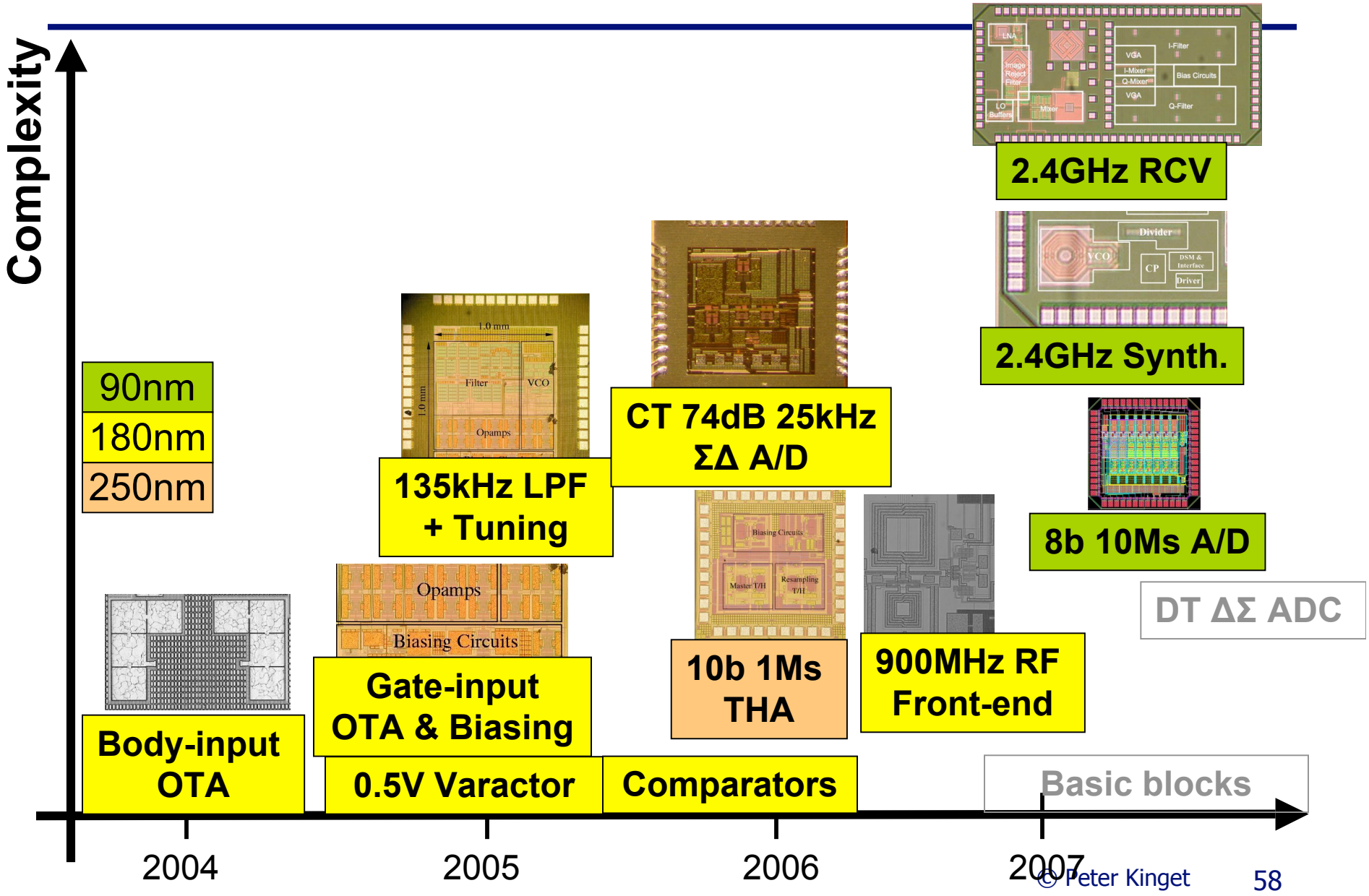


- ISM band applications
- Sliding IF topology
- LNA, Mixers, VGA + on chip RF, IF & BB filtering



[Stanic, Balankutty, Kinget, Tsividis, RFIC07]

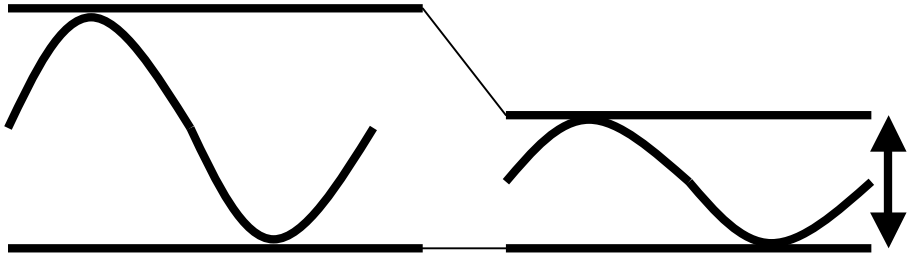
0.5V Analog Roadmap



Where do we go from here…

- Other nanoscale challenges:
  - Gate & subthreshold (OFF) leakage,
  - Smaller g_m/g_o,
  - Reduced body effect.
- Opportunities
  - Device speed significantly improves:
    - Scale device operating points for larger (g_m/I_D),
  - FinFETs, dual gate devices, ….
  - Calibrate using abundant digital gates.
- But, some fundamental limitations are against us…

Power Dissipation Limits



$$V_{DD} = 2\sqrt{2}\,V_{RMS}$$

- Noise limited circuits [Vittoz90]:

$$SNR = \frac{V_{RMS}}{\sqrt{v_{n,RMS}^2}} \qquad \overline{v^2}_{n,RMS} = \frac{kT}{C} \qquad I_{DC} = 2\,f\,C\sqrt{2}V_{RMS}$$

$$P \geq 8\,kT\,f\,SNR^2$$

ideal class B

- Mismatch limited circuits [Kinget96]:

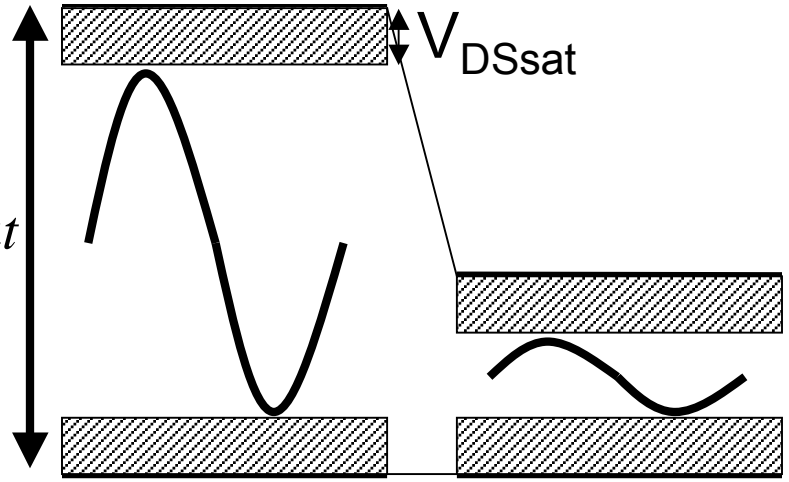
$$Acc = \frac{V_{RMS}}{3\sigma(V_{os})} \qquad \sigma^2(V_{os}) = \frac{C_{ox}A_{VT}^2}{C} \qquad I_{DC} = 2\,f\,C\sqrt{2}V_{RMS}$$

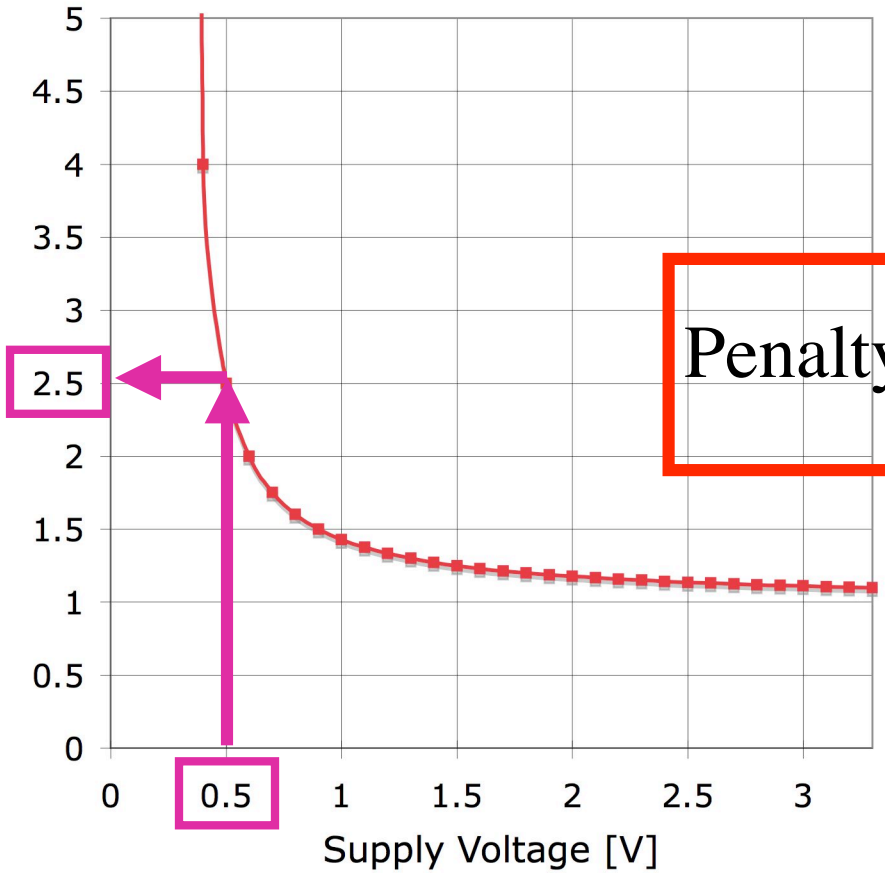
$$P \geq 24\,C_{ox}A_{VT}^2\,f\,Acc^2$$

Low Voltage Power Penalty

- Finite V_{DSsat}:

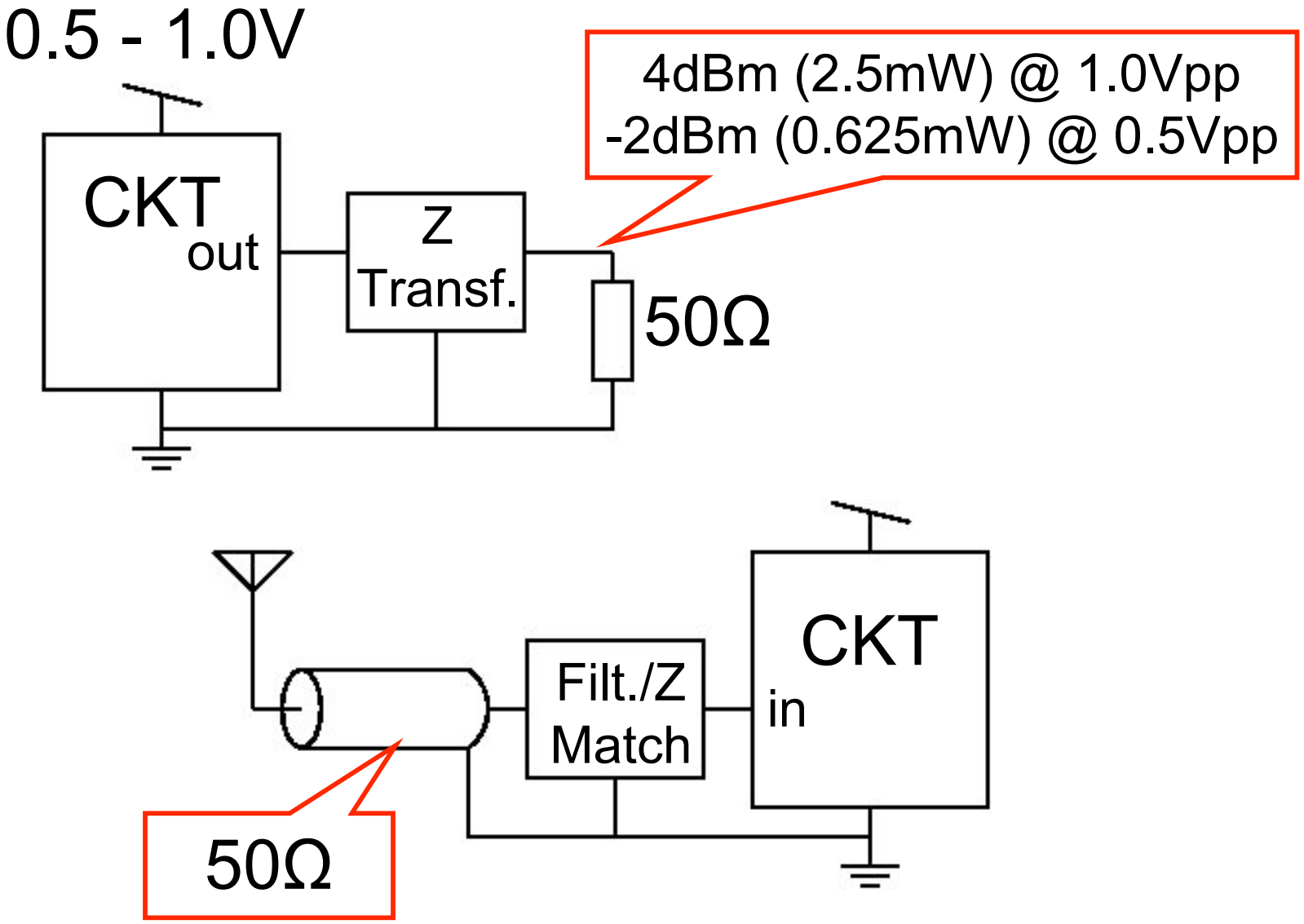
$$V_{DD} = 2\sqrt{2}\,V_{RMS} + 2V_{DSsat}$$





$$\text{Penalty factor} = 1 + \frac{2V_{DSsat}}{(V_{DD} - 2V_{DSsat})}$$

LV Challenge: Interfaces



Ultra Low Voltage Analog Design Techniques

- Device Level:
  - Use body terminal for bias control or signal,
  - Use RSCE, optimize L to reduce V_T.
- Building Block Level:
  - Eliminate transistor stacks,
  - Use LCMFB, CMFF & Neg. G.
- Functional Level:
  - Revise signaling & architecture,
  - New tuning & biasing strategies.
- Demonstrated in 0.5V analog & RF building blocks & systems:
  - filters, THA, ADCs, RF front-ends, freq. synthesizers,
  - in 0.18um CMOS ($|V_T|=V_{DD}$) & 90nm CMOS.

Selection of Recent Publications

0.5V Analog/RF Integrated Circuits:

- S. Chatterjee, K.P. Pun, N. Stanic, Y. Tsividis and P. Kinget, "Analog Circuit Design Techniques at 0.5V", Springer, in press, 2007.
- J. Shen, and P. Kinget, "A 0.5V 8bit 10Msps Pipelined ADC in 90nm CMOS," IEEE Symposium on VLSI circuits, accepted, June 2007.
- N. Stanic, A. Balankutty, P. Kinget, and Y. Tsividis,"A 0.5 V Receiver in 90 nm CMOS for 2.4GHz Applications," IEEE Radio Frequency Integrated Circuits Conference (RFIC), accepted, June 2007.
- S.A. Yu and P. Kinget, "A 0.65V 2.5GHz Fractional-N Frequency Synthesizer in 90nm CMOS" in Digest of Technical Papers IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2007.
- S. Chatterjee, and P. Kinget, "A 0.5-V 1-Msps Track-and-Hold Circuit with 60-db SNDR," IEEE Journal of Solid-State Circuits, vol. 42, no. 4, pp. 722-729, Apr. 2007.
- K.P. Pun, S. Chatterjee, and P. Kinget, "A 0.5-V 74-dB SNDR 25-kHz Continuous-Time Delta-Sigma Modulator with a Return-to-Open DAC," IEEE Journal of Solid-State Circuits, Vol. 42, no 3, pp. 496-507, March 2007.
- N. Stanic, P. Kinget and Y. Tsividis, "A 0.5 V 900 MHz Receiver Front End", IEEE Symposium on VLSI Circuits, June 2006.
- S. Chatterjee, Y. Tsividis and P. Kinget, "0.5 V Analog Circuit Techniques and Their Application in OTA and Filter Design," IEEE Journal of Solid-State Circuits, vol. 40, no 12, pp. 2373 - 2387, Dec. 2005.

RF Integrated Oscillators:

- B. Soltanian, H. Ainspan, W. Rhee, D. Friedman and P. Kinget, "An Ultra Compact Differentially Tuned 6 GHz CMOS LC VCO with Dynamic Common Mode Feedback", IEEE Journal of Solid-State Circuits, in press, 2007.
- B. Soltanian, and P. Kinget, "A Low Phase Noise Quadrature LC VCO Using Capacitive Common-Source Coupling", European Solid-State Circuits Conference, pp. 436-439, Sept. 2006
- F. Zhang and P. Kinget, "Design of Components and Circuits Underneath Integrated Inductors" IEEE Journal of Solid-State Circuits, vol. 41, no. 10, pp. 2265-2271, Oct. 2006.
- B. Soltanian and P. Kinget, "AM-FM Conversion by the Active Devices in MOS LC-VCOs and its Effect on the Optimal Amplitude", IEEE RFIC Symposium, June 2006.
- B. Soltanian and P. Kinget, " Tail Current-Shaping to Improve Phase Noise in LC Voltage Controlled Oscillators " IEEE Journal of Solid-State Circuits, vol. 41, no. 8, pp. 1792-1802, Aug. 2006.

Ultra-wideband Pulse Radio:

- Tien-Ling Hsieh, P. Kinget, Ranjit Gharpurey, "An Approach to Interference Detection for Ultra Wideband Radio Systems", Fifth IEEE Dallas Circuits and Systems Workshop, pp. 91-94, Oct. 2006.
- F. Zhang and P. Kinget, "Low Power Programmable Gain CMOS Distributed LNA" IEEE Journal of Solid-State Circuits, vol. 41, no 6, pp. 1033-1043, June 2006.
- A. Jha, R. Gharpurey and P. Kinget, "Quadrature-DAC based pulse generation for UWB pulse radio transceivers" in Digest of Technical Papers IEEE International Symposium on Circuits and Systems, pp. 666-669, May 2006.

Injection-locking:

- G. Gangasani and P. Kinget, "A time-domain model for predicting the injection locking bandwidth of non-harmonic oscillators" in Transactions on Circuits and Systems II, pp. 1035-1038, Oct. 2006.
- G. Gangasani and P. Kinget, "Injection-Lock Dynamics in Non-Harmonic Oscillators" in Digest of Technical Papers IEEE International Symposium on Circuits and Systems, pp. 1675-1678, May 2006.

Device Mismatch:

- P. Kinget, "Device mismatch and Tradeoffs in the Design of Analog Circuits", IEEE Journal of Solid-State Circuits, vol. 40, no 6, pp. 1212-1224, June 2005.

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  - Y. Tsividis (Columbia), K. P. Pun (City Univ. Hong Kong), S. Chatterjee (now IIT Delhi), B. Soltanian (now LSI)
  - A. Balankutty, Y. Feng, A. Jha, J. Shen, N. Stanic, S. Yu, F. Zhang.
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Thank you for your attention

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