0.5V Analog Integrated Circuits

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Analog, Digital, Mixed-Mode and RF Integrated Circuits

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Analog, Mixed Signal and RF Integrated Circuit Design Research

Ultra-low voltage circuits: 0.5V

RF integrated oscillators

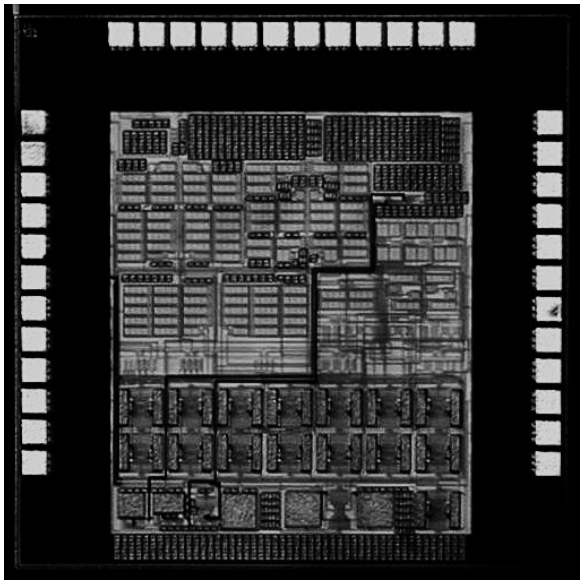
Ultra-wideband RF circuits

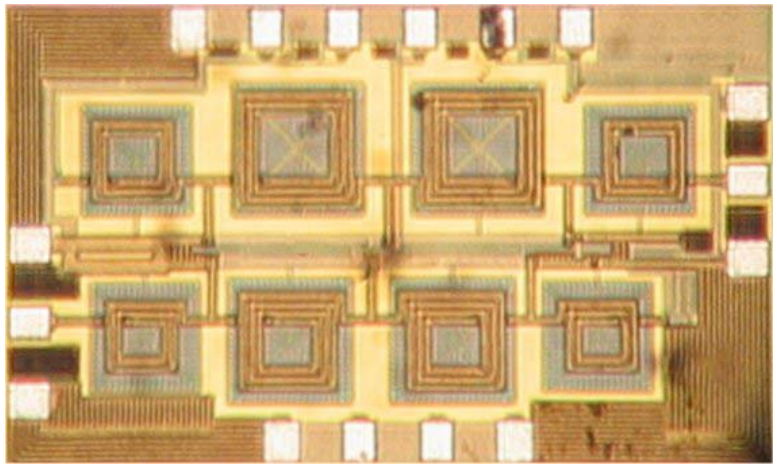
Injection locked circuits

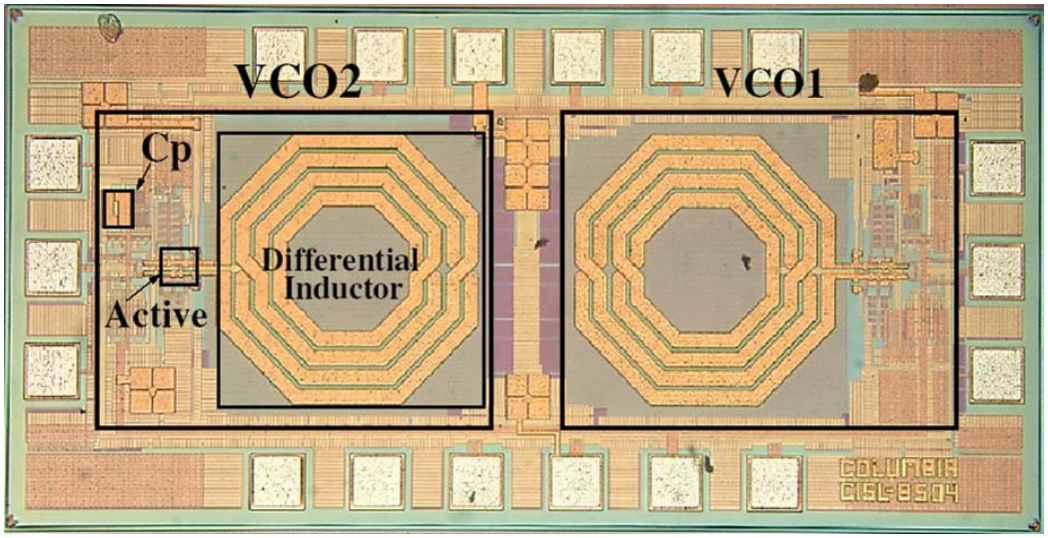
Device mismatch & its influence on Analog & RF ics

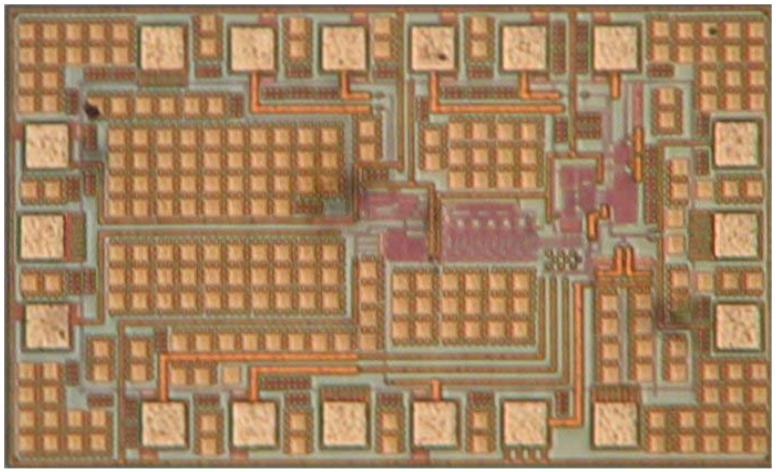
Biological Interfaces

Sample of Recent Chips







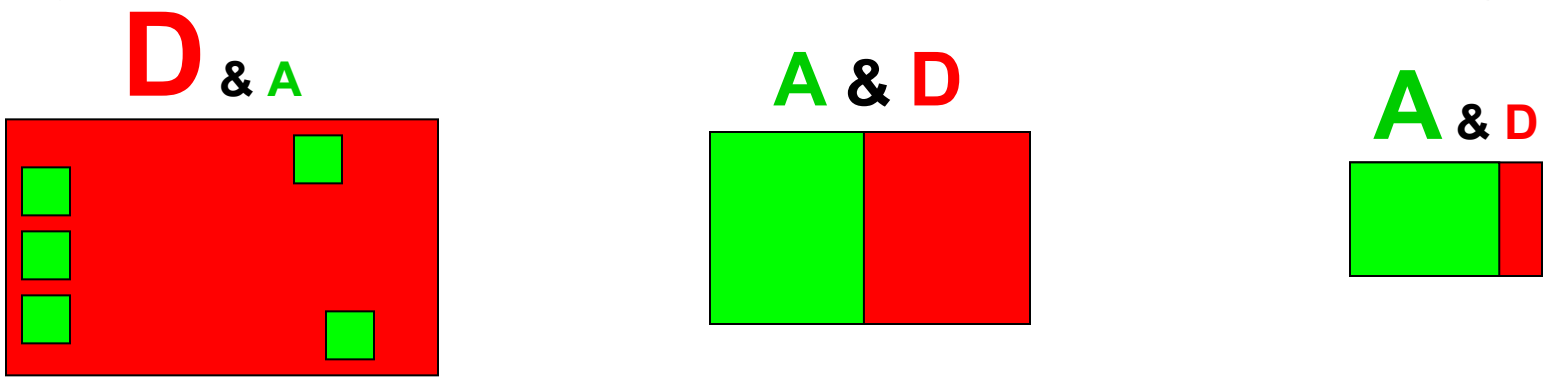


Outline

- Why 0.5 V Analog Integrated Circuits?
- Design Challenges & Opportunities at 0.5 V.
- 0.5 V Operational Transconductance Amplifiers.
- 0.5 V Biasing circuits.
- 0.5 V Fully Integrated Active RC filter with on-chip automatic tuning.
- Conclusions.

Analog in a *Mixed Signal World*

- Sounds, images, EM waves, …. are ANALOG.
- Information processing & storage are DIGITAL.
- System-on-chip is powerful economic paradigm.

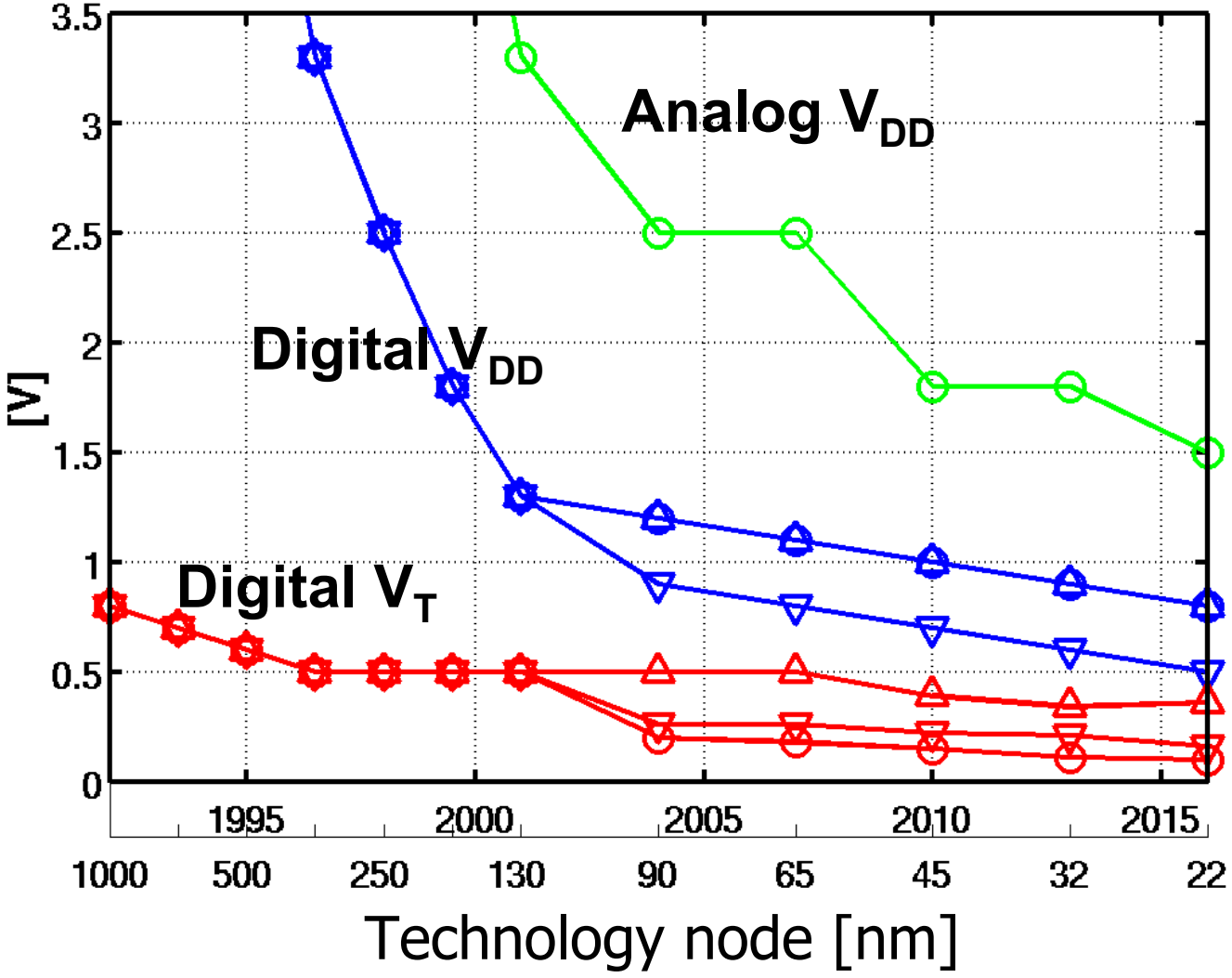


- Digital drives technology development & choice.

If Analog can be done in a digital technology, it will be done.

Most Digital ICs need some Analog!

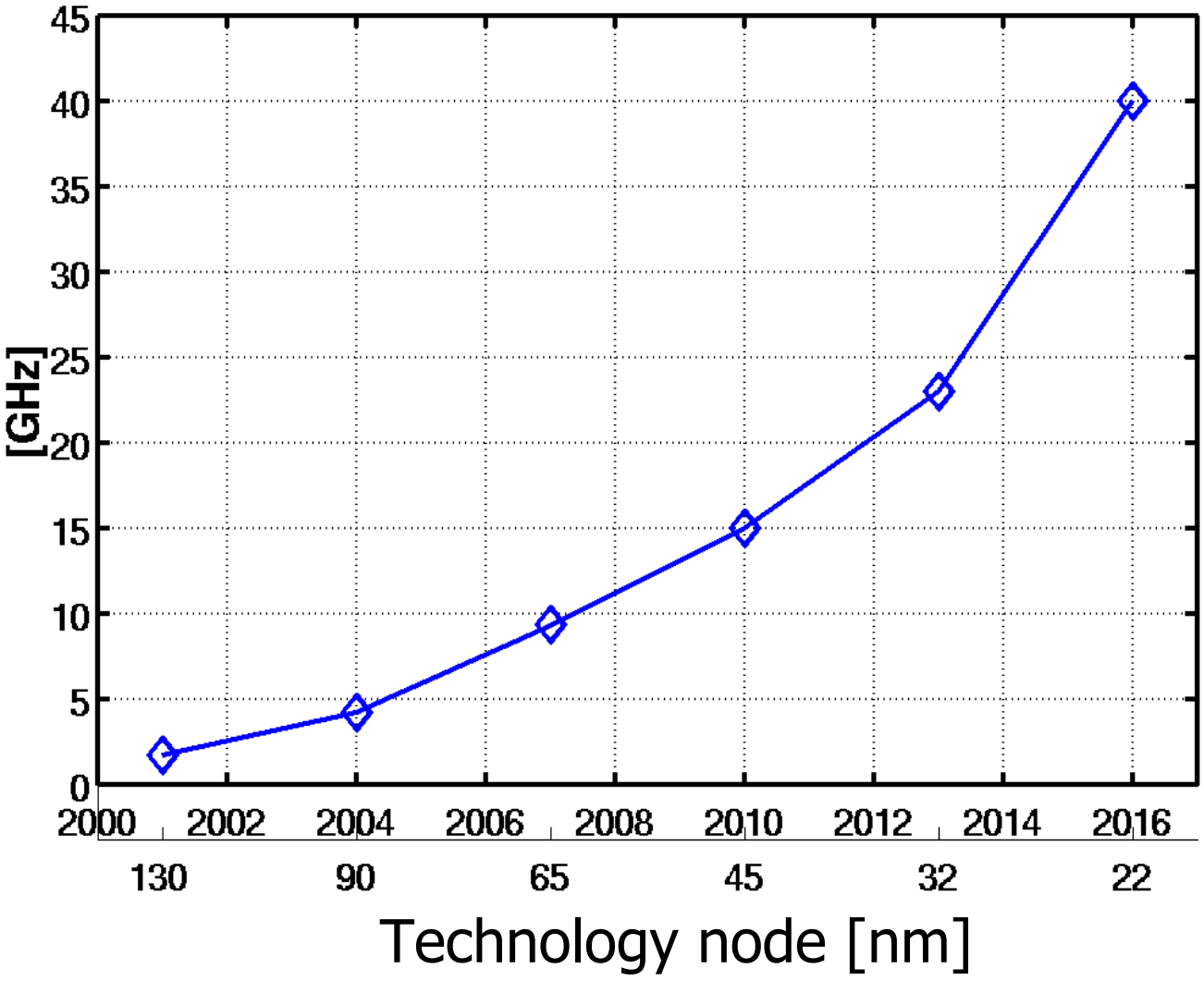
CMOS Trends: Supply Voltage



[ITRS'04]

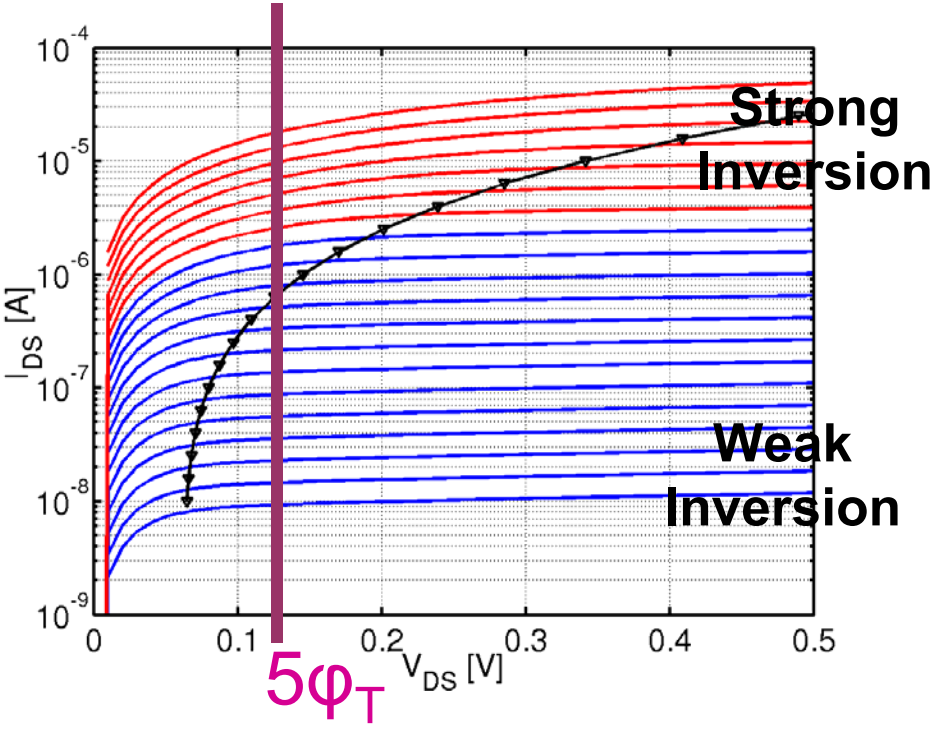
–O– High Perf.
–Δ– Low Standby
–V– Low Power

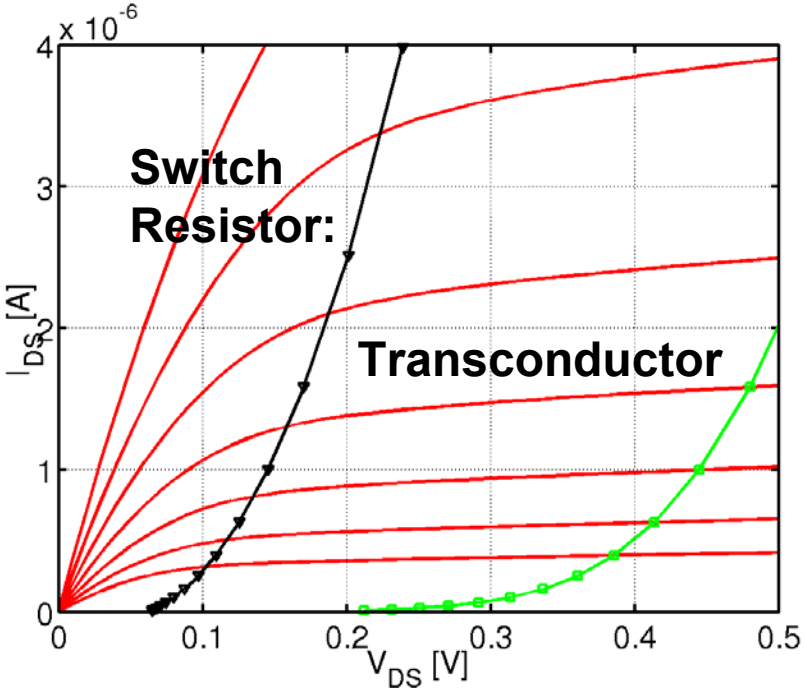
CMOS Trends: On chip Clock Speed



[ITRS'04]

MOS transistor

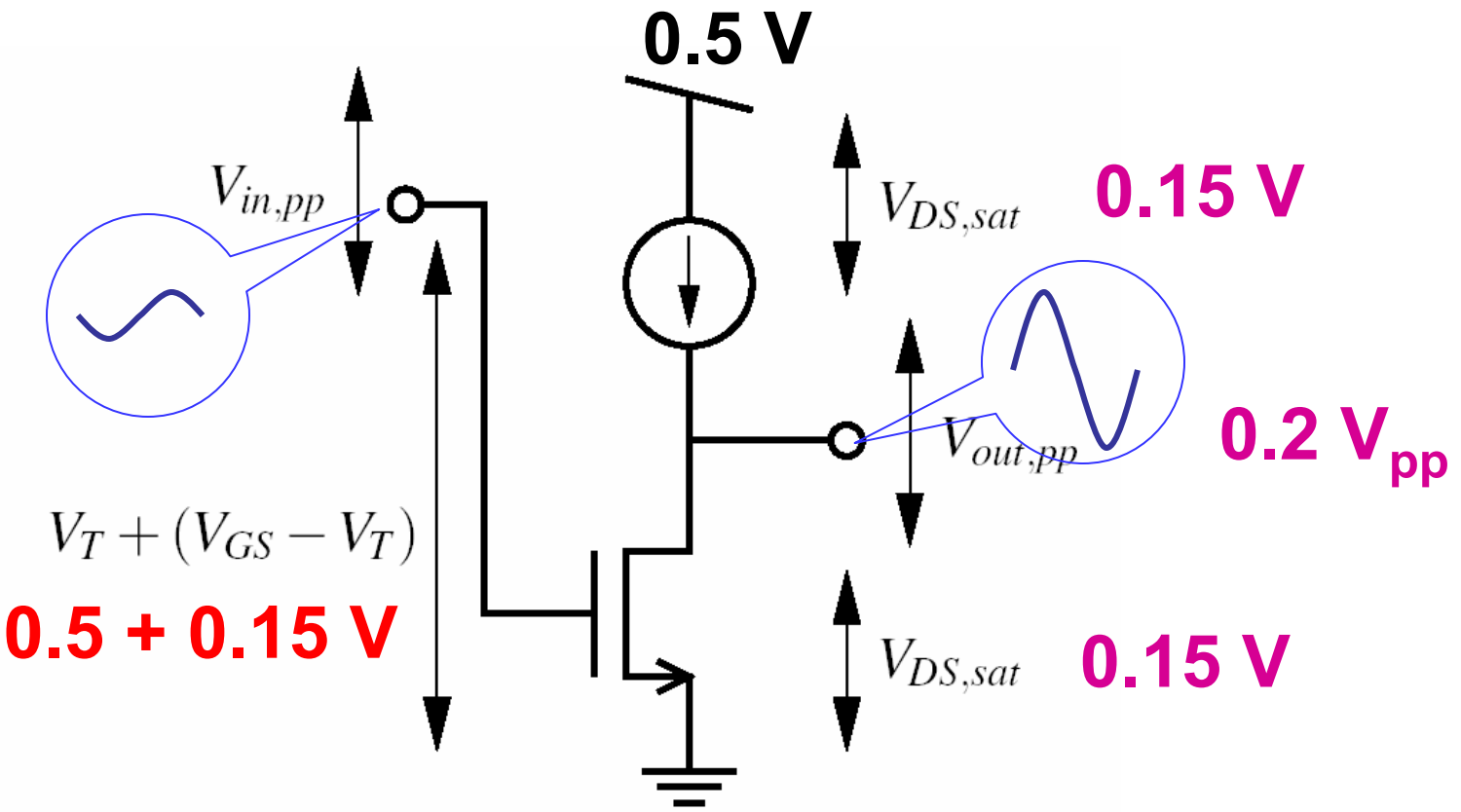




- Transconductor or Current Source
  $V_{DS} > 0.15V$ (for $V_{GS}-V_T \leq 0.2$)
- Switch/Resistor
  only for very small signal range !?

0.24µm/0.36µm nMOS in 0.18µm CMOS

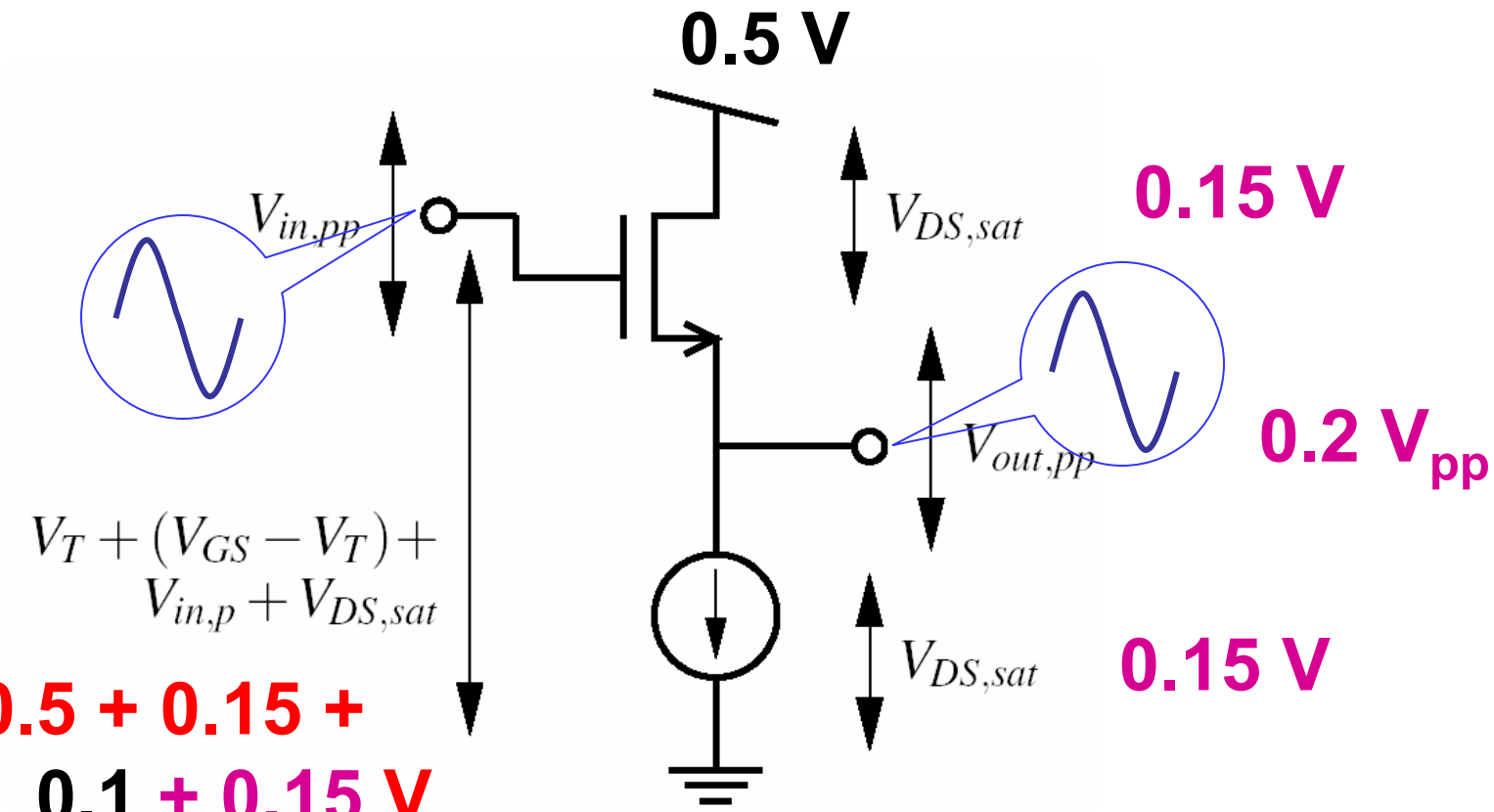
Common Source Amplifier



V_T= 0.5 V

$V_{DS,sat}$= 0.15 V

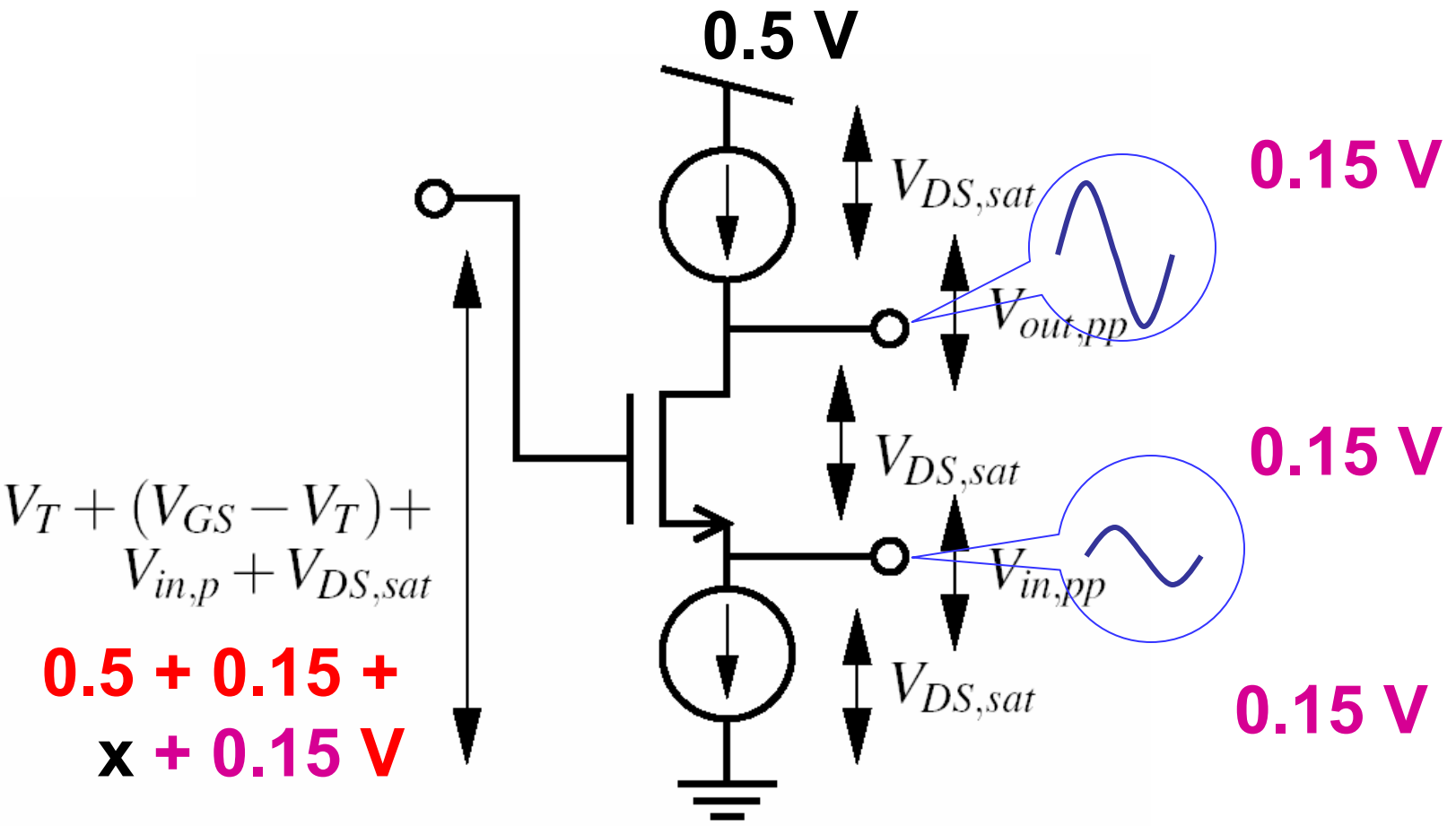
Common Drain Buffer



V_T= 0.5 V

$V_{DS,sat}$= 0.15 V

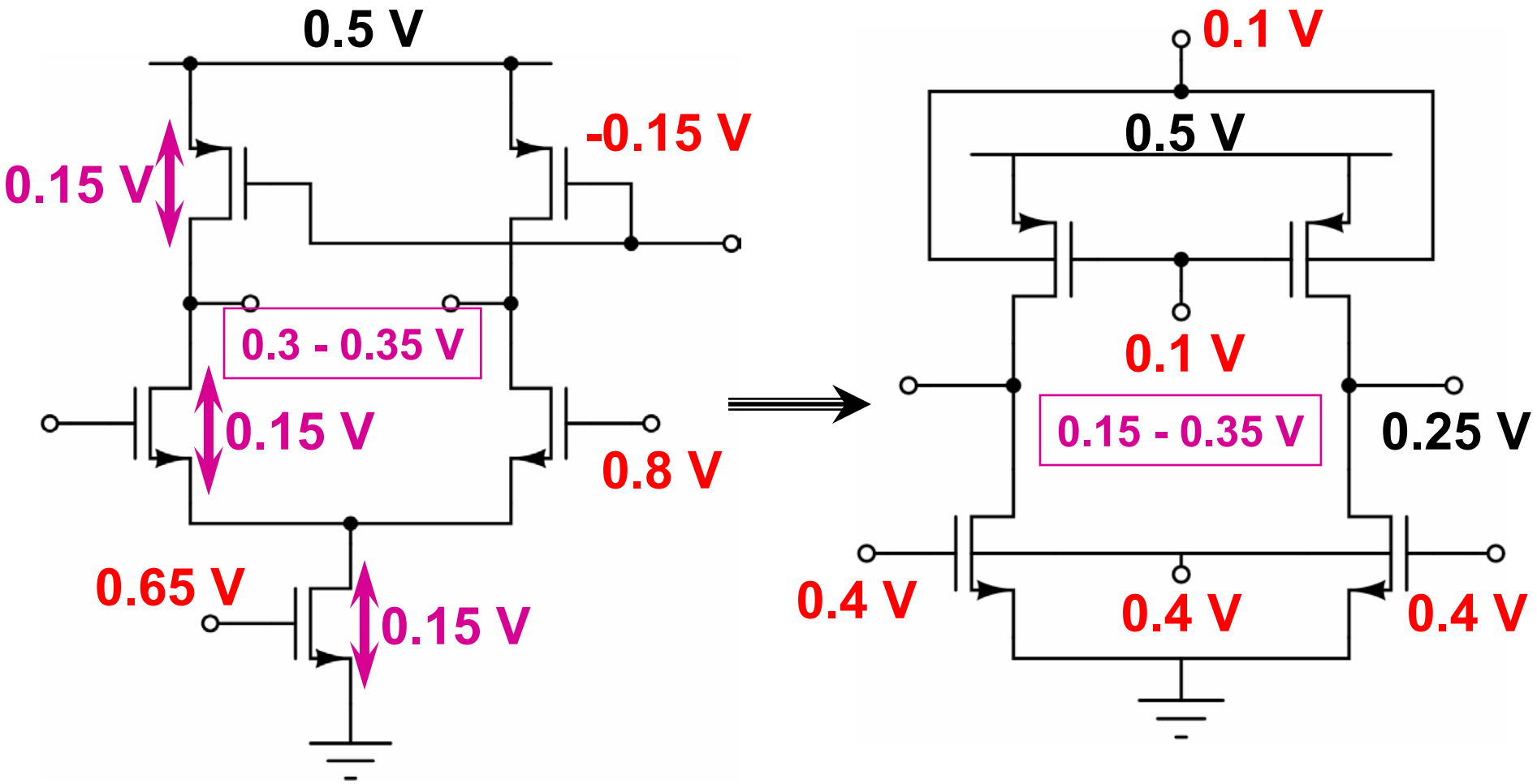
Common Gate Amplifier / Cascode



V_T= 0.5 V

$V_{DS,sat}$= 0.15 V

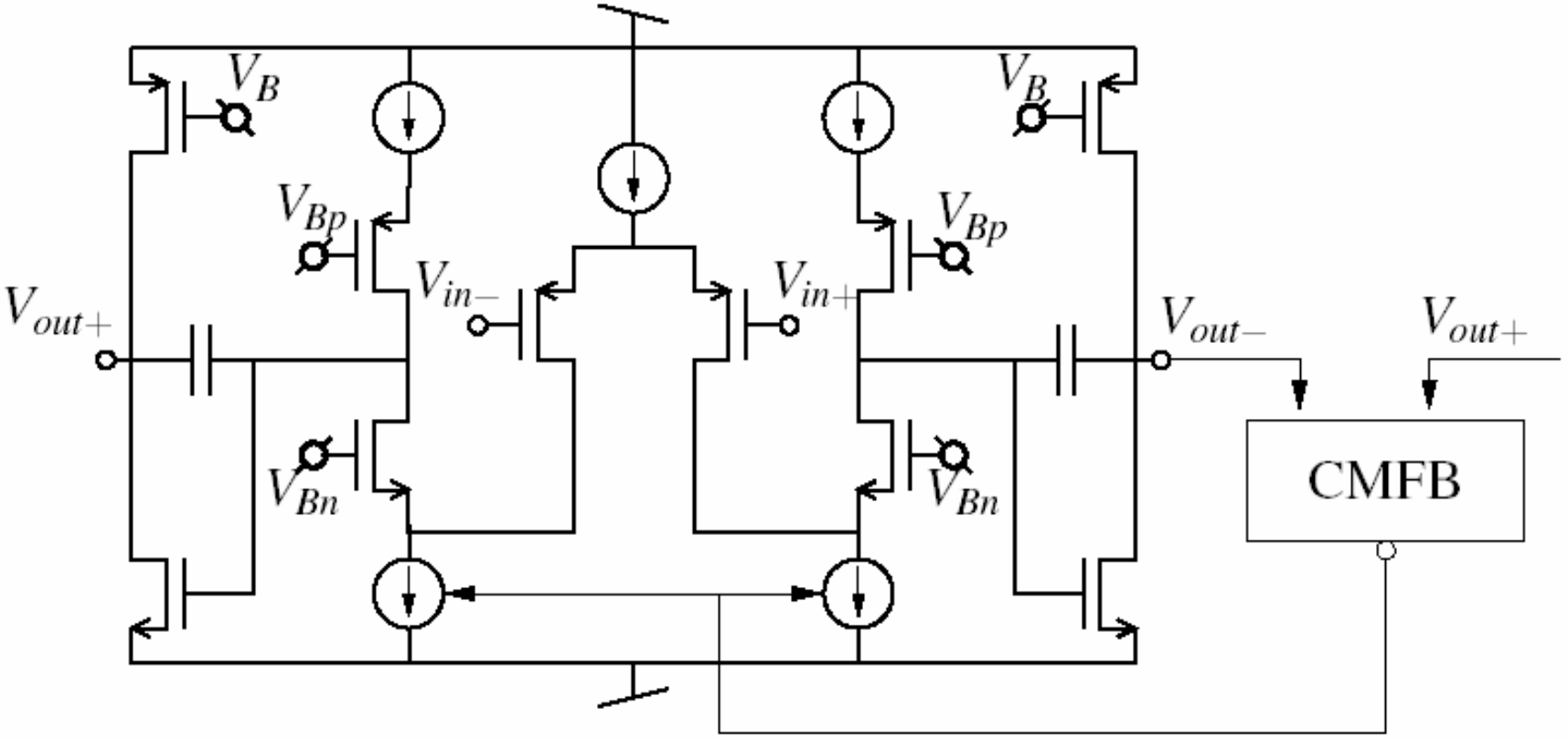
Differential OTA design challenges



$V_T = 0.5$ V

$V_{DS,sat} = 0.15$ V

CMFB in Folded Cascode OTA



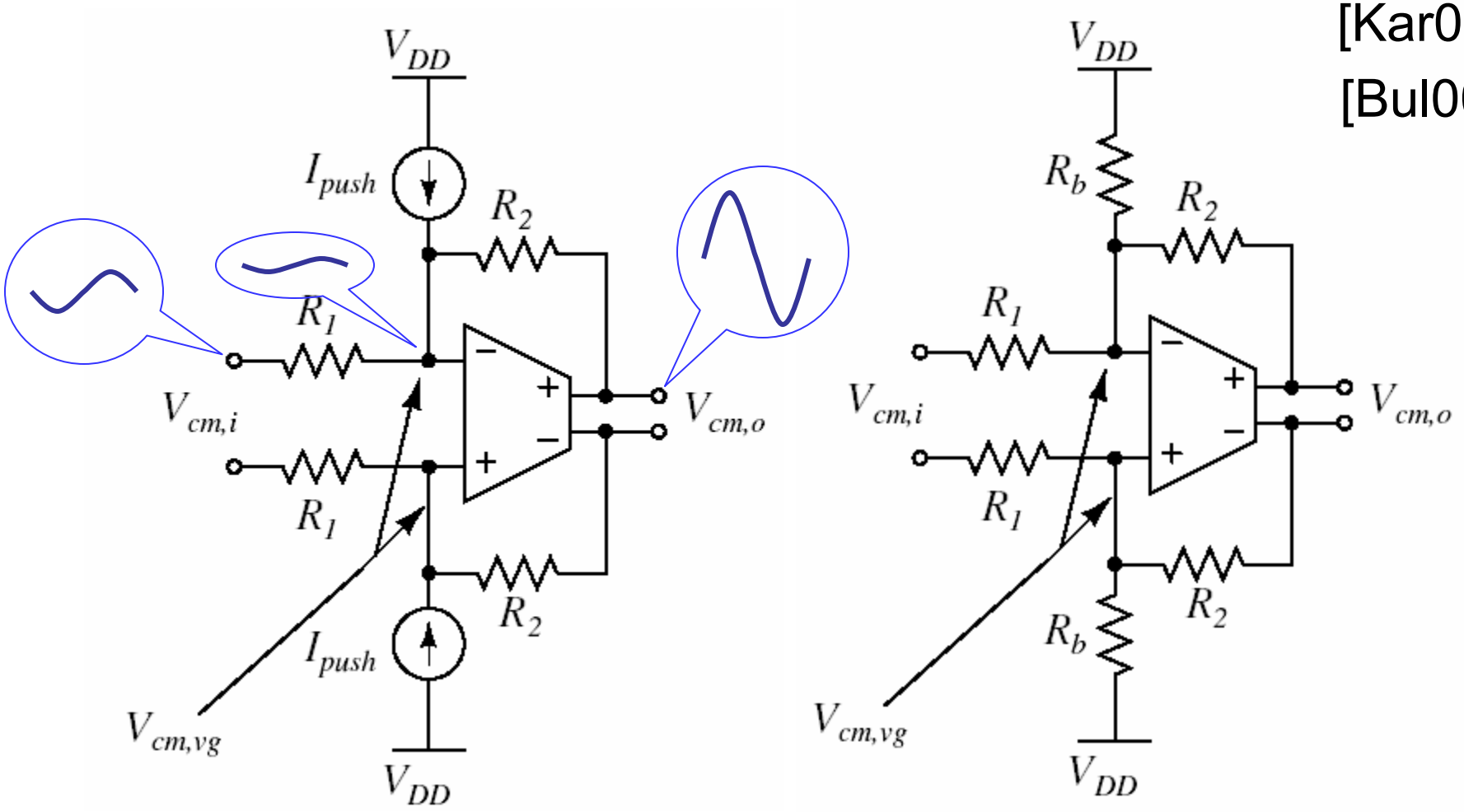
Common Mode Feedback requires 'fast' amplifier operating from $V_{out,CM} = V_{DD}/2$!?

Challenges at 0.5 V

- $V_{DS,sat}$ related challenges:
  - *Independent* of region of operation!
  - *Independent* of V_T!
  - Signal swings are limited.
  - Avoid transistor stacks.
- V_{GS} related challenges:
  - *Depend* on region of operation & $(V_{GS}-V_T)$.
  - *Depend* on V_T!
  - Avoid signal swing on gate.

‘Feedback to the rescue’

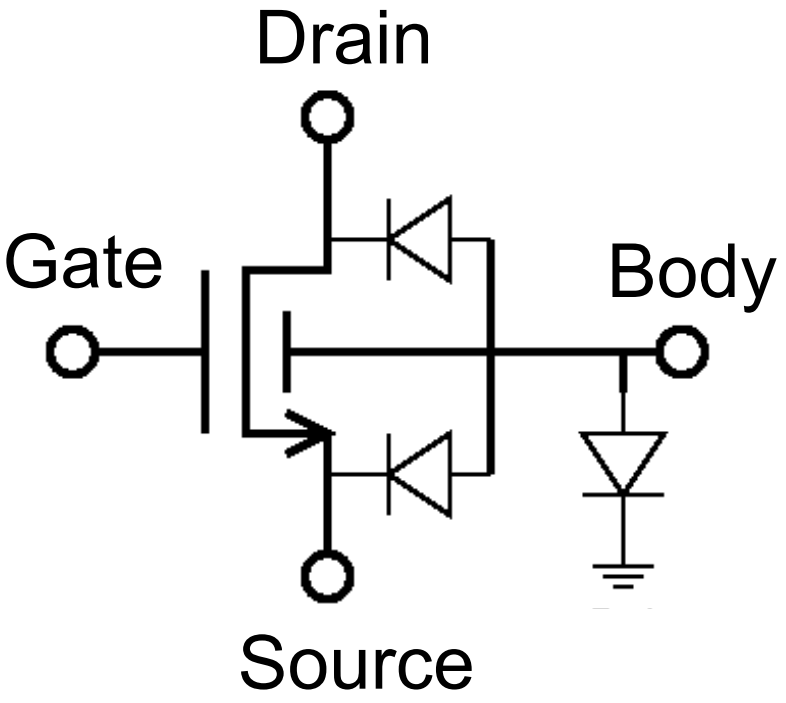
[Kar00]
[Bul00]

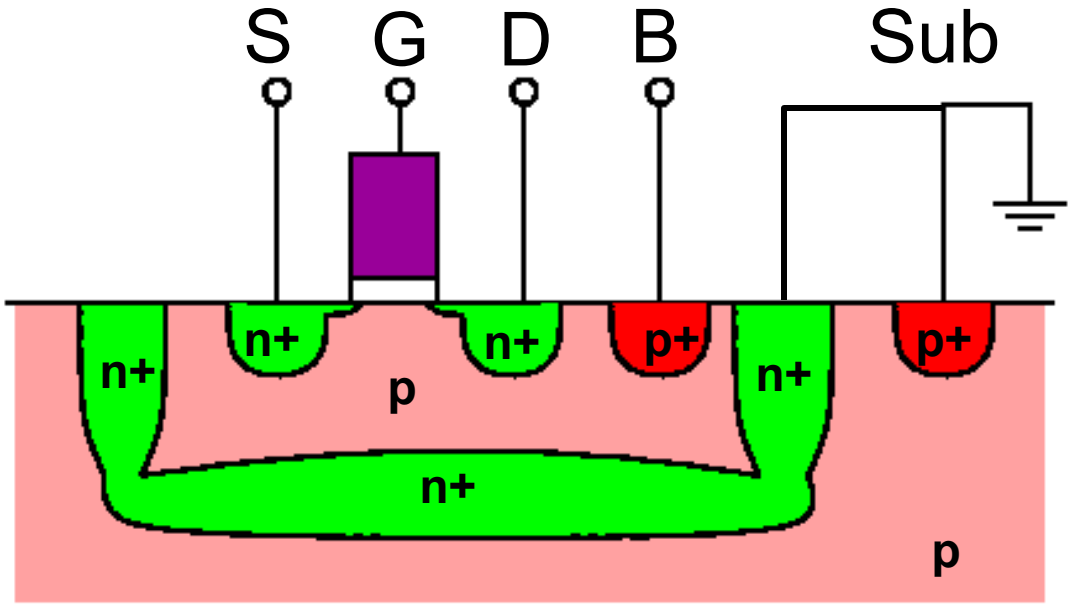


CM @ OTA-in > CM @ input and output

Opportunities at 0.5 V: MOS 4-terminal device

nMOS circuit equivalent (deep n-well process)

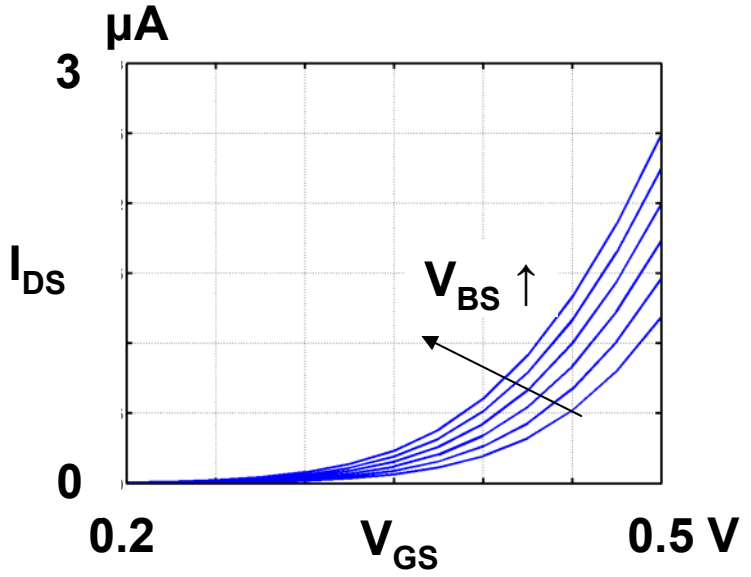


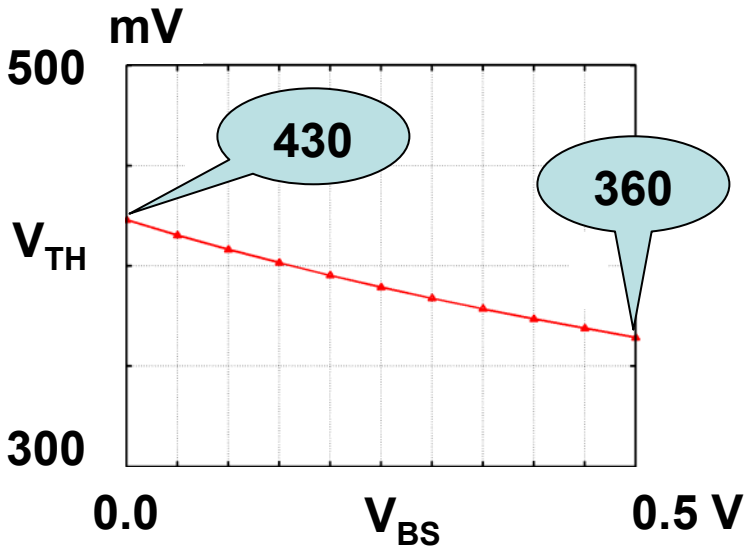


nMOS cross section (deep n-well process)

Opportunities at 0.5 V

- Body terminal
  - Signal input: [Guz87]
  - V_{TH} reduction & control [Kob94], [Von94]
  - Bias control
- Latch-up not an issue
  - Assuming V_{DD} and GND are 'well behaved'.
- Techniques can be ported to 'double gate' devices

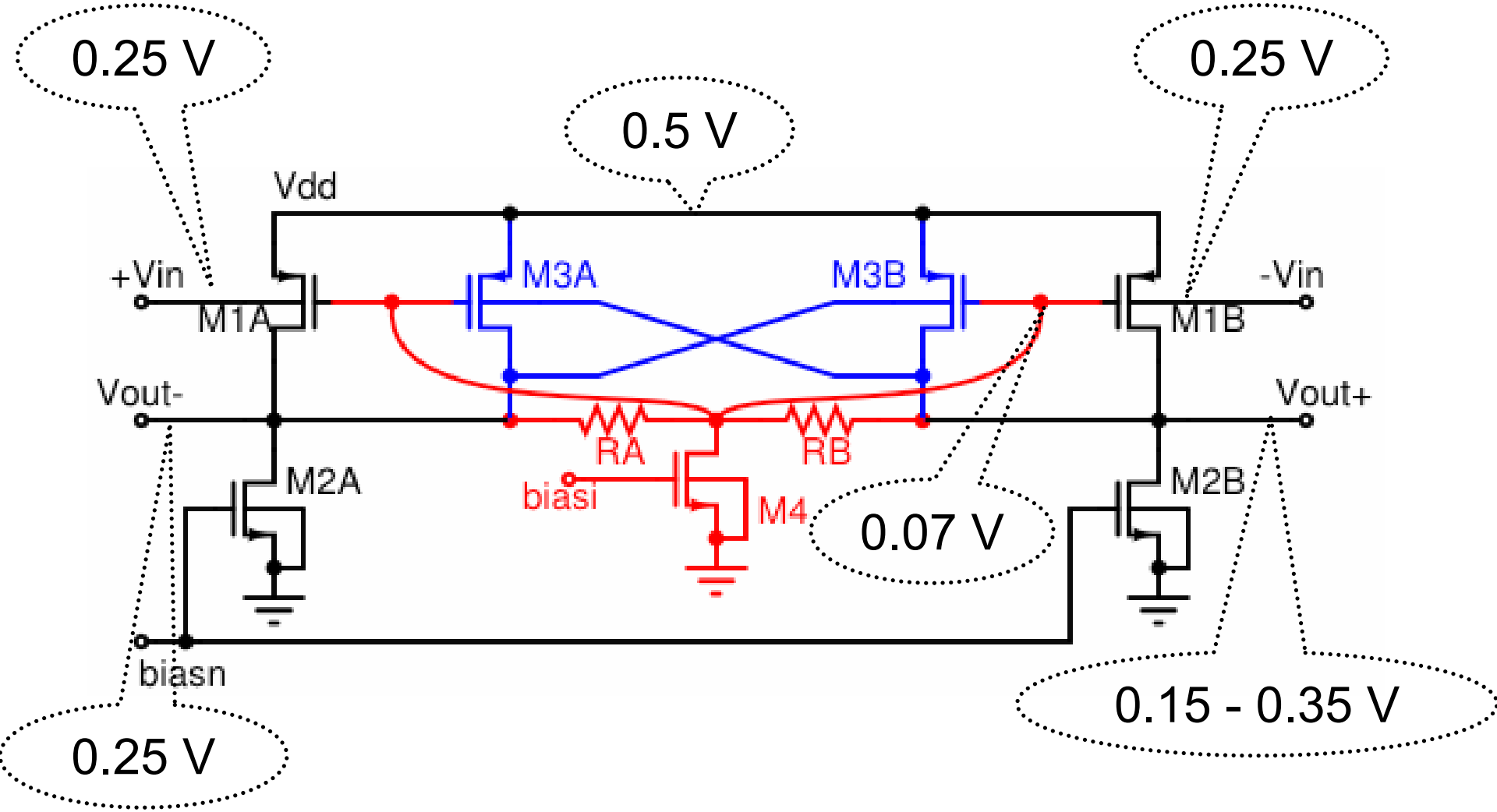




0.24µm/0.36µm nMOS in 0.18µm CMOS

0.5 V Body-input OTA

Low-voltage differential-gain stage



Single-stage gain, CMRR

$$A_{\text{diff}} = \frac{g_{mb_1}}{g_{ds_1} + g_{ds_3} + g_{ds_2} + 1/R - g_{mb_3}} \approx 25 \text{ dB}$$

$$A_{\text{cm}} = \frac{g_{mb_1}}{g_{ds_1} + g_{ds_3} + g_{ds_2} + g_{mb_3} + g_{m_1} + g_{m_3}} \approx -11 \text{ dB}$$

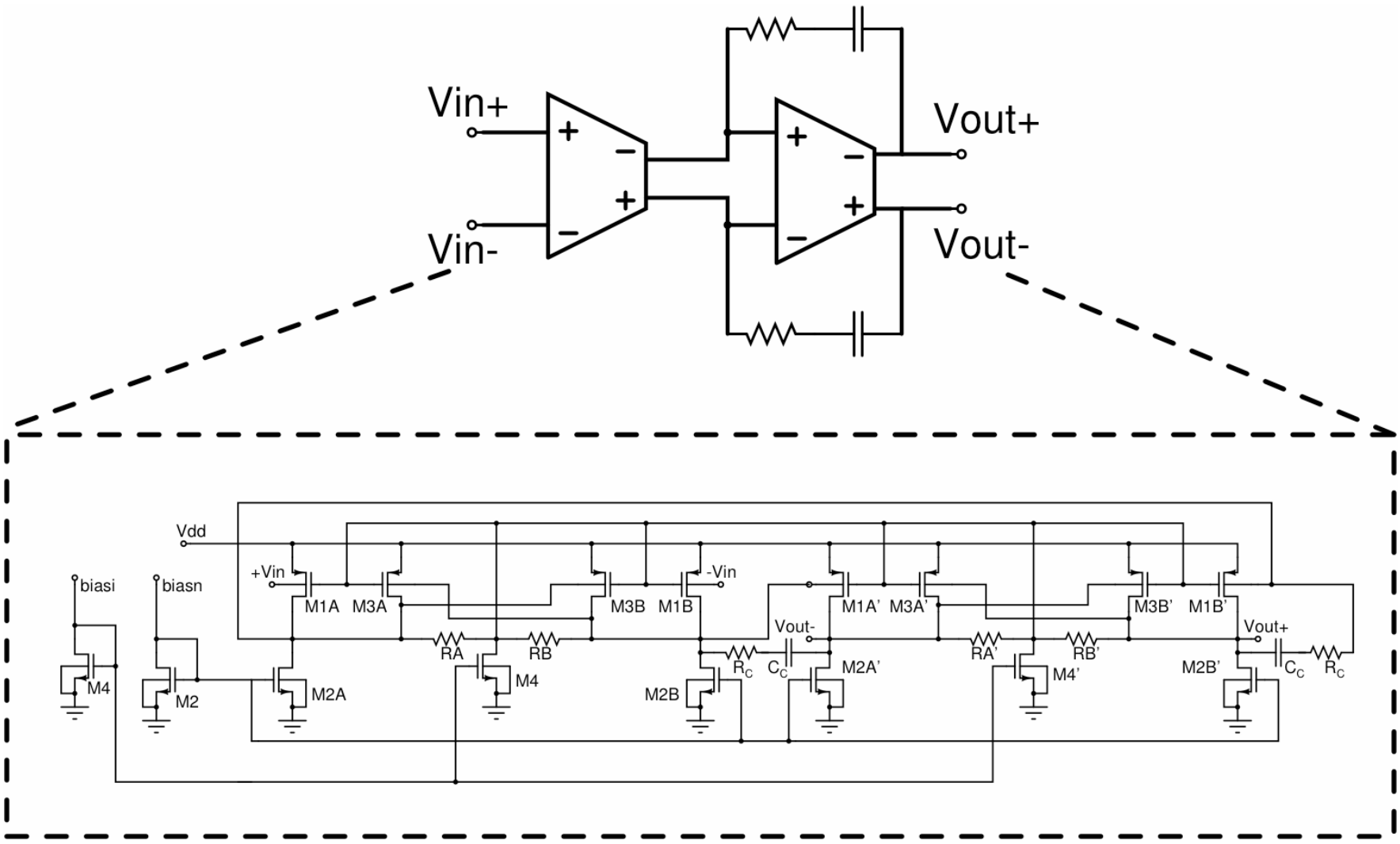
Differential mode load: g_{ds}

Common mode load: $(g_{m1} + g_{m3})$

$$\Longrightarrow \text{CMRR} \approx 36 \text{ dB/stage}$$

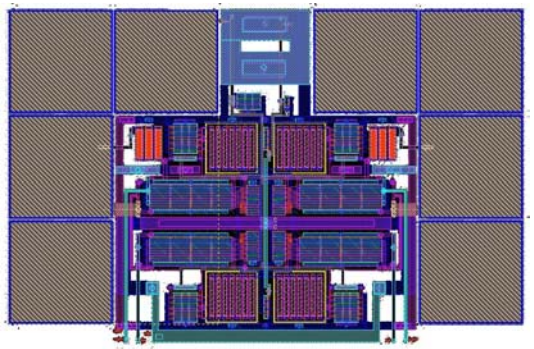
$$\Longrightarrow \text{A}_{\text{diff}} \approx 25 \text{ dB/stage}$$

Two-stage fully-differential OTA

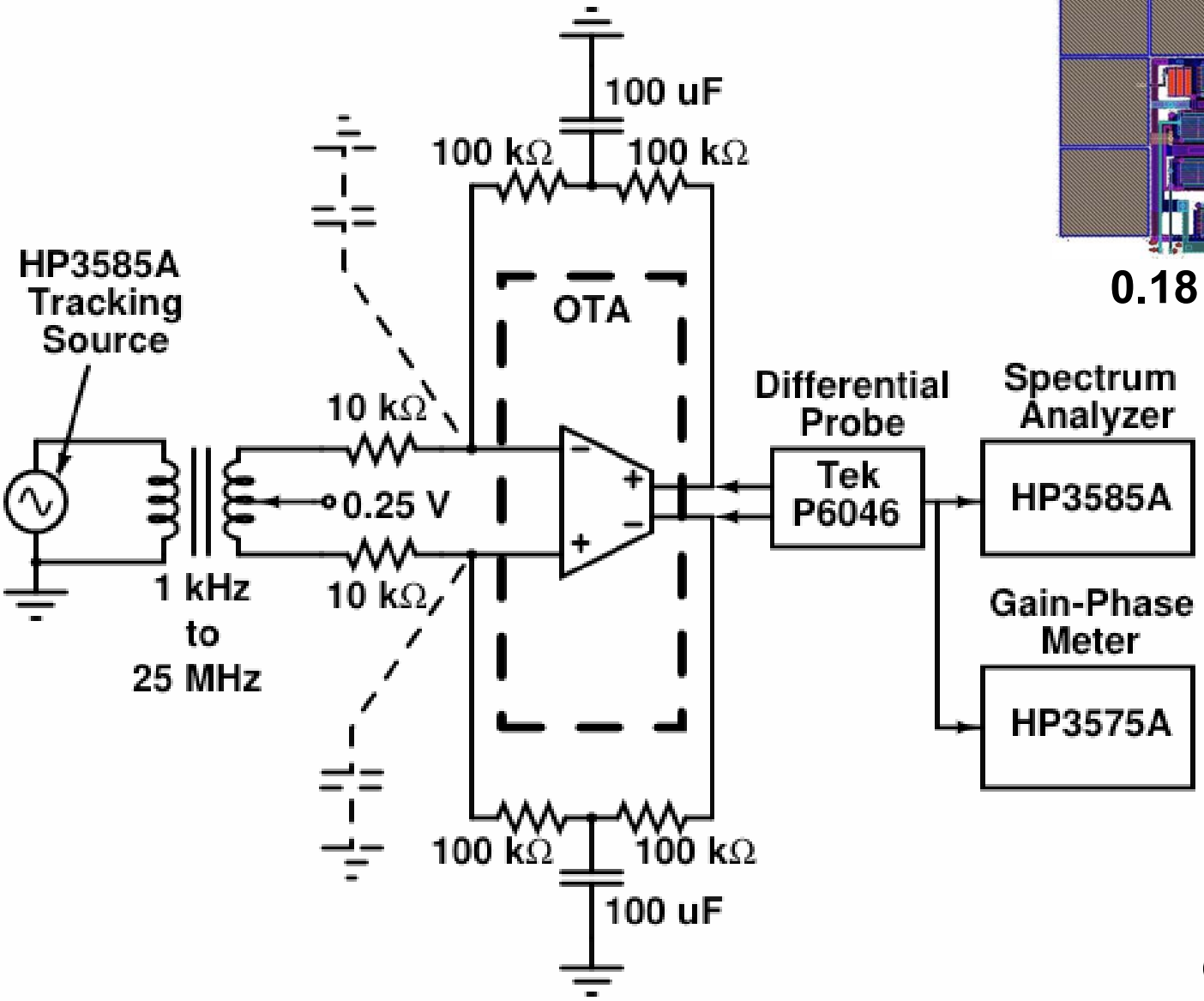


Pole splitting using Miller capacitor

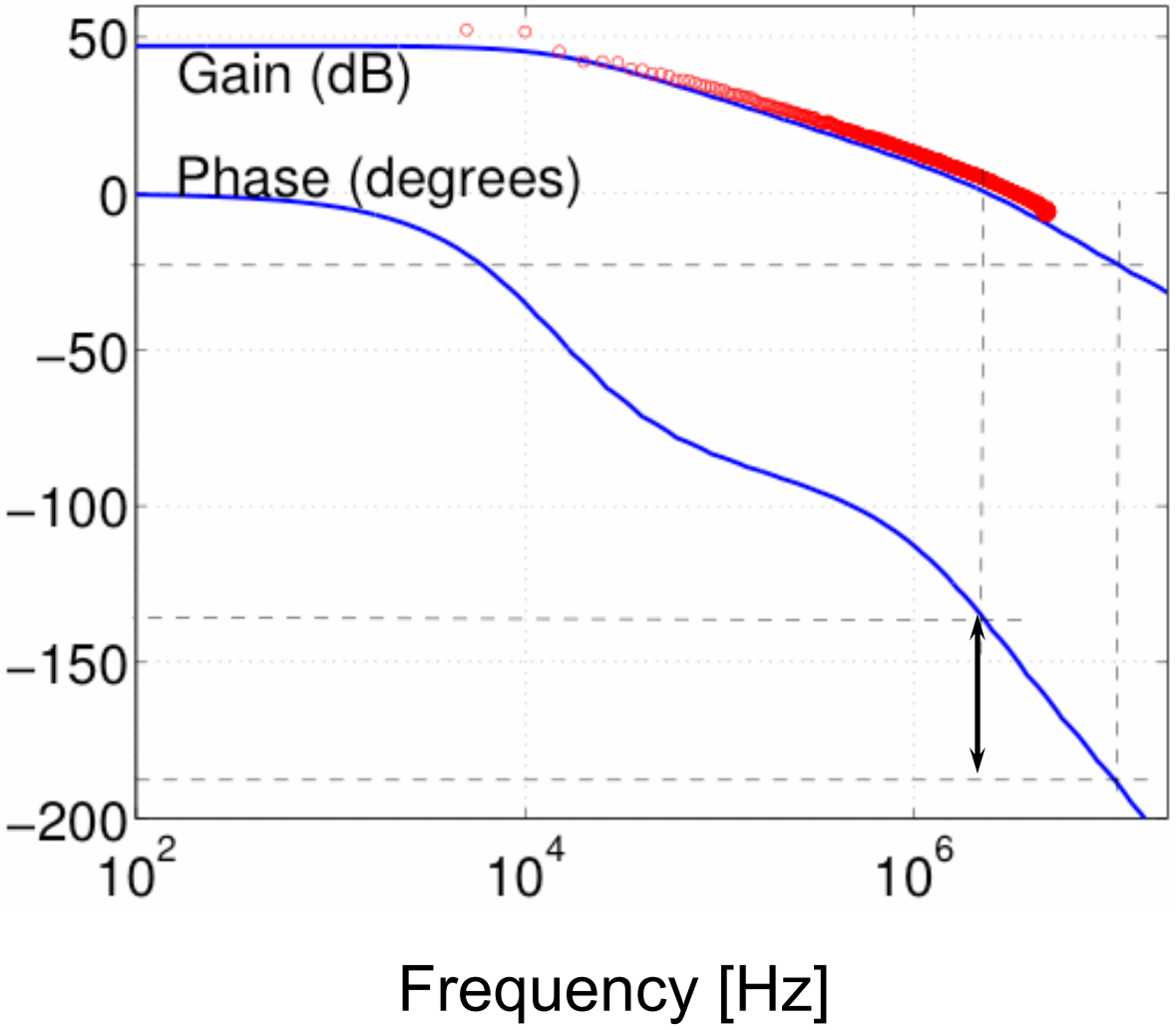
Setup for open-loop measurements



0.18 μm CMOS



Open loop frequency response



DC gain: 52 dB

GBW: 2.5 MHz

Measurement

Simulation

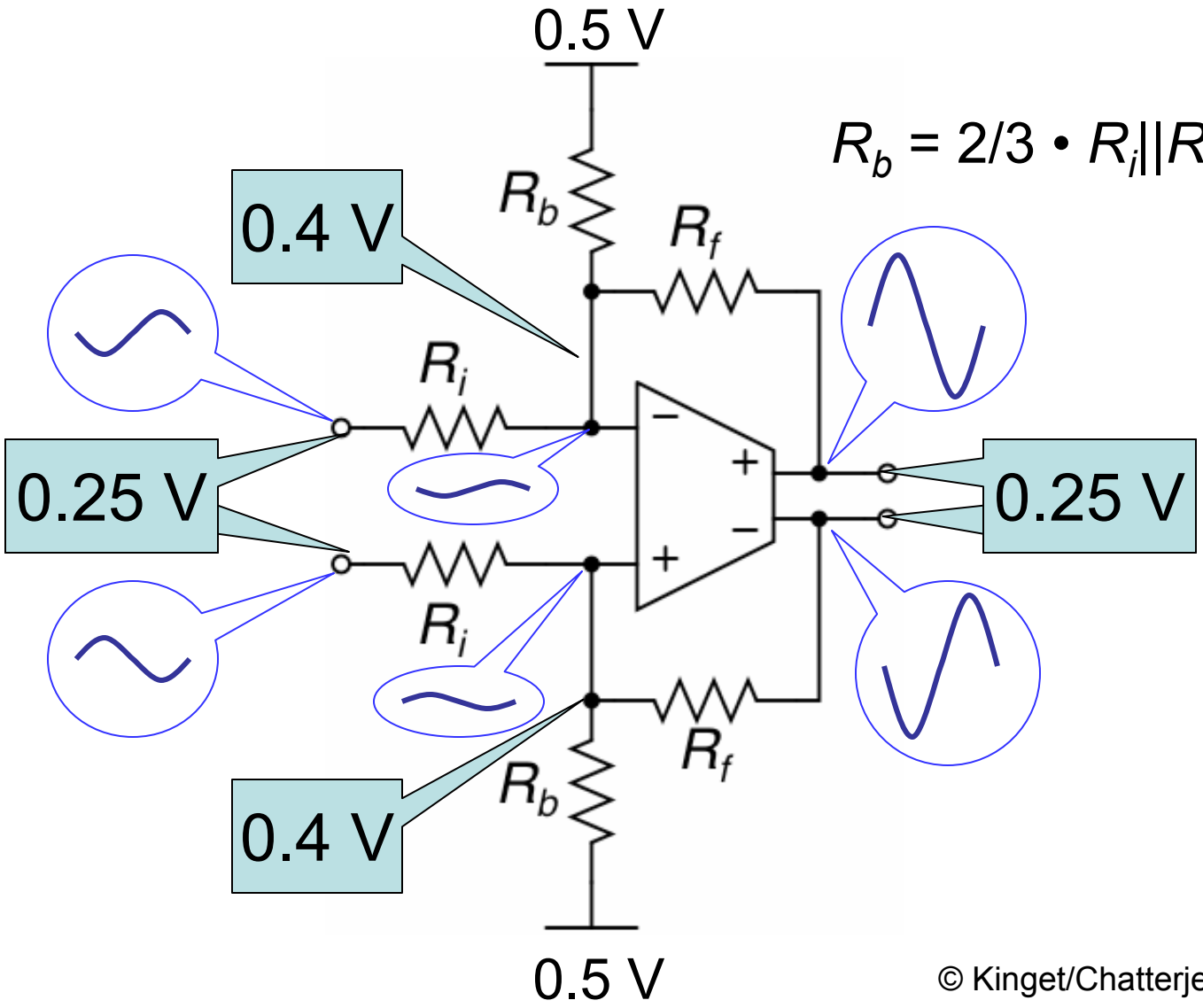
Phase Margin: 45^0

Bulk-input OTA performance

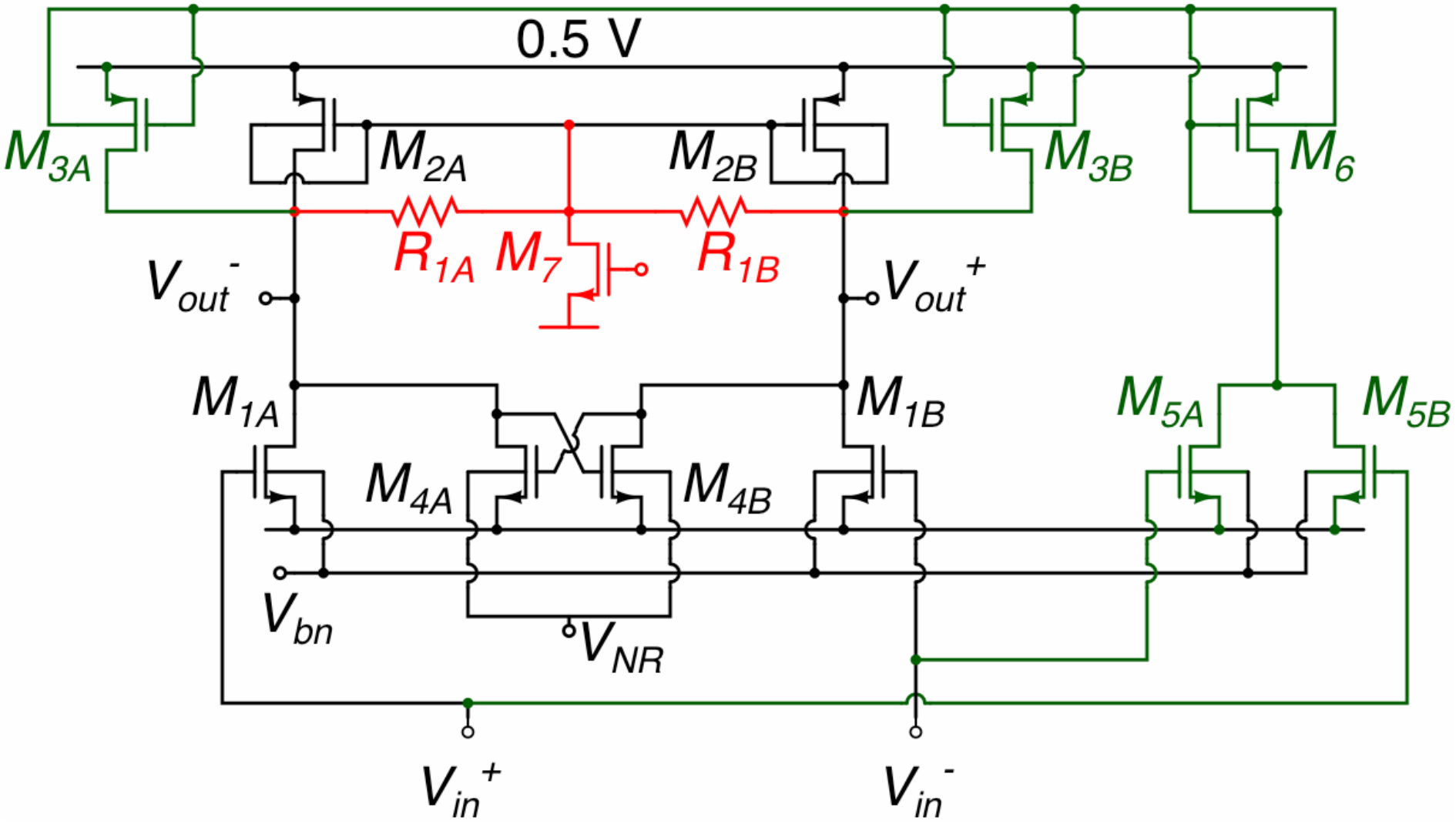
	Parameter	Measured	Simulated
	Area	0.026 sq mm	
Open loop	Supply voltage	0.5 V	0.5 V
Open loop	Load cap.	20 pF	20 pF
Open loop	Power dissipation	110 μW	100 μW
Open loop	Open-loop dc gain	52 dB	48 dB
Open loop	Open-loop unity-gain BW	2.5 MHz	2.4 MHz
Open loop	Input current @ 27^o C	$<$ 1 nA	0.25 nA
Open loop	Slew Rate	2.89 V/μsec	2.92 V/μsec
Closed loop	Closed-loop unity-gain BW	2.2 MHz	2.0 MHz
Closed loop	CMRR @ 5 kHz	78 dB	78 dB
Closed loop	PSRR @ 5 kHz	76 dB	NA
Closed loop	Input ref. noise @ 10 kHz	280 nV/$\sqrt{\text{Hz}}$	220 nV/$\sqrt{\text{Hz}}$
Closed loop	Input ref. noise @ 1 MHz	80 nV/$\sqrt{\text{Hz}}$	90 nV/$\sqrt{\text{Hz}}$
Closed loop	Output amp. (diff) for 1% HD_3	400 mV p-p	
Closed loop	Output clipping level (diff)	520 mV p-p	

0.5 V Gate-input OTA

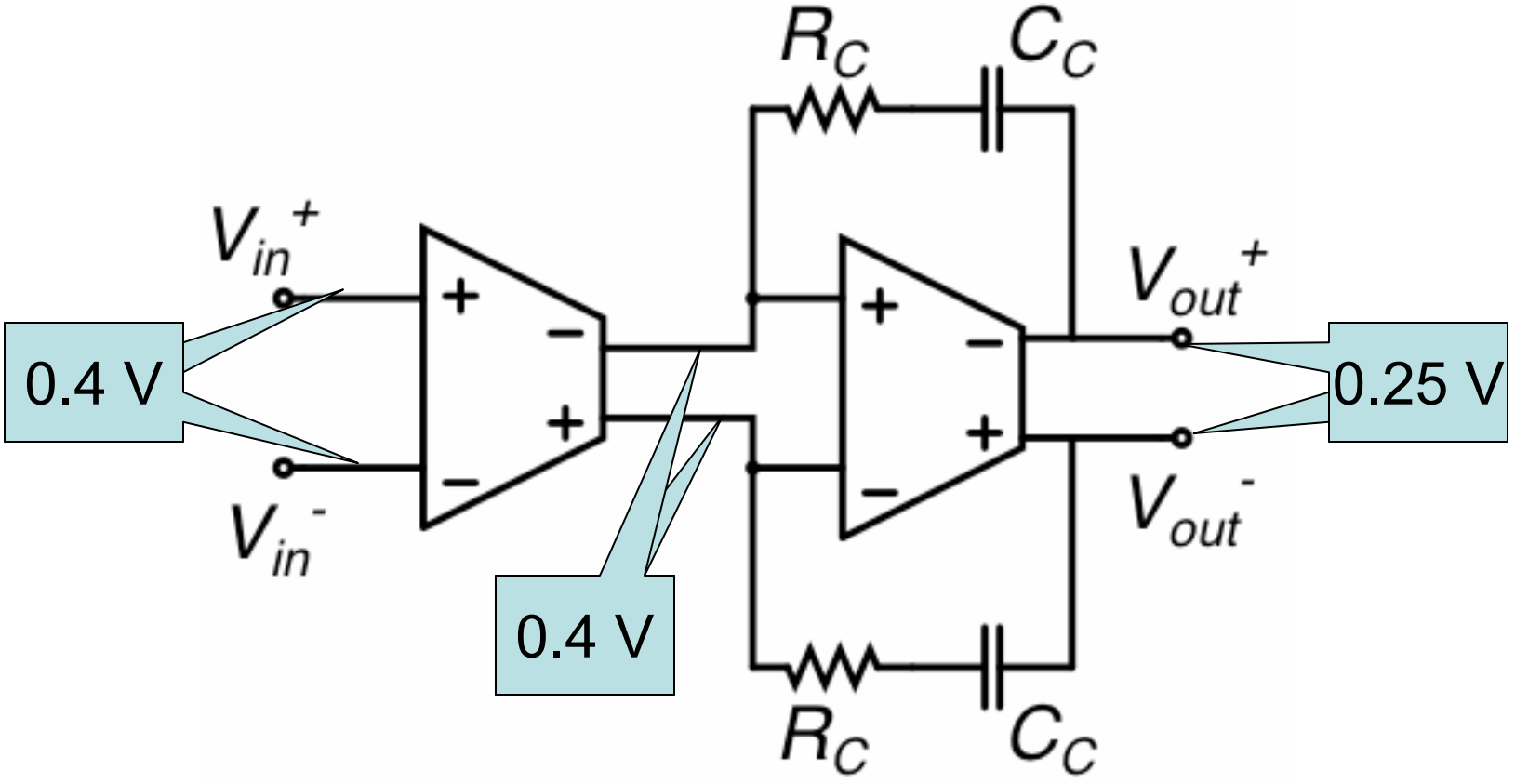
Setting common-mode voltages



0.5 V OTA gate-input stage

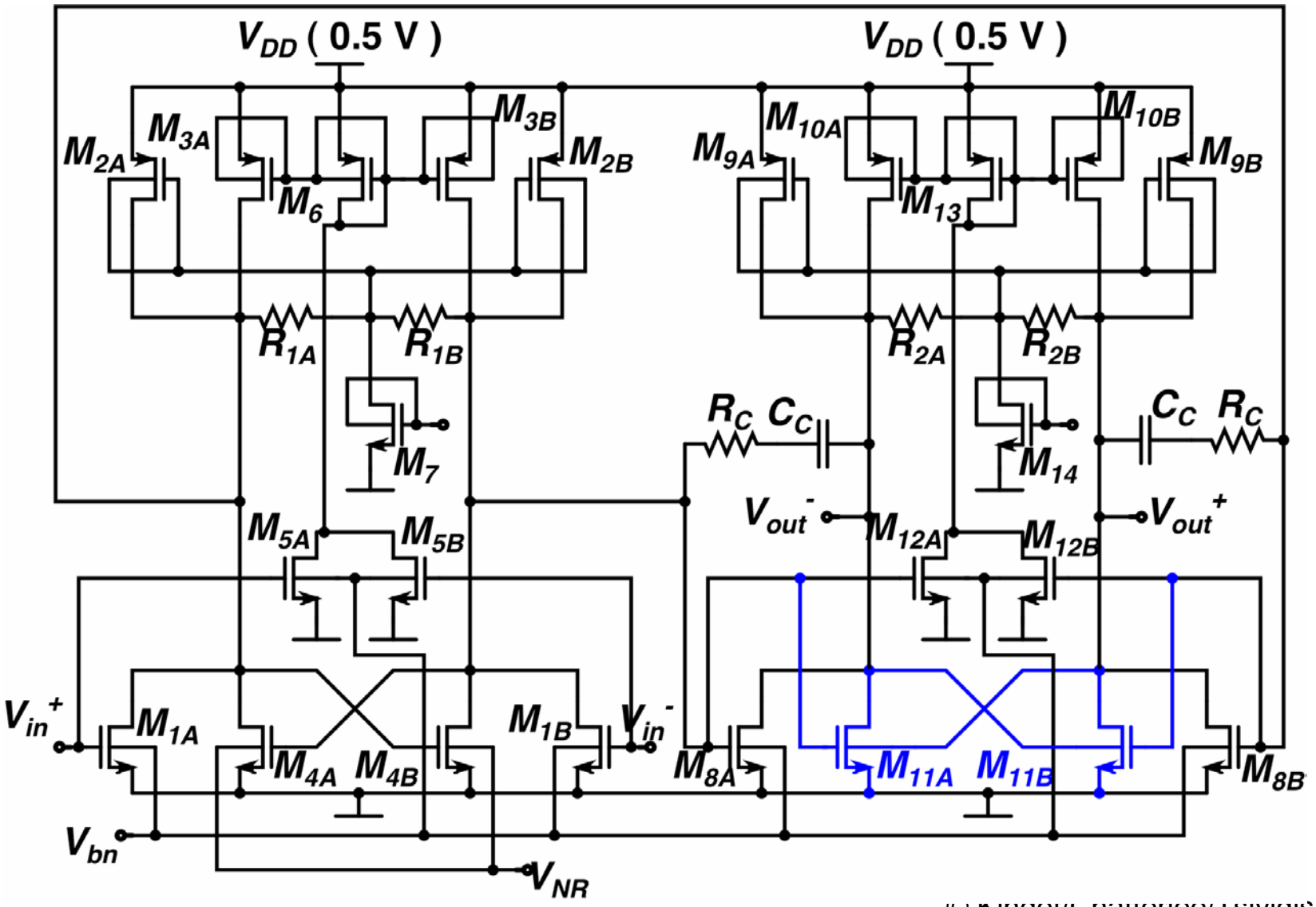


Two stage OTA

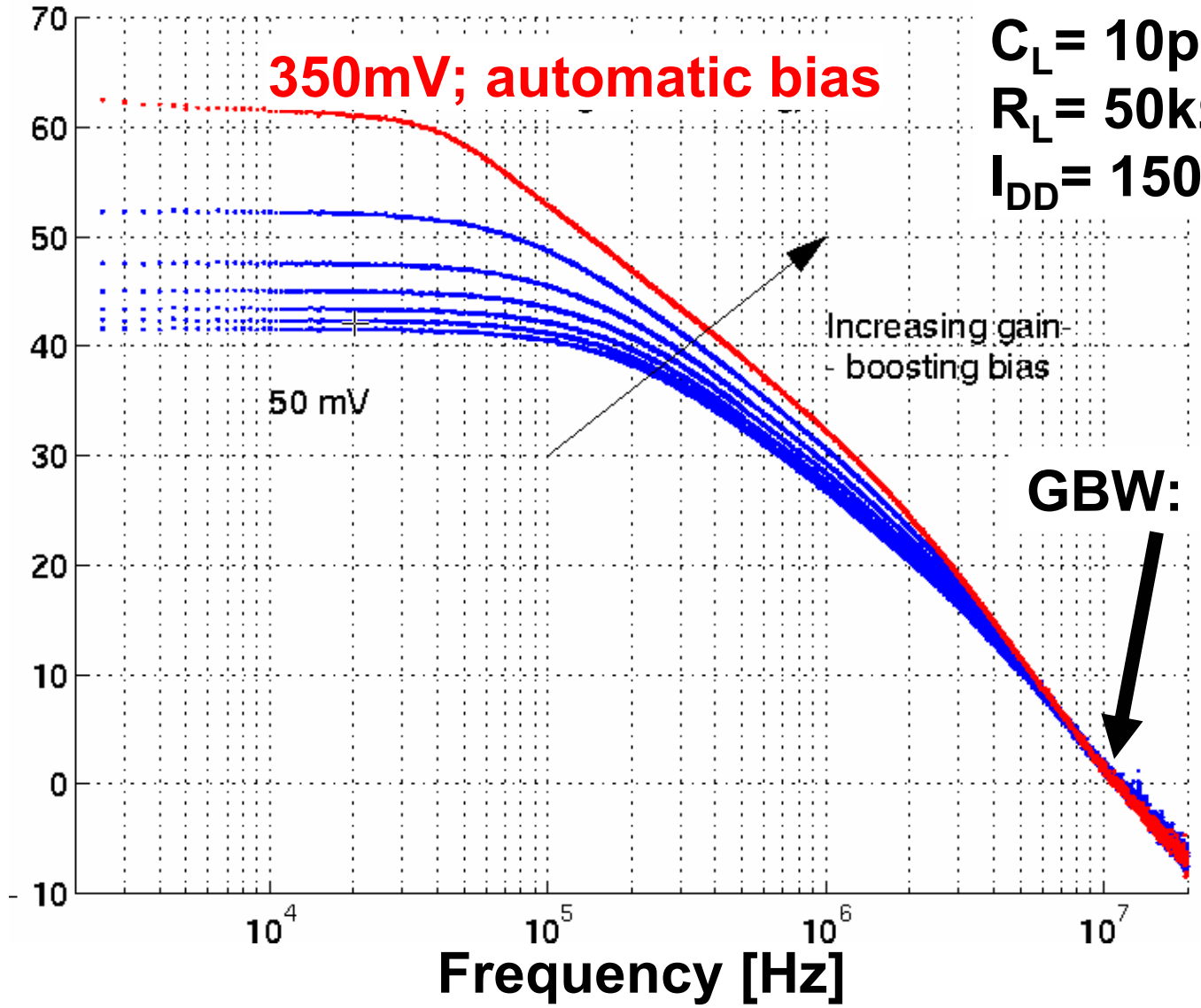


- Common-mode output of first stage is 0.4 V

Two-stage fully differential 0.5 V OTA with Miller compensation



Open Loop Performance (meas.)

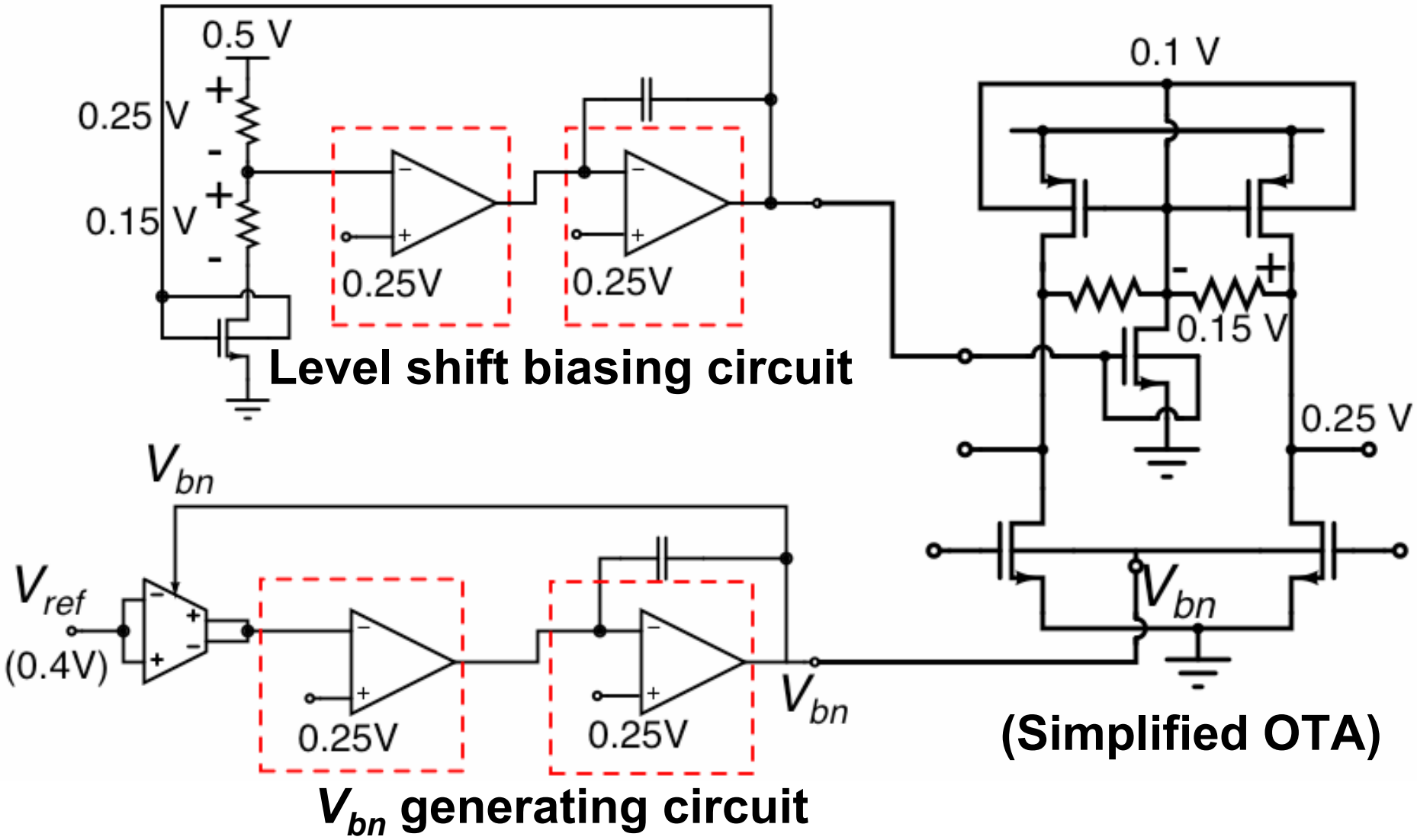


	[Bla 98]	[Las 00]	[Leh 01]	[Sto 02]	[Fer 96]	[Pel 98]	B-I	G-I
V_{DD} [V]	1	1	0.8	0.9	1.3	0.9	0.5	0.5
A_{DC} [dB]	49	70	53	70	84	59	52	50/62
GBW [MHz]	1.3	0.2	1.3	6e-3	1.3	4	2.5	10
Power [uW]	300	5	-	0.5	460	-	110	75
C_L [pF]	22	7	20	12	-	14	10	10
SE/Diff.	S	S	S	S	S	D	D	D
Techn. [um]	2	0.35	0.5	2.5	0.7	0.5	0.18	0.18
Special Devices	**Lat. BJT**	**-**	**Lat. BJT**	**Depl. MOS**	**-**	**-**	**-**	**-**
100 η [1/V]	9.5	28		13			11.4	66.7

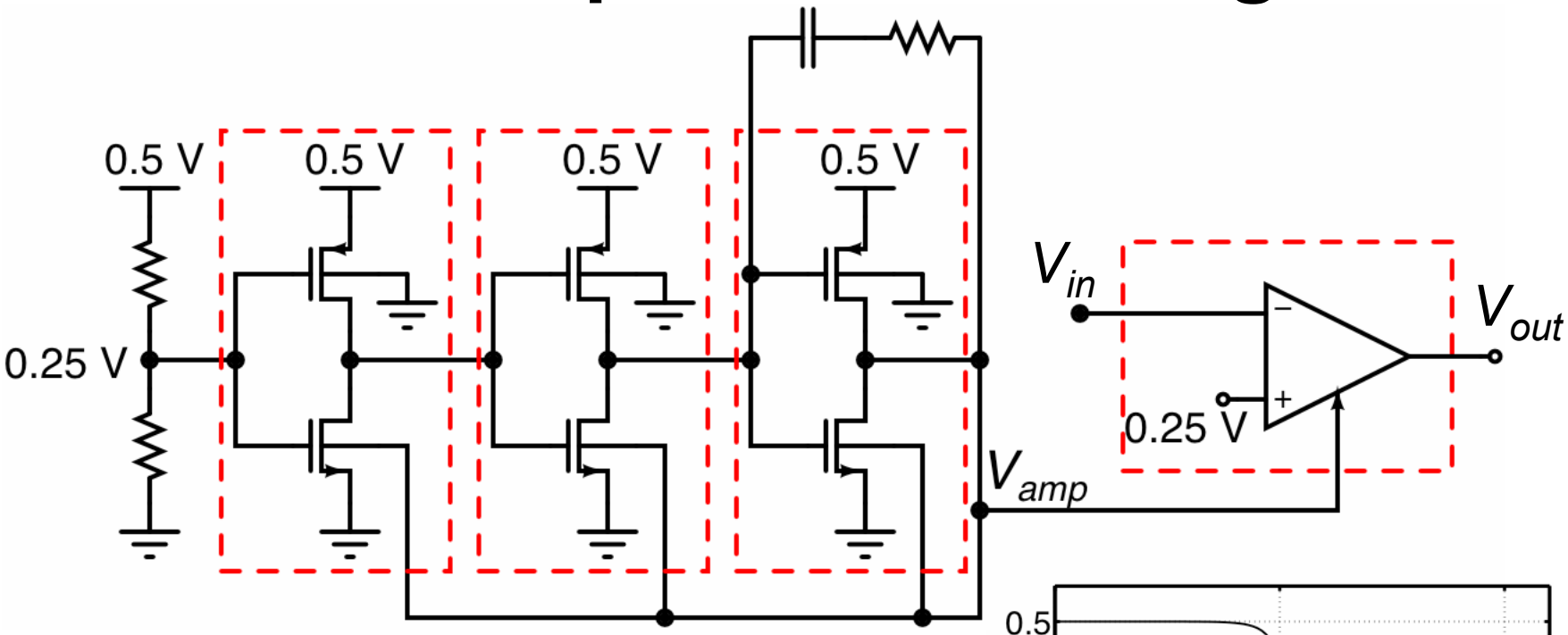
$$\eta = \frac{\text{GBW} \cdot C_L}{I_{\text{supply}}}$$

On-chip automatic biasing circuits

On-chip biasing circuits

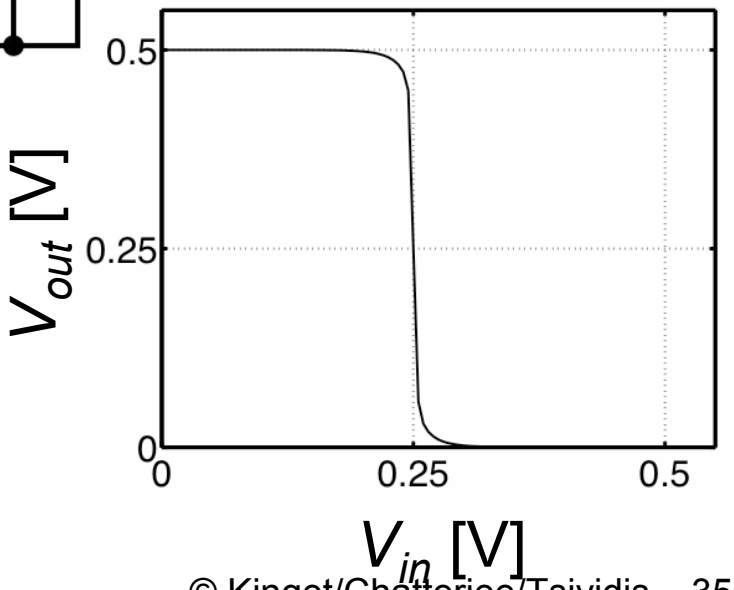


Error amplifier for biasing

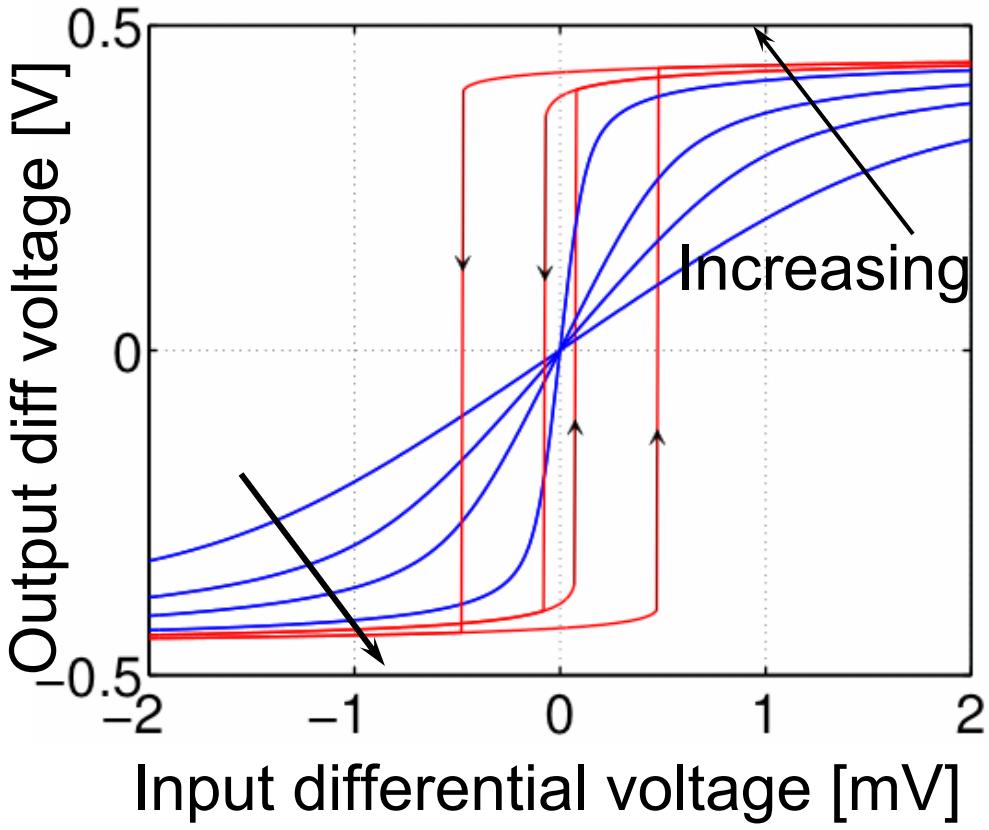


- 20 kHz GBW for 1 pF load
- 2 μA current
- Controlled body voltage

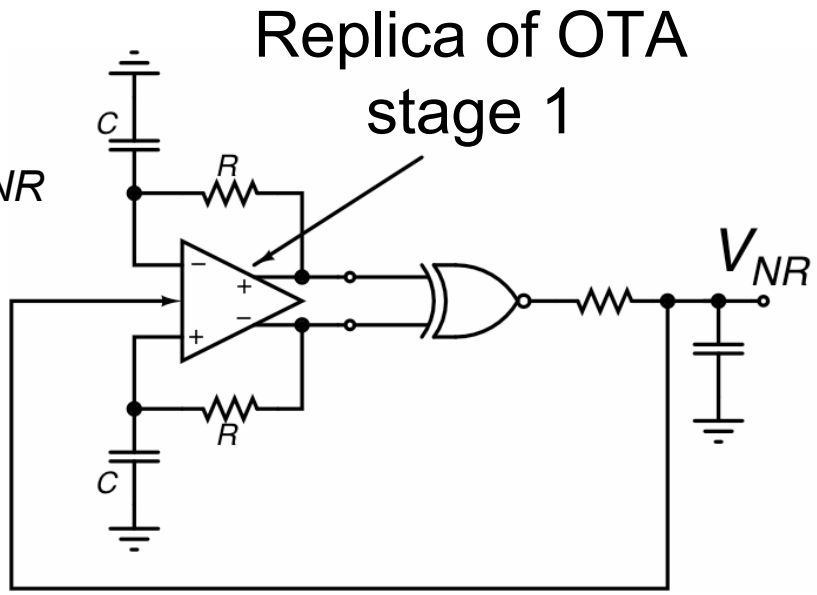
sets the amplifier threshold



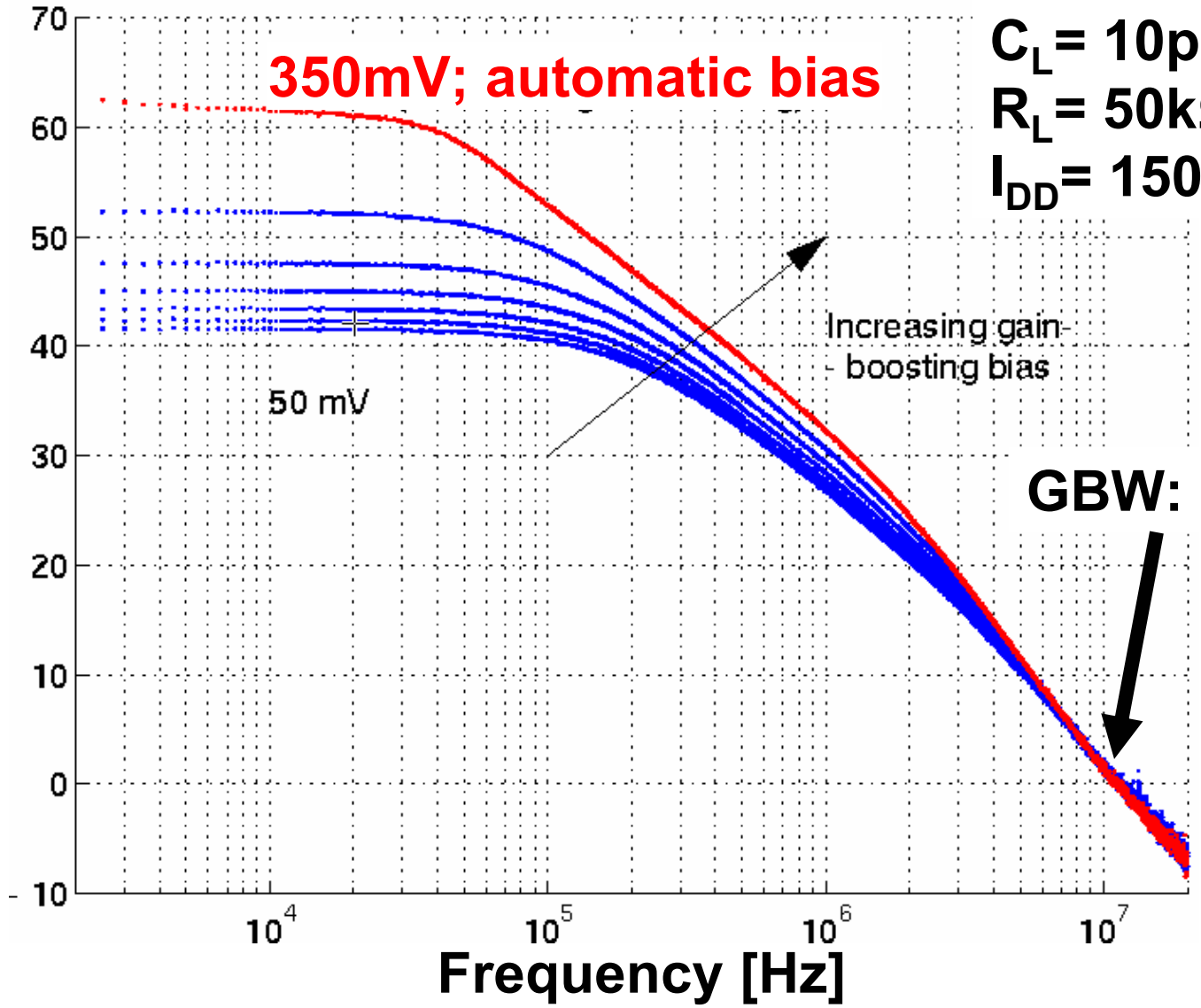
OTA dc transfer characteristics and V_{NR} generation



V_{NR} generating circuit

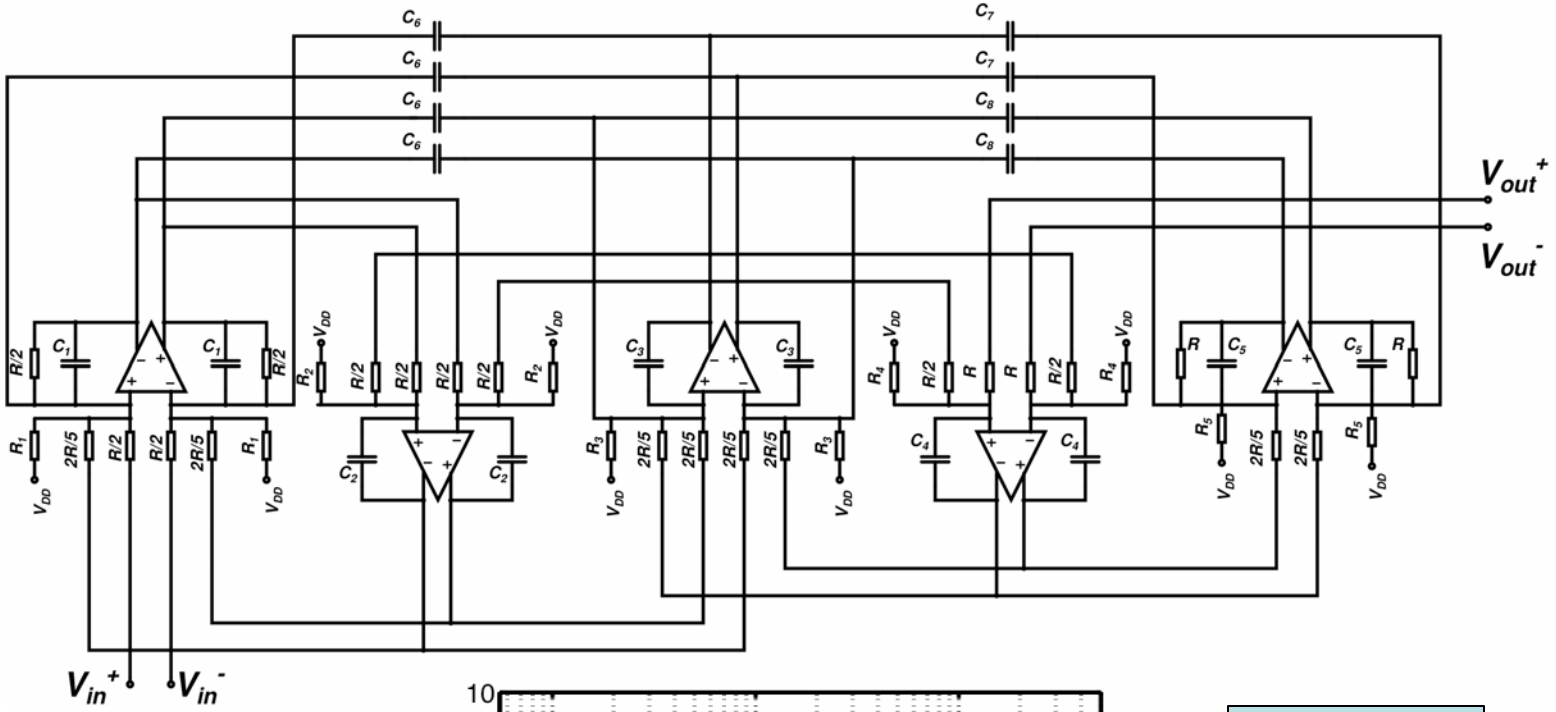


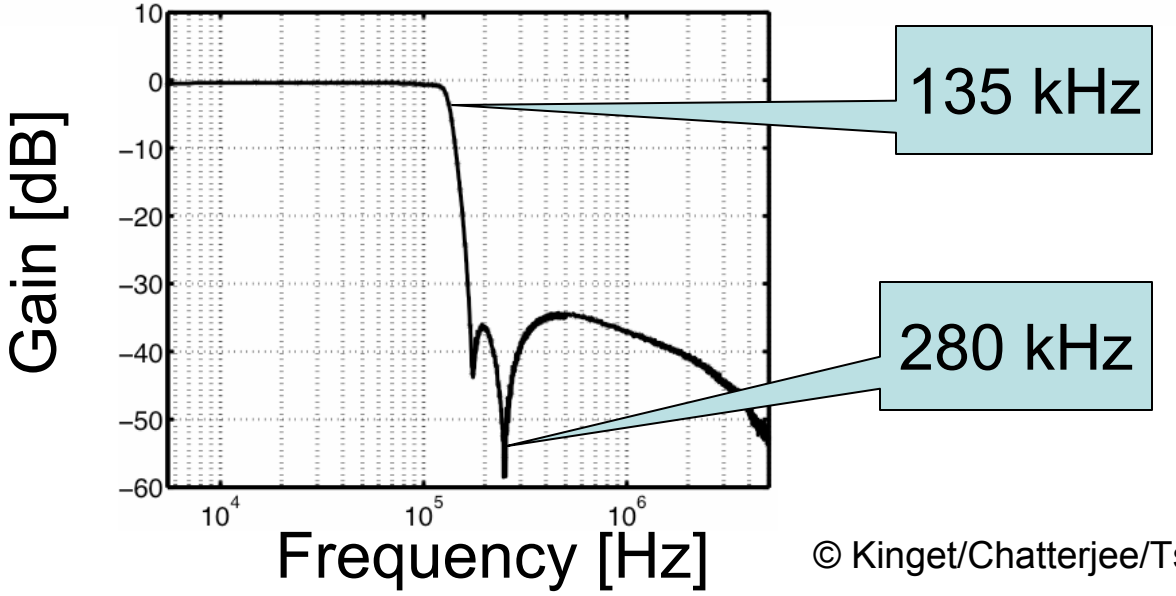
Open Loop Performance (meas.)



0.5 V Continuous time tunable active RC Filter

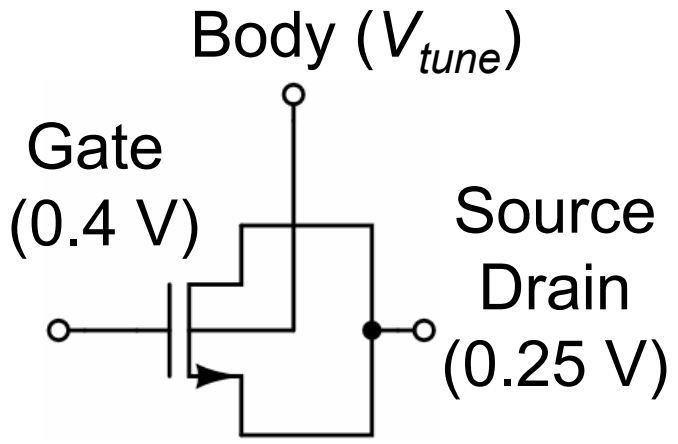
0.5 V 5th order elliptic LPF

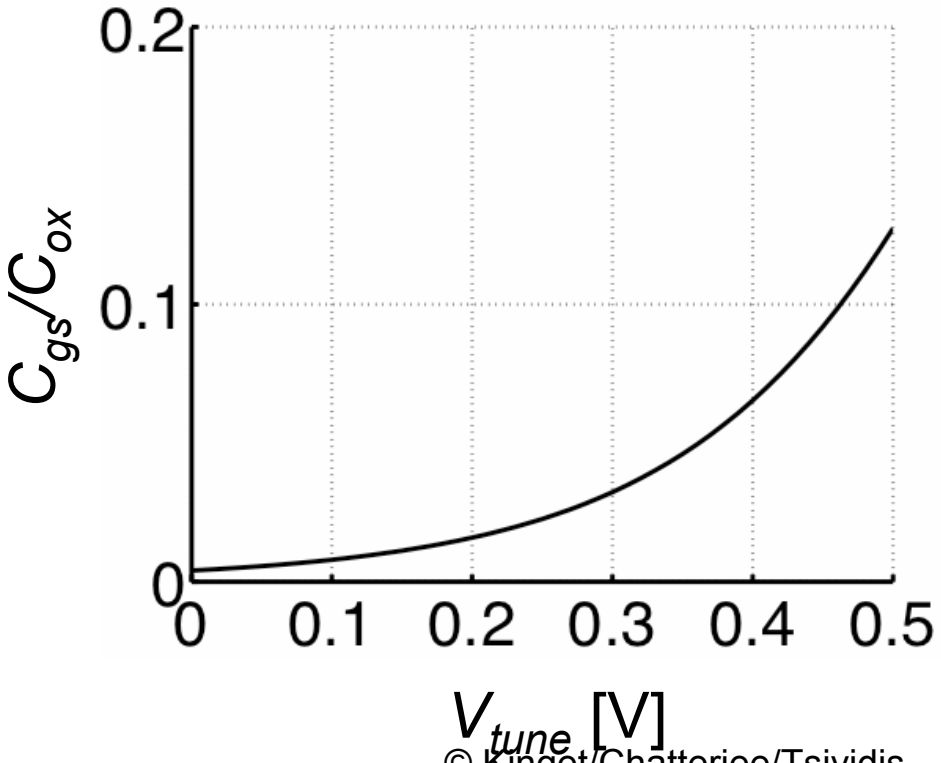




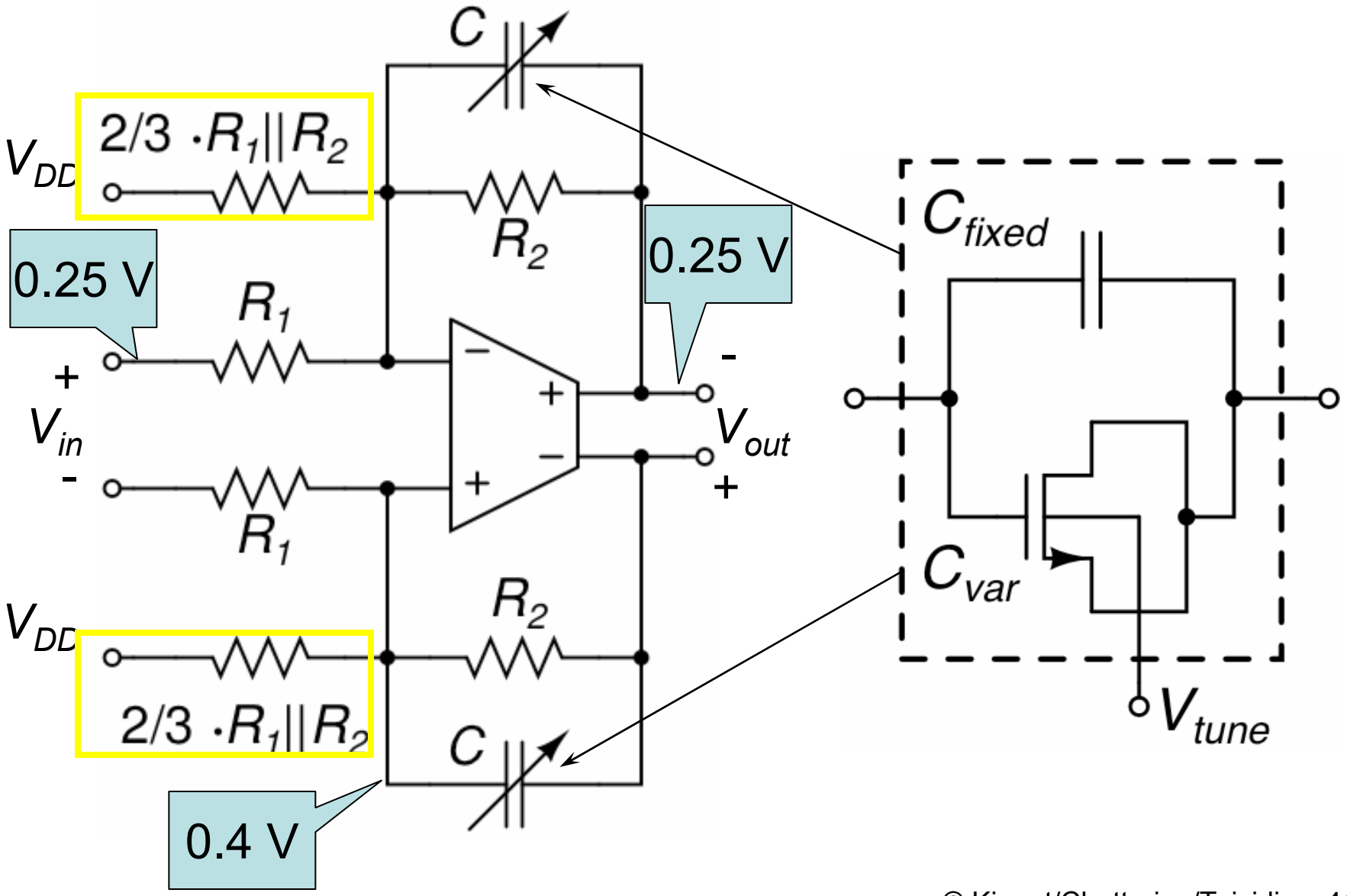
Filter tuning challenges at 0.5 V

- Gm-C
- MOSFET-C
- Switching banks of R's and C's
- **Varactor-R techniques**

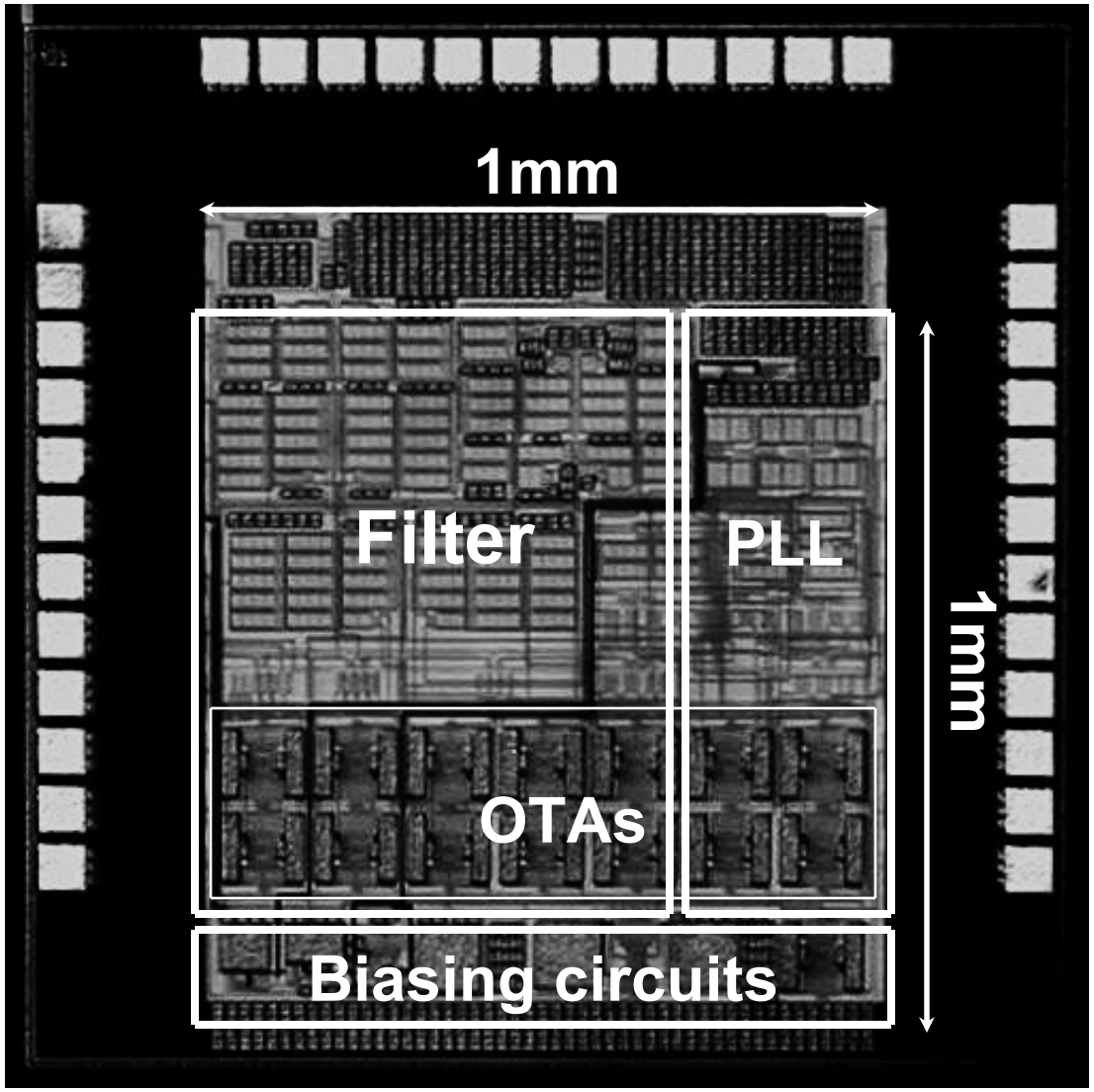




Low-voltage tunable integrator

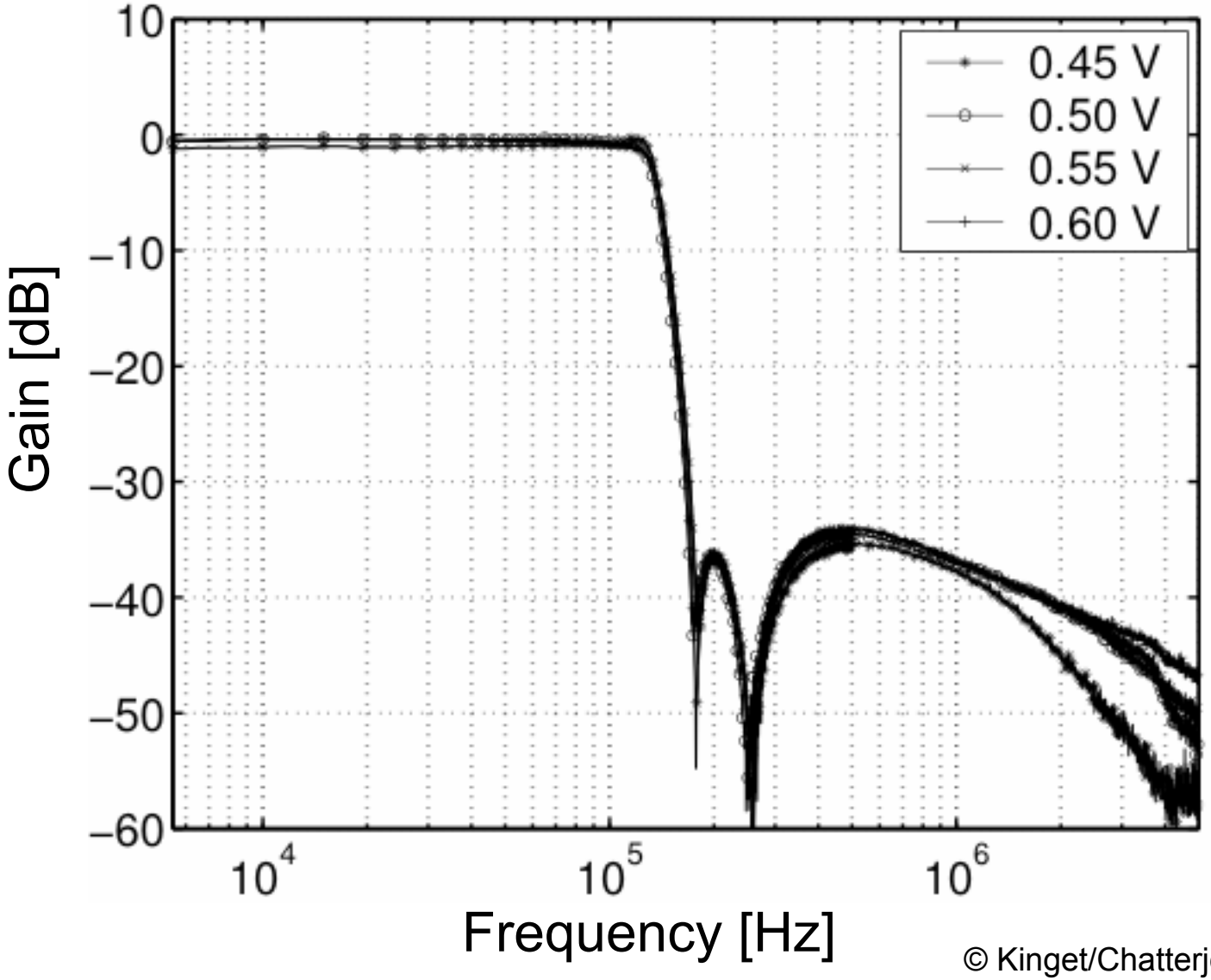


Die photograph

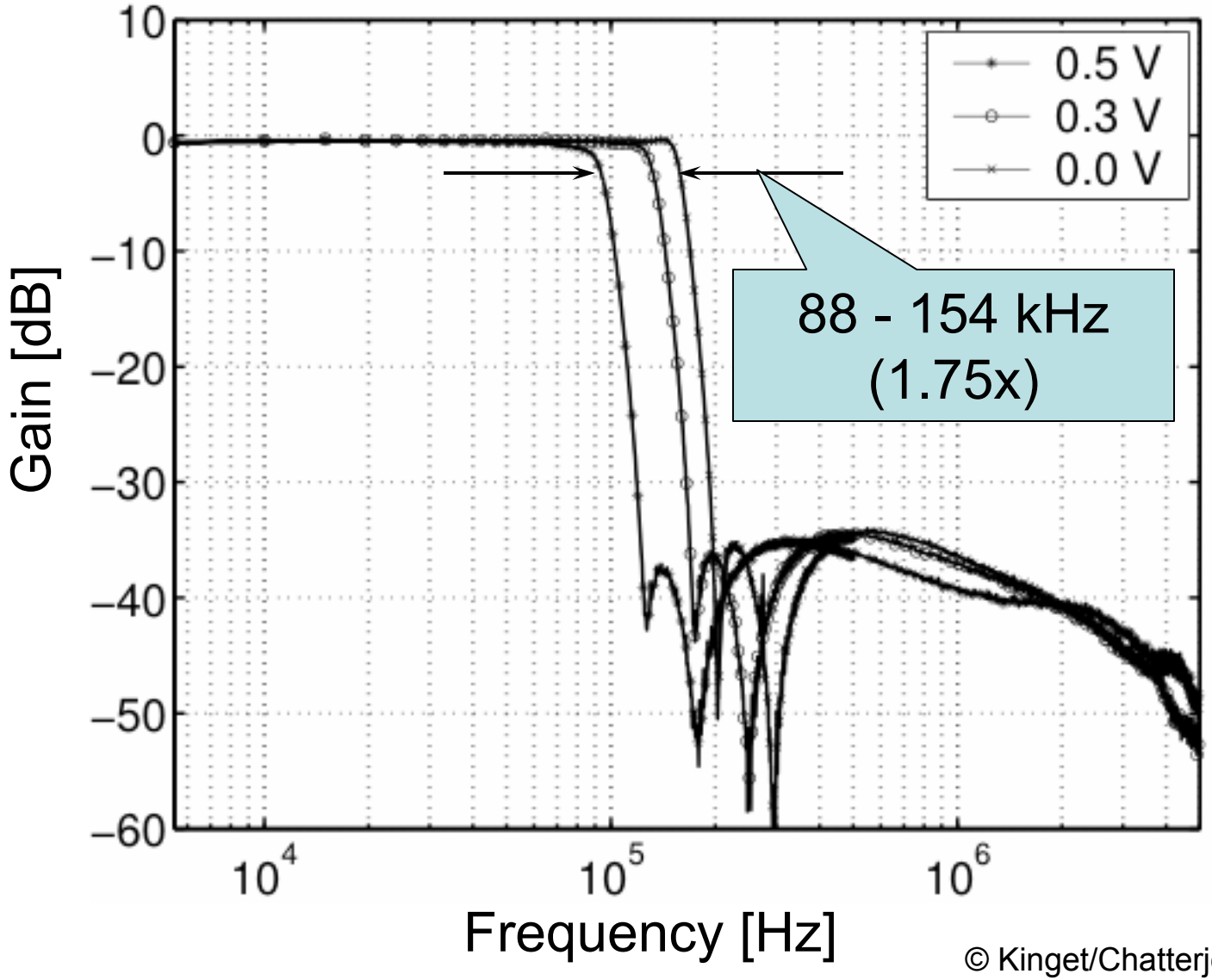


- 0.18 μm CMOS
- MIM capacitors
- High-res resistors
- Standard V_T
- Triple well devices

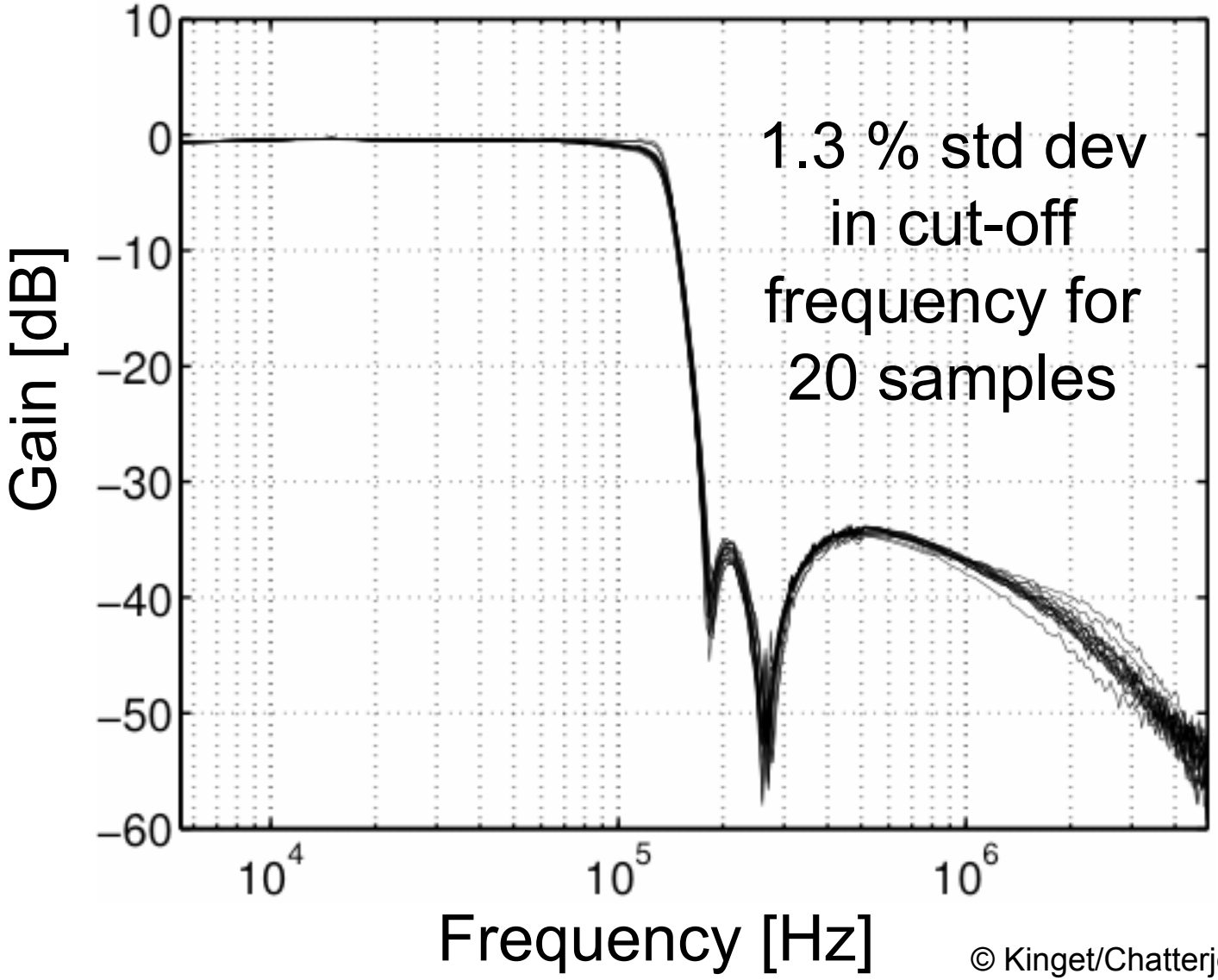
Measured filter response for different supply voltages



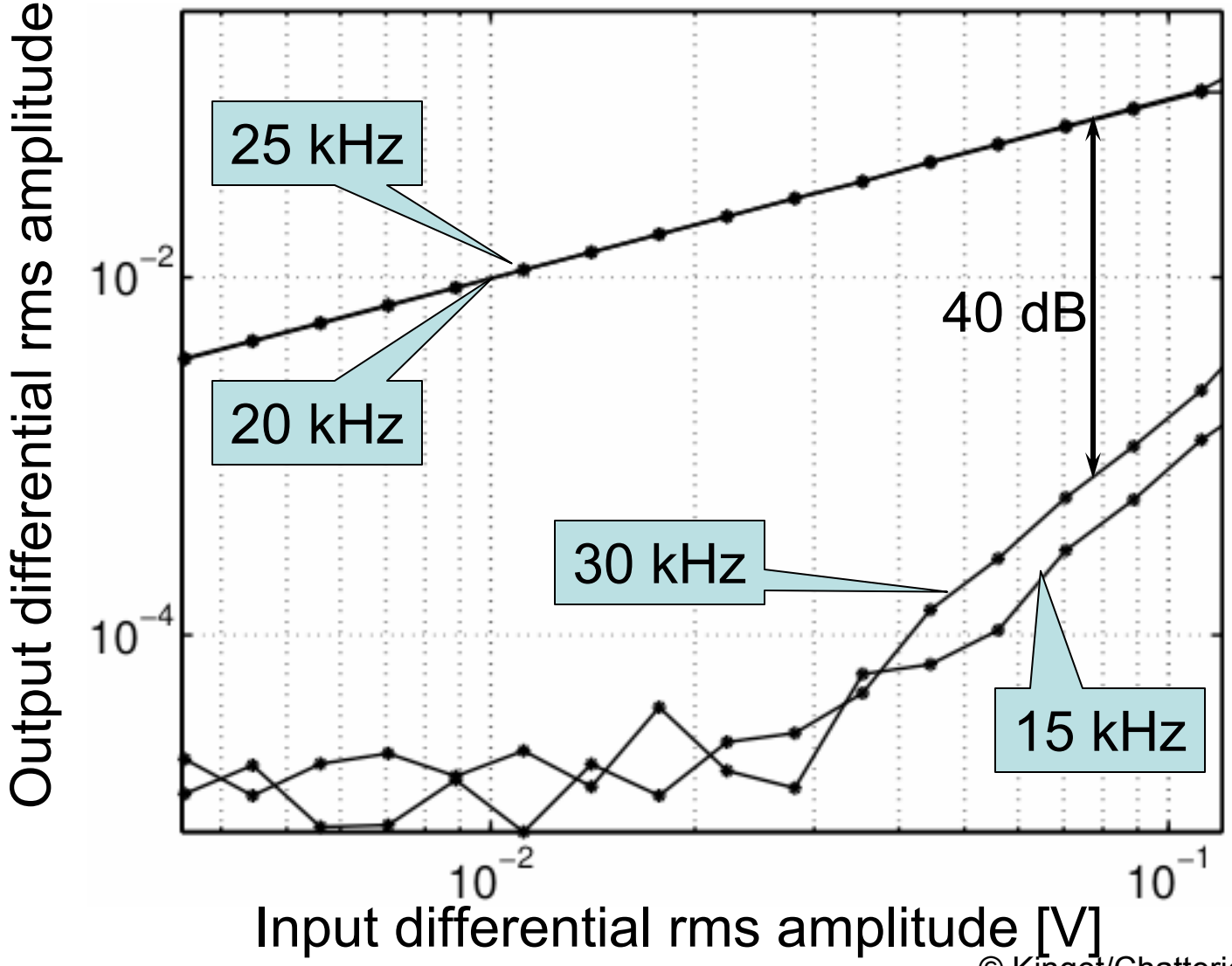
Measured filter response for different tuning voltages



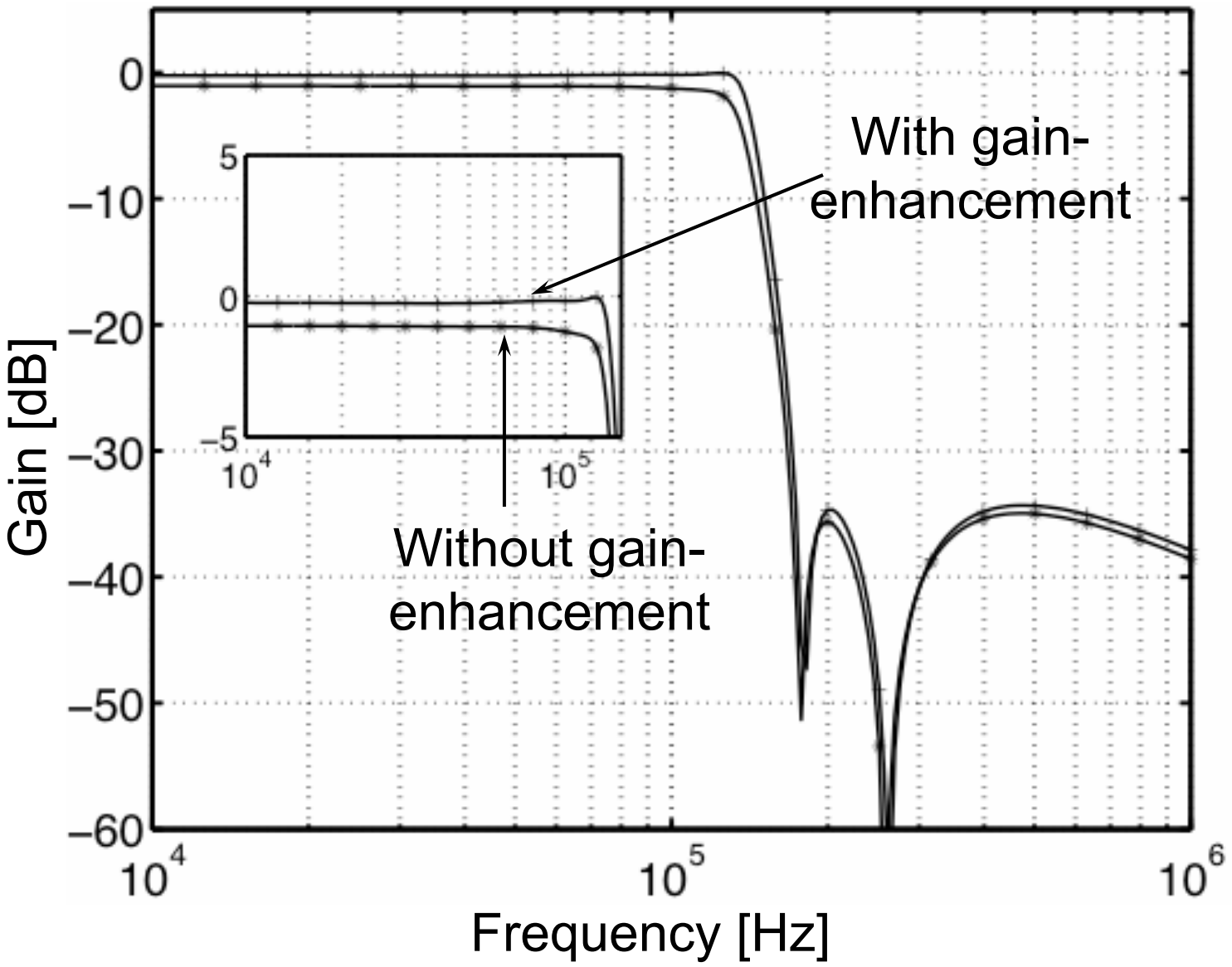
Measured filter response for different chips



Measured 3rd order inter-modulation



Effect of gain enhancement



Performance summary at 27C

V_{DD} [V]	0.45	0.50	0.55	0.60
-3 dB cut-off frequency [kHz]	135.0	135.0	135.0	135.0
Total current [mA]	1.5	2.2	3.3	4.3
Noise [μV rms]	87	74	68	65
Input [mV rms] (100kHz / 1% THD)	50	50	50	50
In-band IIP_3 [dBV]	-5	-3	-3	-3
Out-of-band IIP_3 [dBV]	3	5	3	5
Dynamic range [dB]	55	57	57	58
Tuning range [kHz] $V_{tune} = V_{DD}$	96.5	88.0	84.5	69.0
V_{tune} = 0.0 V	153.0	154.5	148.0	150.5
VCO feed-thru @280kHz [μV rms]	104	85	72	72

- Measured CMRR (10 kHz common mode tone): 65 dB
- Measured PSRR (10 kHz tone on power supply): 43 dB

Functionality tested from 5C to 85C at 0.5 V

Conclusions

- Developed true low voltage design techniques for 0.5 V analog circuits.
- Low voltage OTAs designed - can be used as building block in other designs.
- Automatic biasing and tuning through bodies of devices.
- PLL-tuned 5th order elliptic low-pass filter demonstrated.
- Step towards 0.5 V analog circuits for the nano-scale CMOS era

Acknowledgments

- Analog Devices for supporting part of this work.

More details

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