COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK
Department of Electrical Engineering

0.5V Analog integrated circuits for nanoscale CMOS technologies

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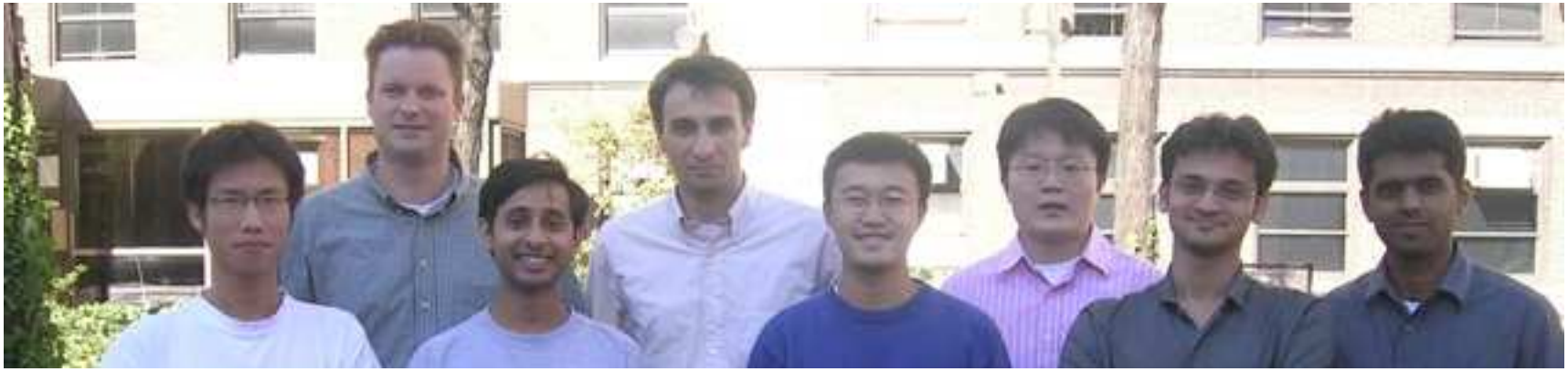
Analog & RF IC Design Research



Ultra-low voltage circuits: 0.5V

RF integrated oscillators

Ultra-wideband RF circuits

RF Passives

Injection locked circuits

Device mismatch & its influence on Analog & RF ICs

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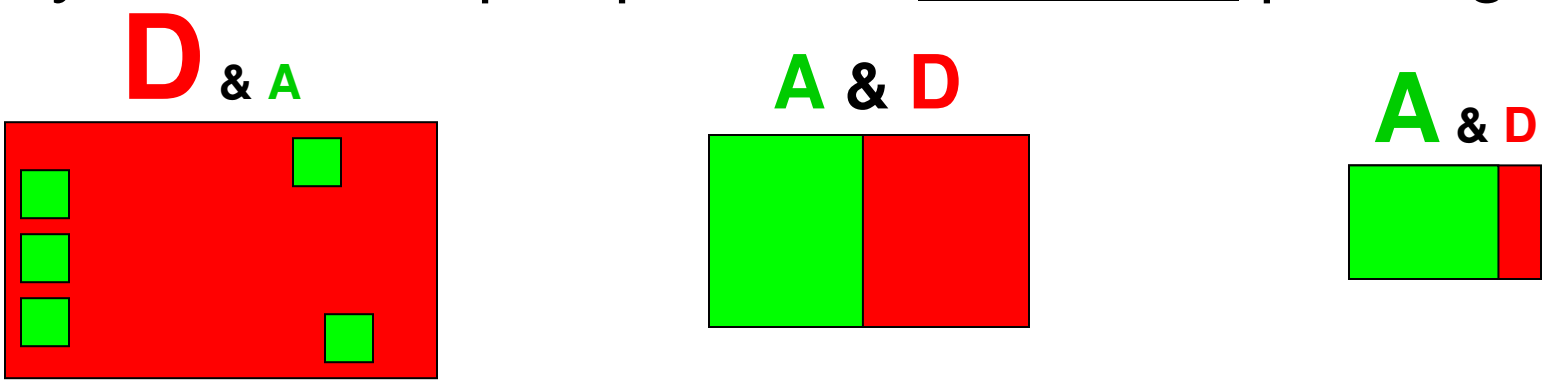
Outline

- Do we need Analog Integrated Circuits in nanometer CMOS?
- Design Challenges & Opportunities.
- 0.5 V Operational Transconductance Amplifiers & Biasing Circuits.
- 0.5 V Fully Integrated Active RC Filter with on-chip Automatic Tuning.
- A 0.5V 74dB SNDR 25kHz CT ΣΔ Modulator with Return-to-open DAC
- Conclusions.

Analog in a *Mixed Signal World*

- Sounds, images, EM waves, …. are ANALOG.
- Information processing & storage are DIGITAL.
- System-on-chip is powerful economic paradigm.

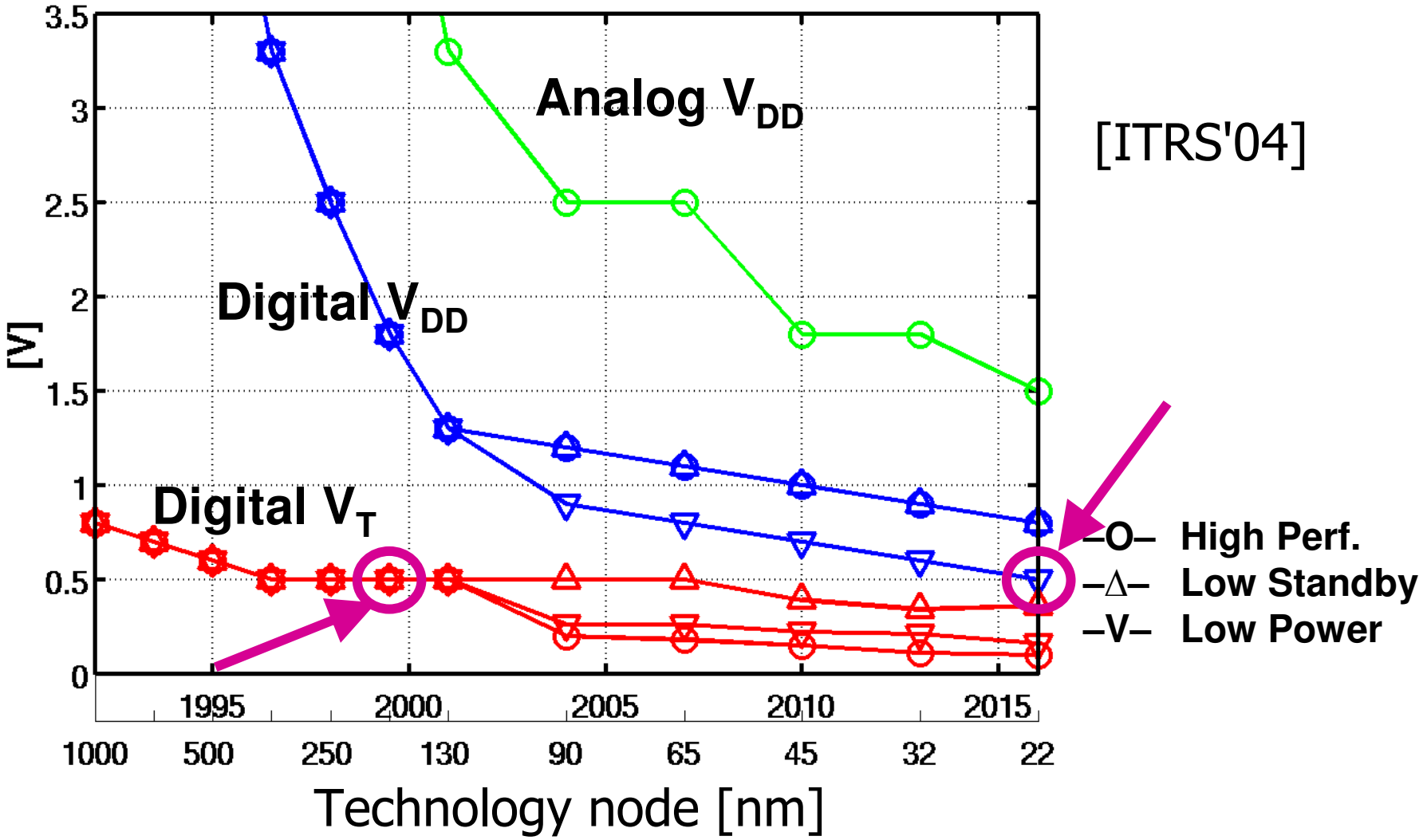


- Digital drives technology development & choice.

Most Digital ICs need some Analog!

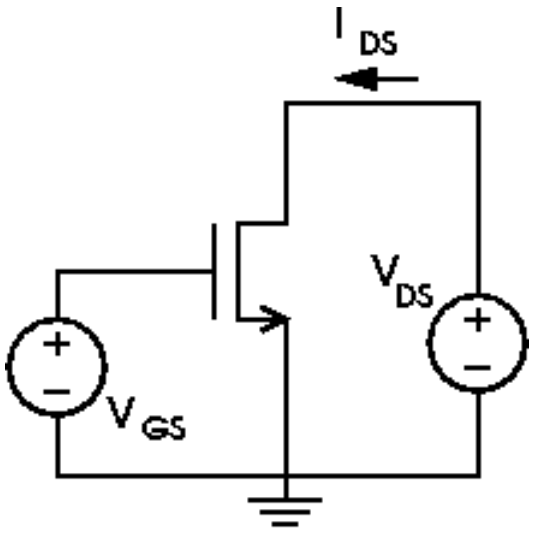
If Analog can be done in a digital technology, it will be done.

CMOS trends: Supply voltage

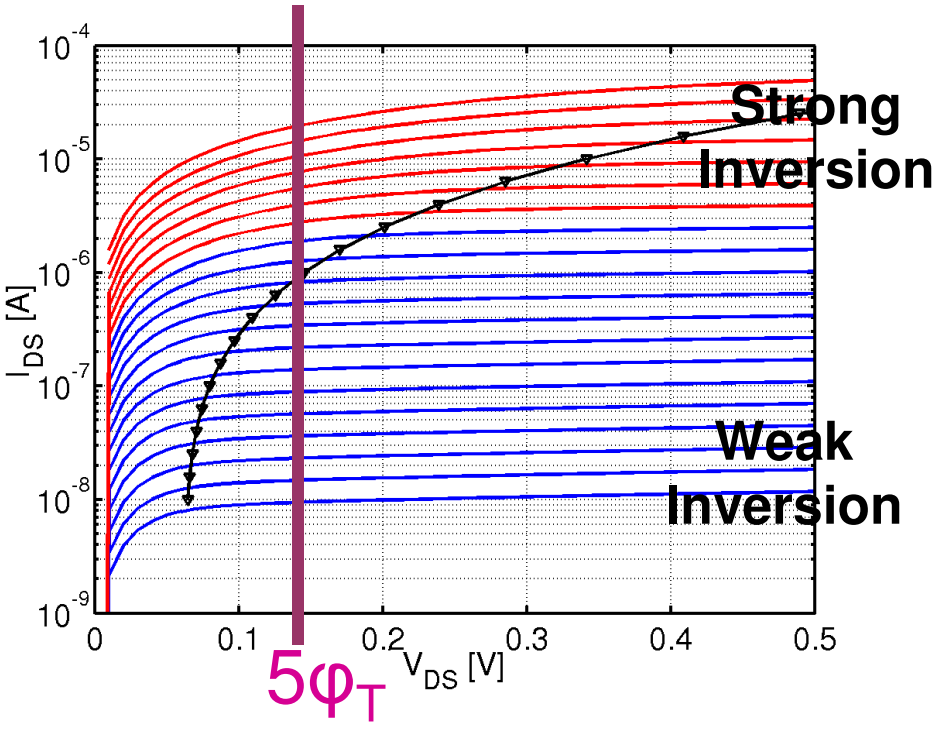


[ITRS'04]

MOST biasing: CS or VCCS

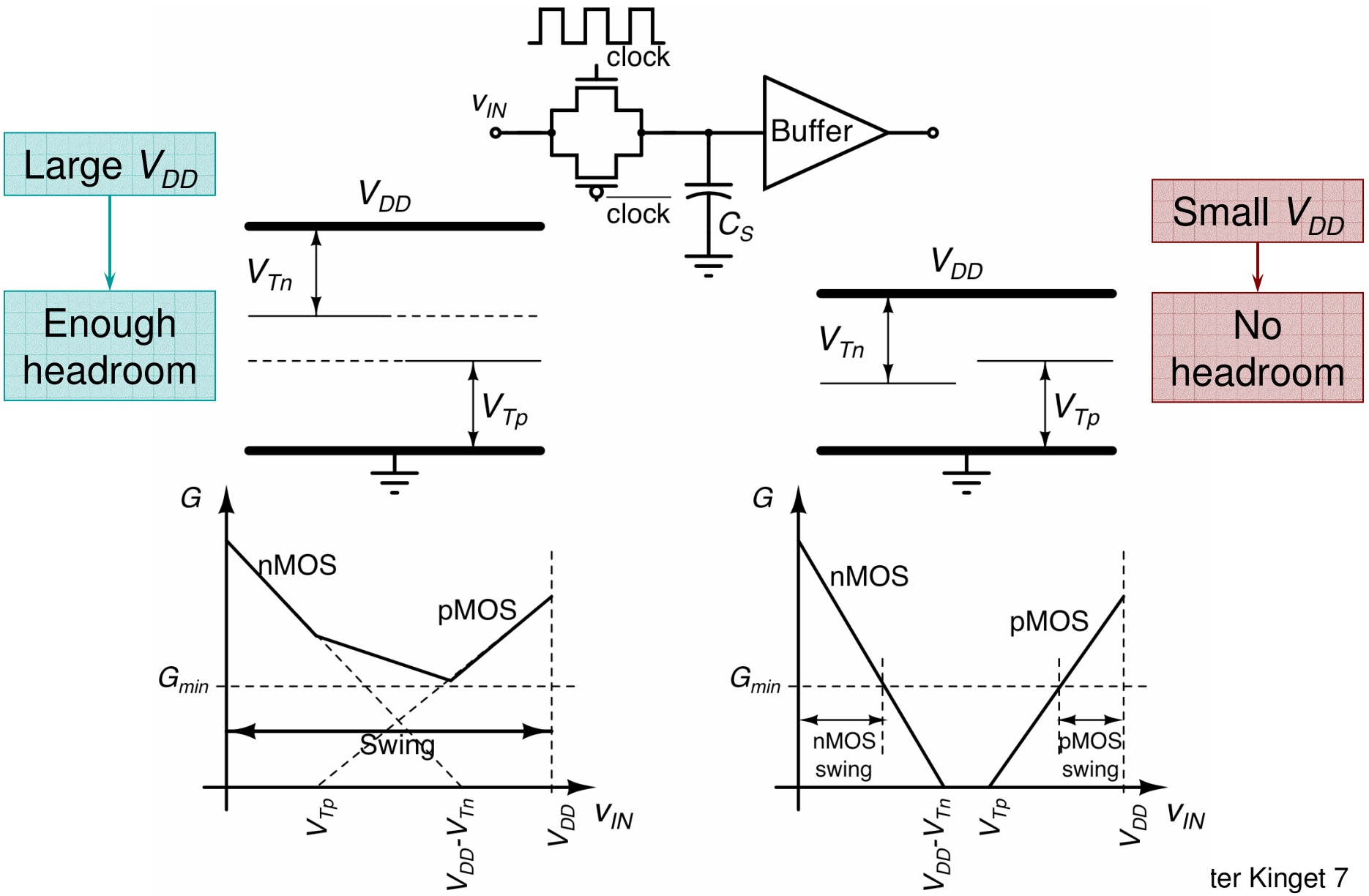


0.24µm/0.36µm nMOS in 0.18µm CMOS

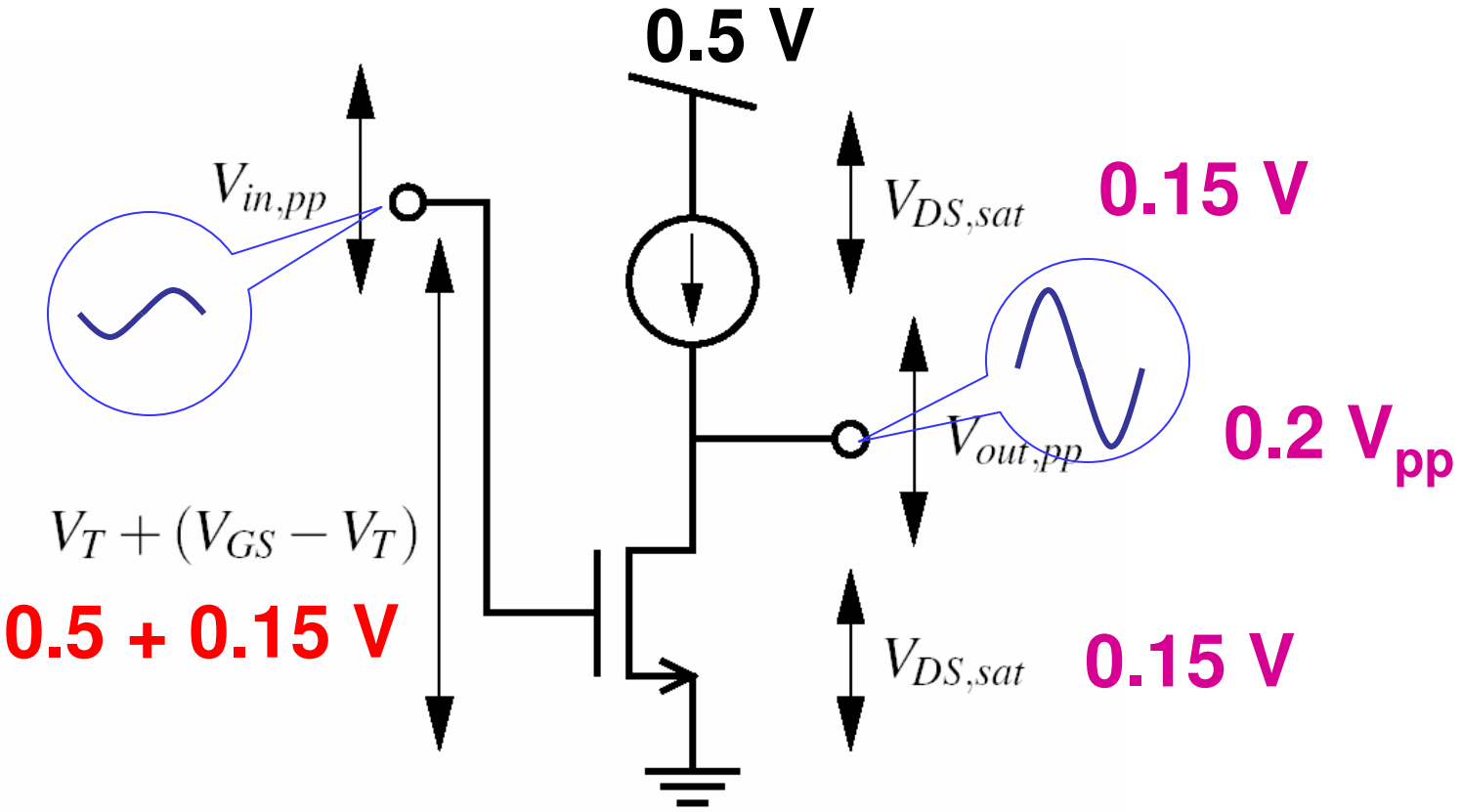


- Transconductor or Current Source
  $V_{DS} > 0.15V$ (for V_{GS}-$V_T \leq 0.2$)

Switches at 0.5 V



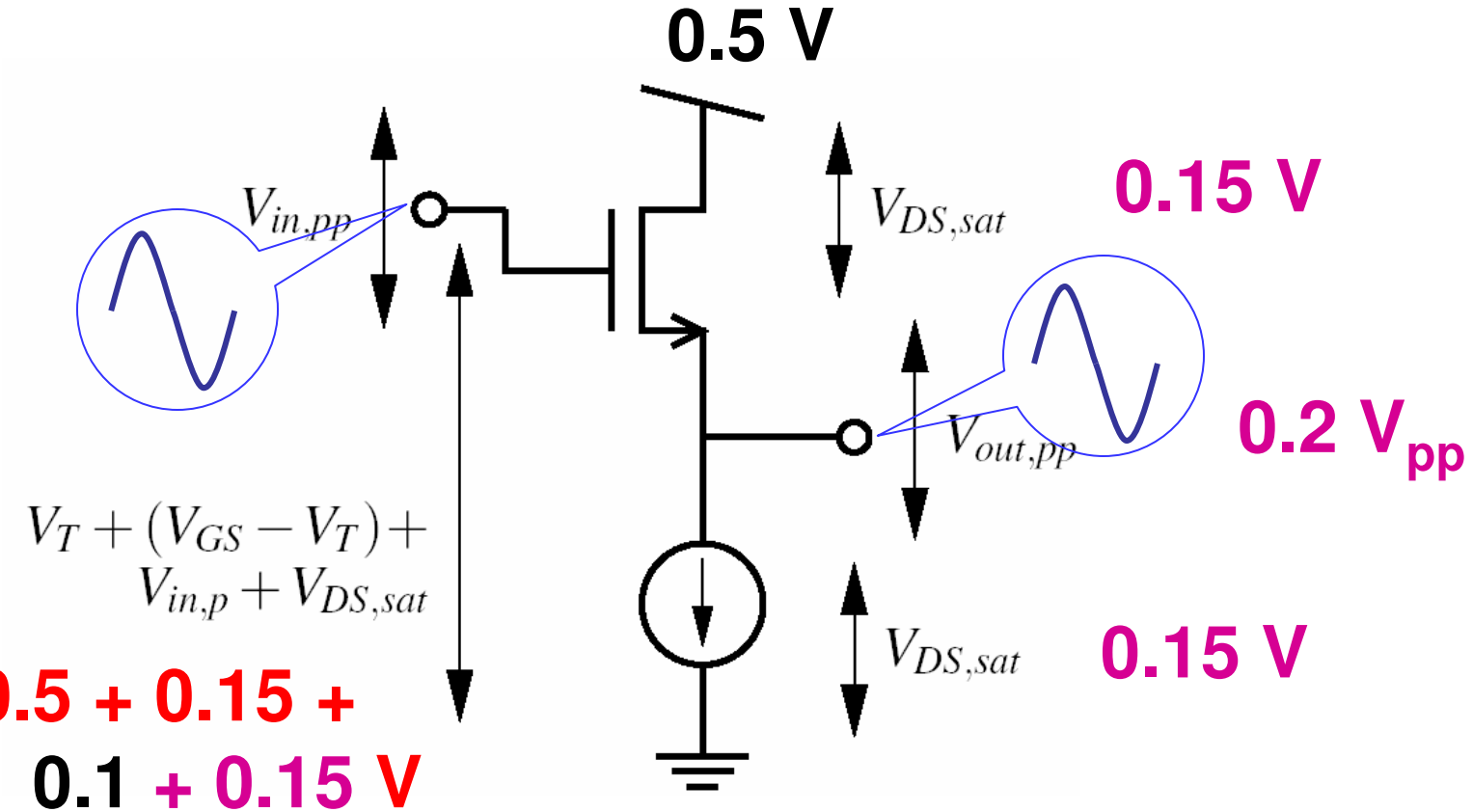
Common source amplifier



V_T= 0.5 V

$V_{DS,sat}$= 0.15 V

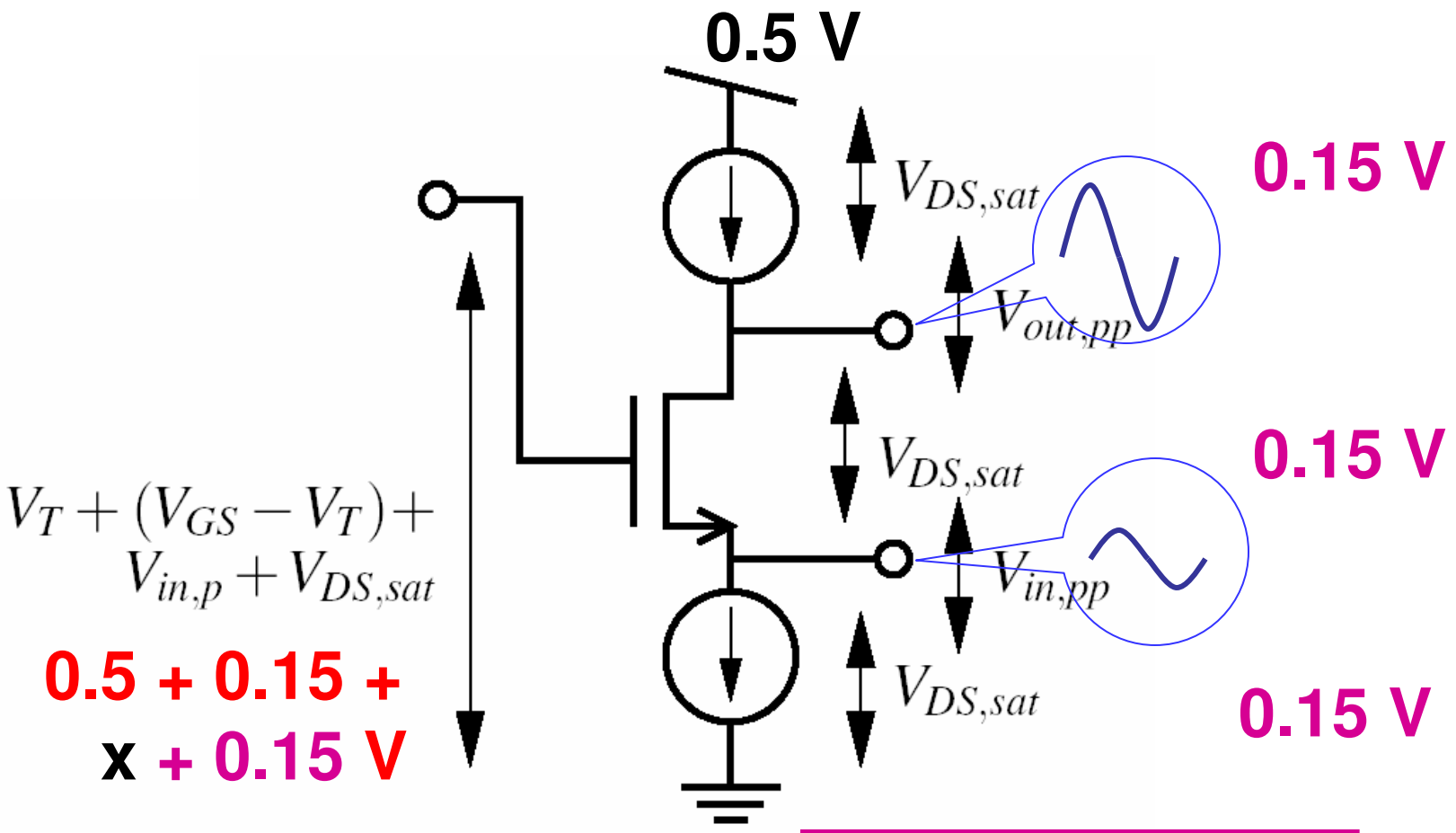
Common drain buffer



V_T= 0.5 V

$V_{DS,sat}$= 0.15 V

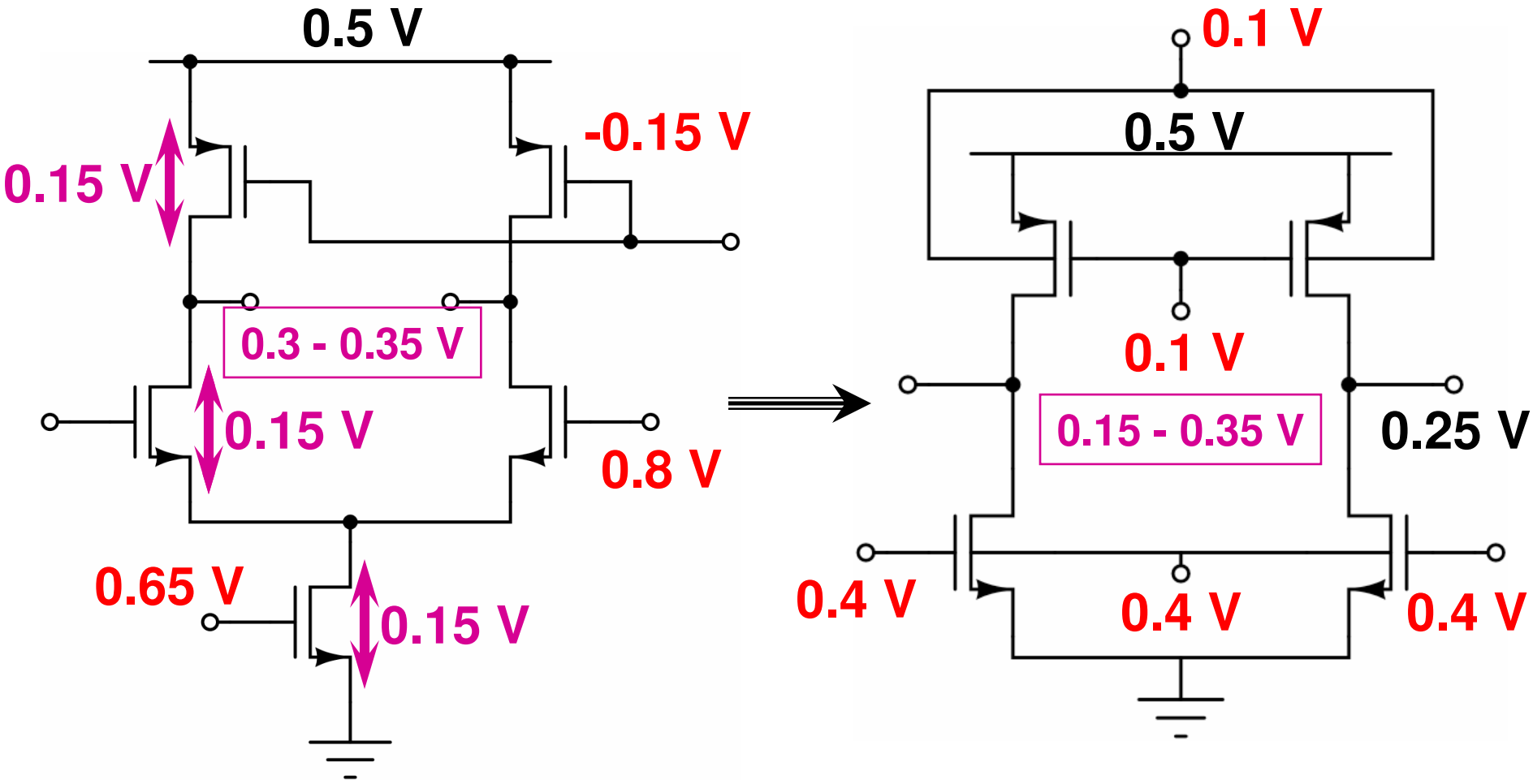
Common gate amplifier / Cascode



V_T= 0.5 V

$V_{DS,sat}$= 0.15 V

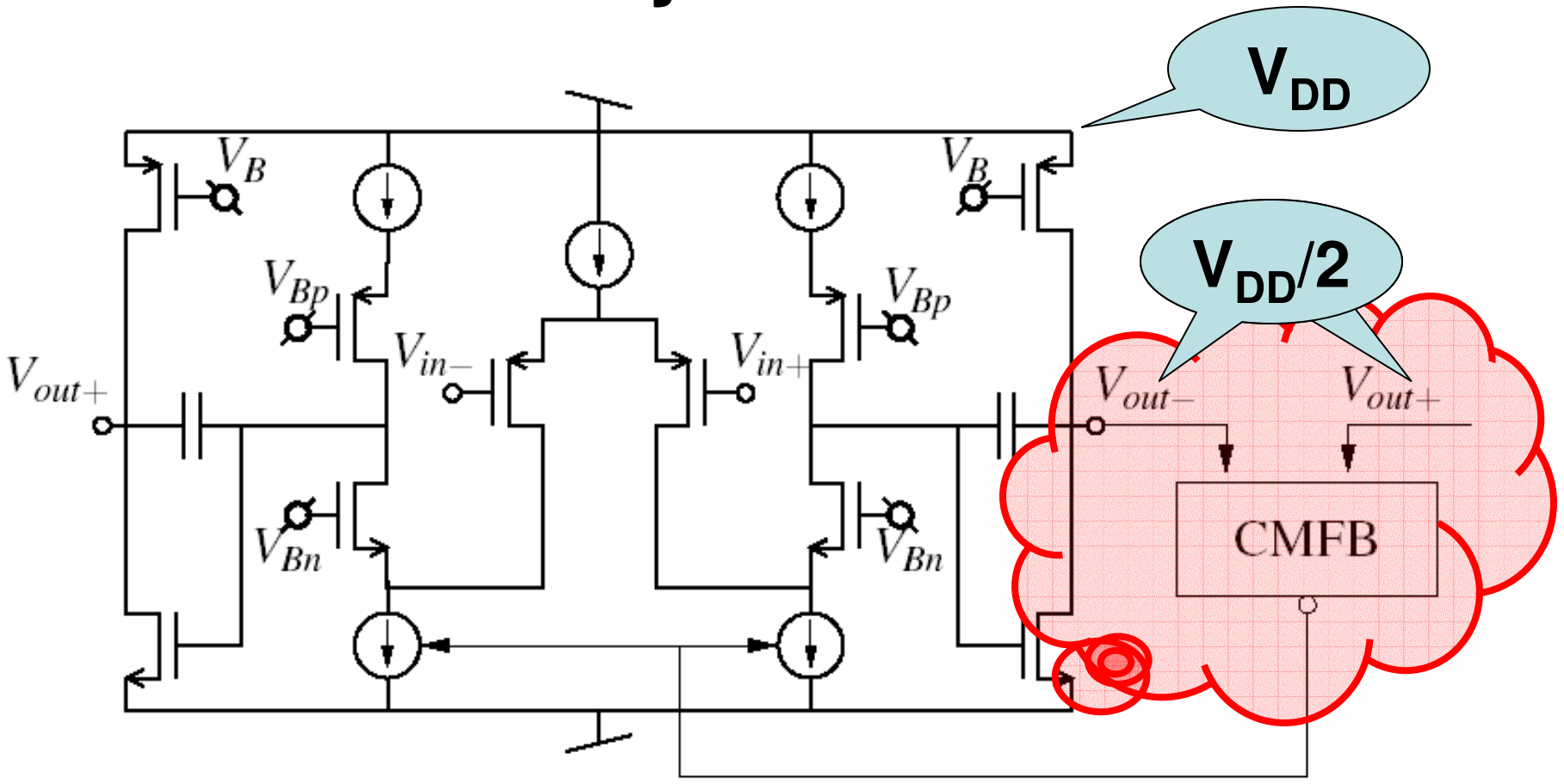
Differential OTA design challenges



$V_T = 0.5$ V

$V_{DS,sat} = 0.15$ V

CMFB for fully differential OTAs



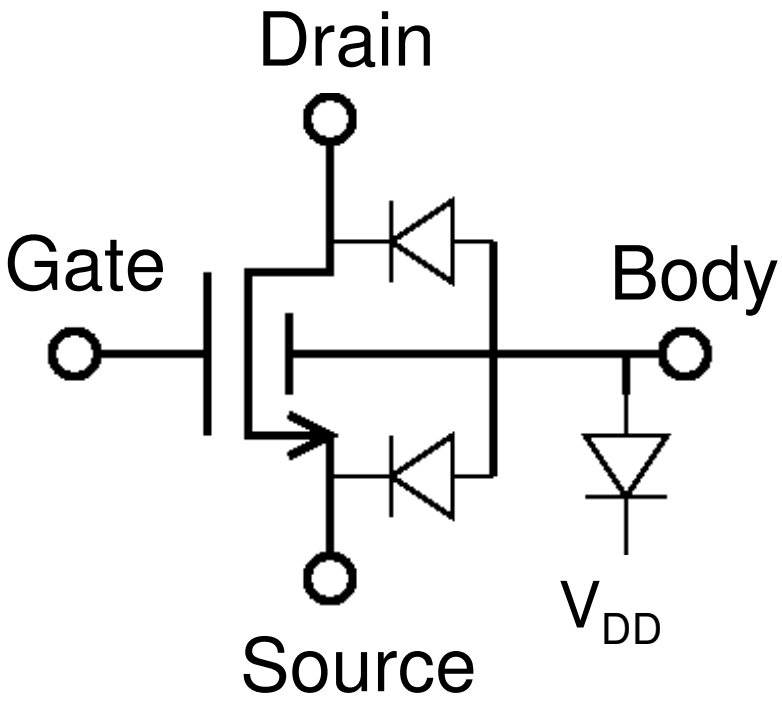
Common Mode Feedback requires 'fast' amplifier operating from $V_{out,CM} = V_{DD}/2$!?

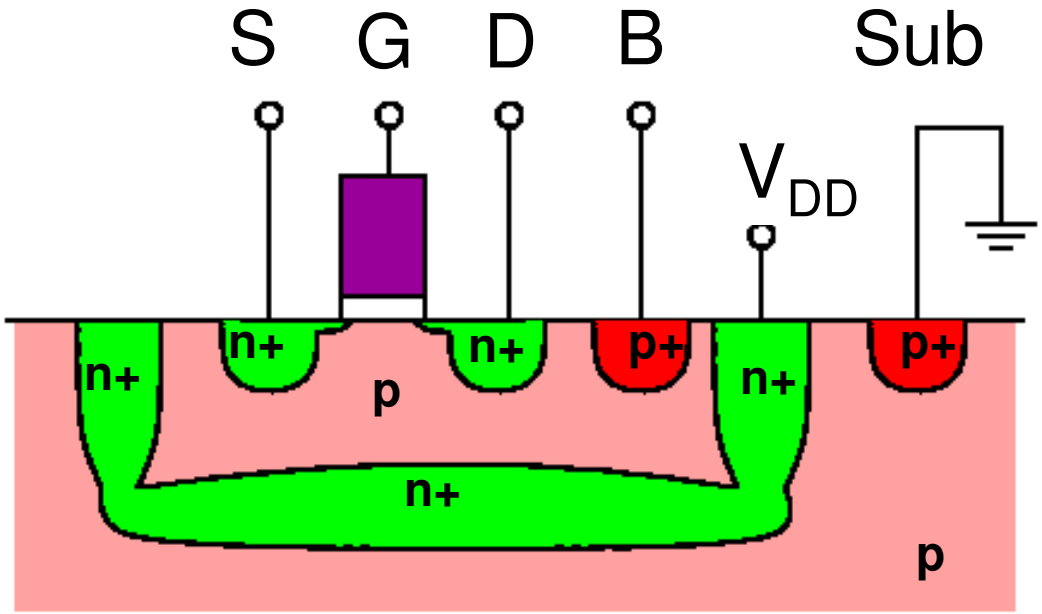
Challenges at 0.5 V

- $V_{DS,sat}$ related challenges:
  - *Independent* of region of operation!
  - *Independent* of V_T!
  - Signal swings are limited:
    - Use differential circuits.
  - Avoid transistor stacks:
    - No tail current source: How to achieve CM rejection?
    - No cascodes: How to increase DC gain?
- V_{GS} related challenges:
  - *Depend* on region of operation & $(V_{GS}-V_T)$.
  - *Depend* on V_T!
  - Avoid signal swing on gate:
    - How to do overall CMFB?
    - How to achieve strong inversion operation?

Opportunities at 0.5 V: MOST has 4-terminals

nMOS circuit equivalent (deep n-well process)



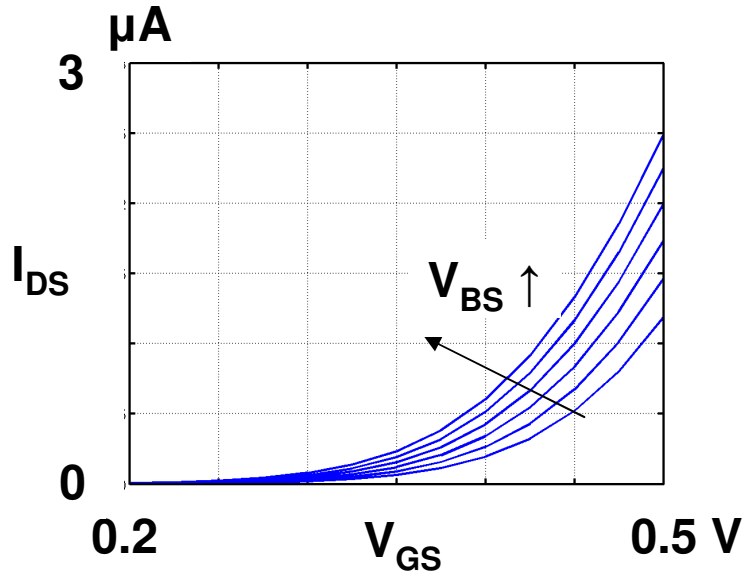


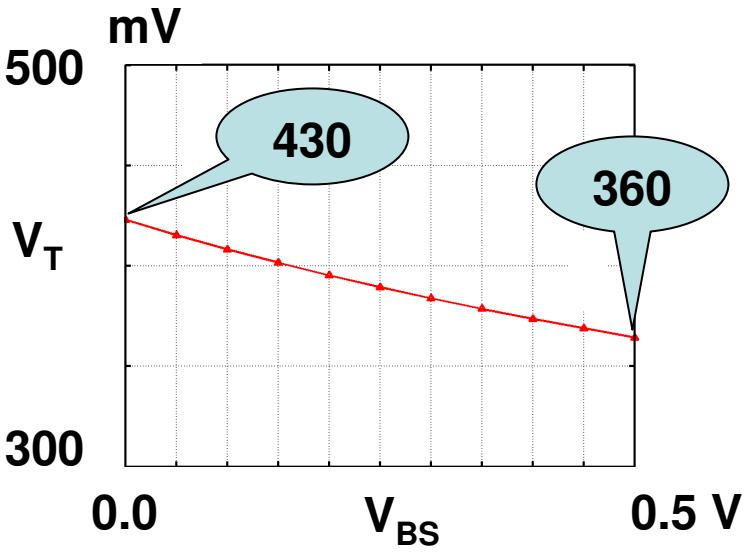
nMOS cross section (deep n-well process)

Opportunities at 0.5 V

- Body terminal
  - Signal input: [Guz87]
  - V_T reduction & control
    [Kob94], [Von94]
  - Bias control
- Latch-up not an issue
  - Assuming V_{DD} and GND are 'well behaved'.
- Techniques can be ported to 'double gate' devices

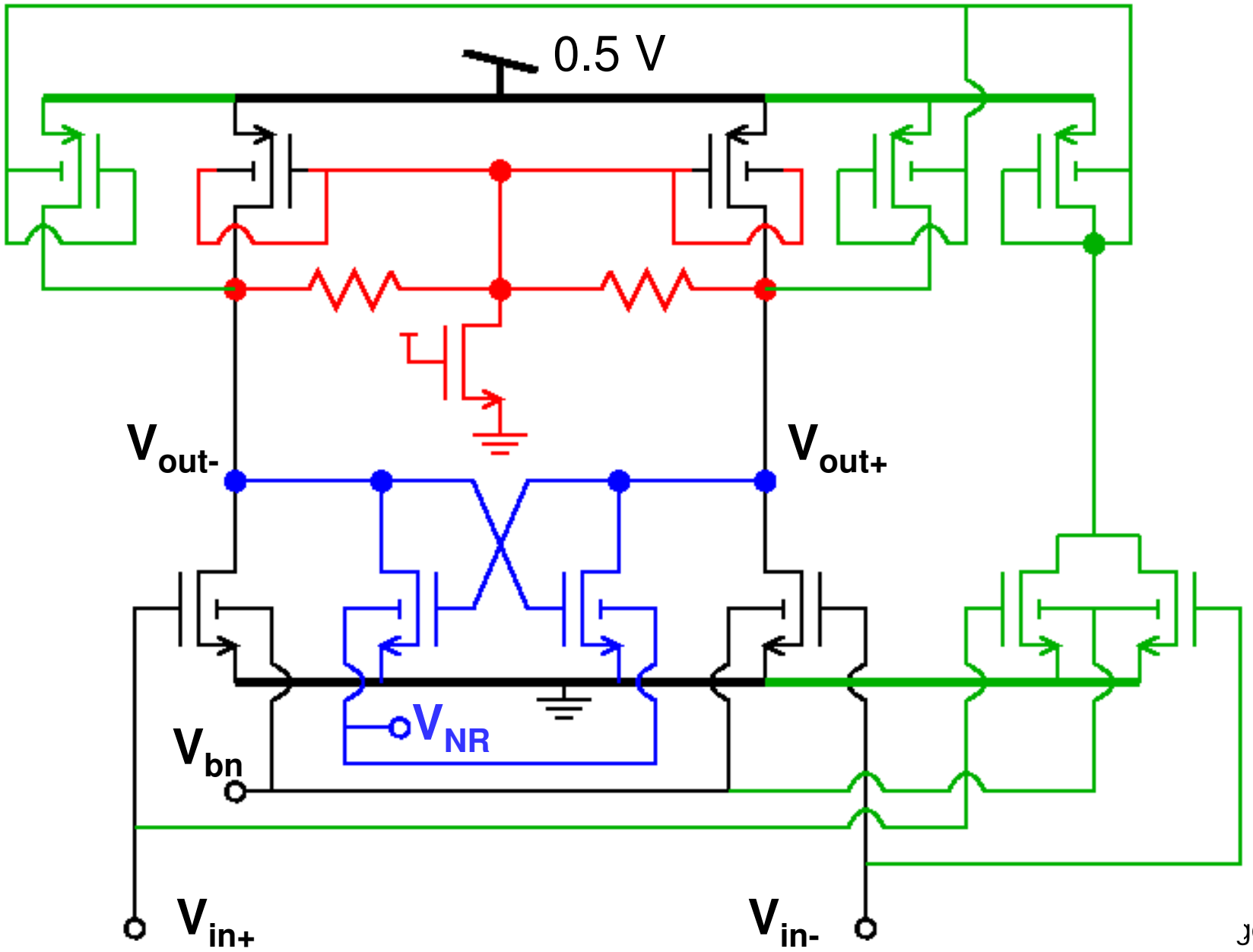
0.24µm/0.36µm nMOS in 0.18µm CMOS



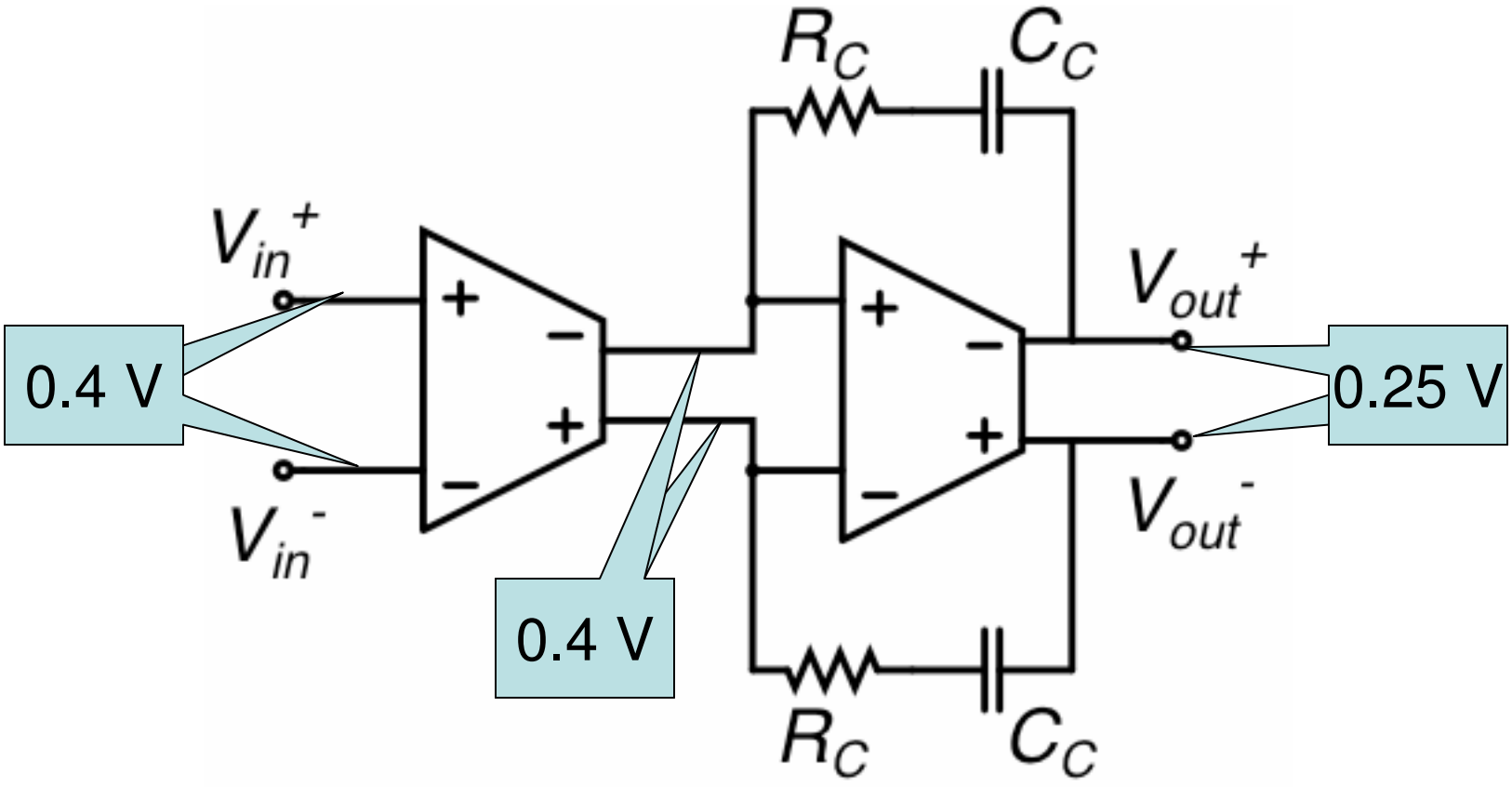


0.5 V Gate-input OTA

0.5 V Gate-input OTA stage

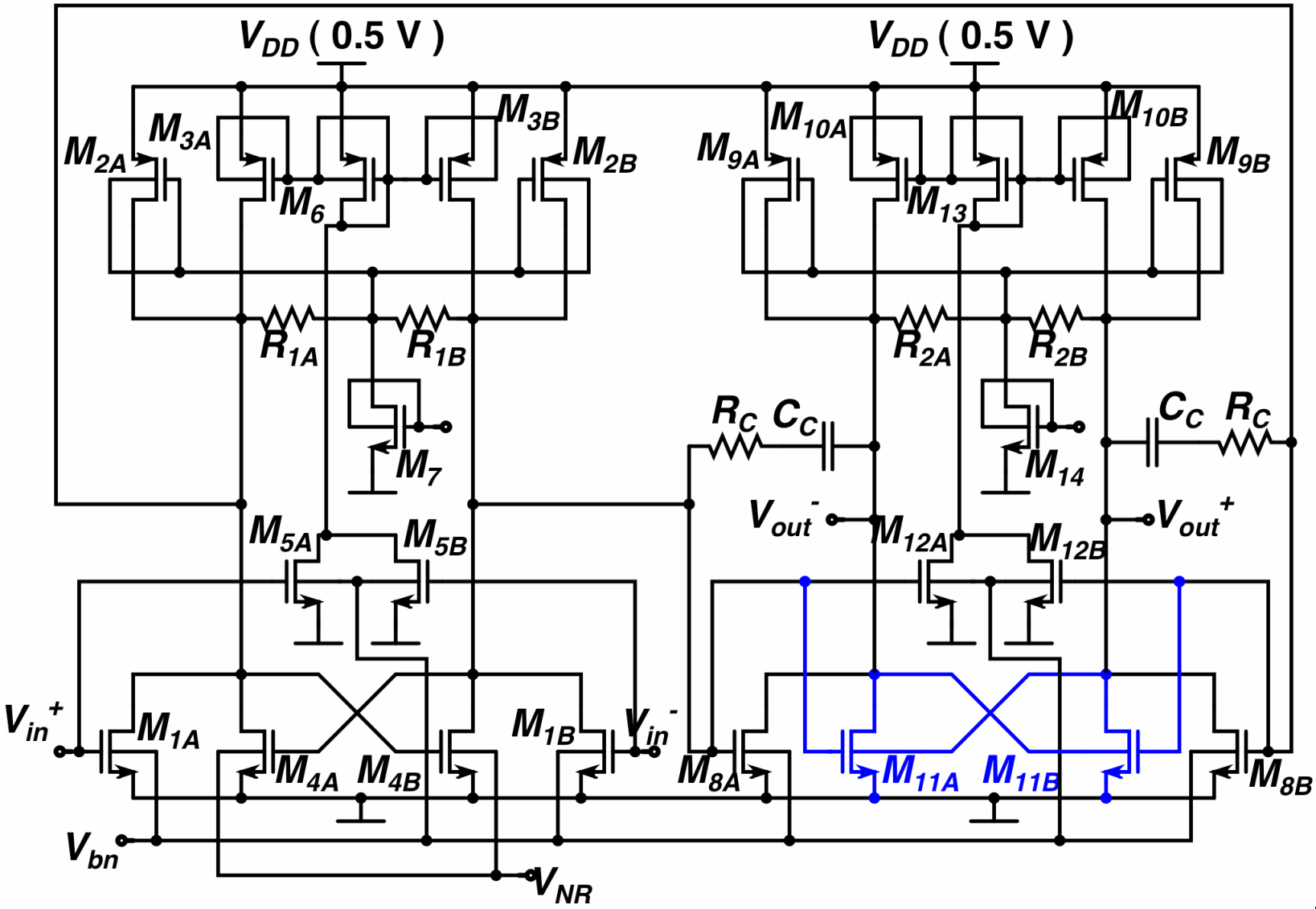


Two stage OTA

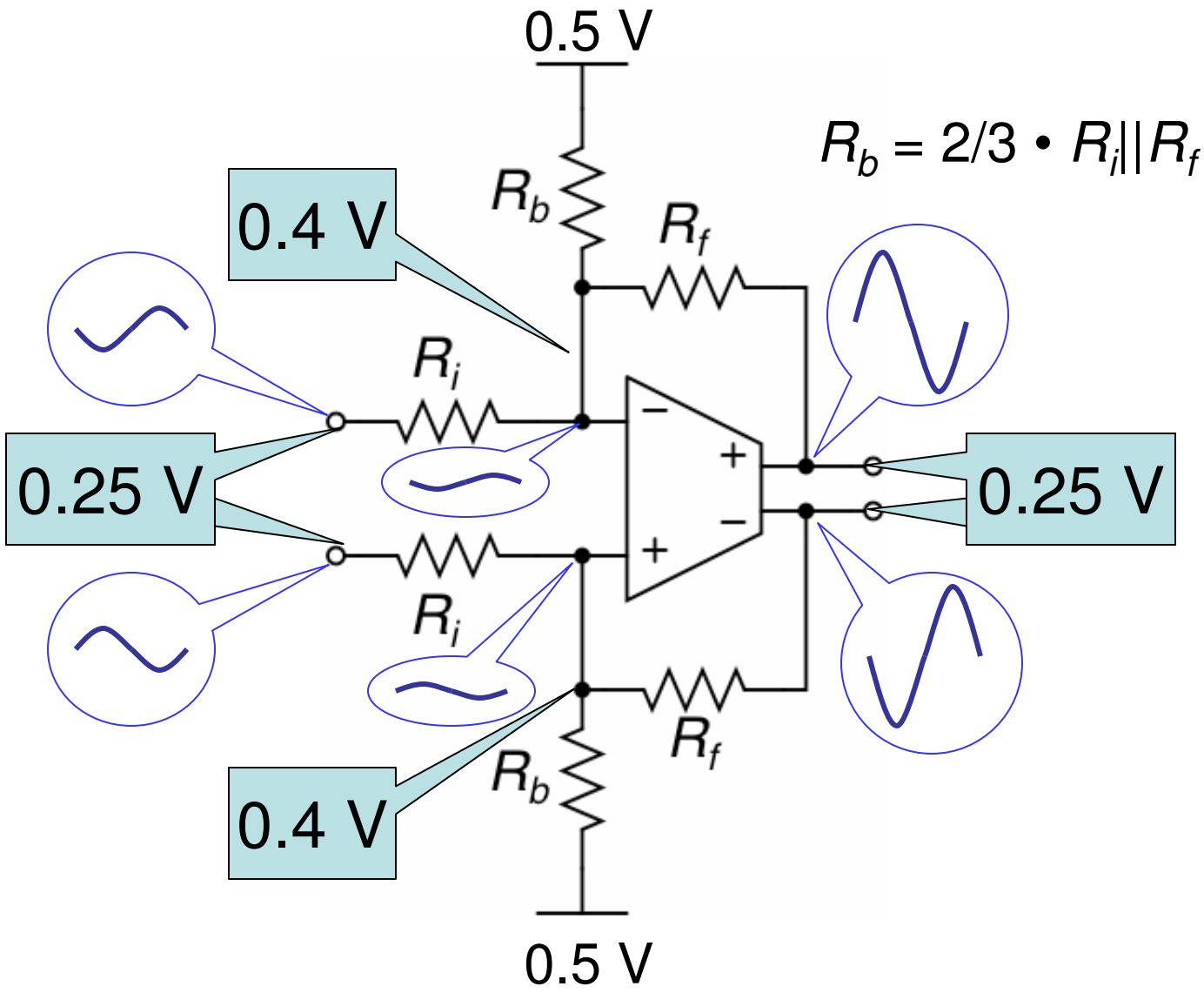


- Common-mode output of first stage is 0.4 V

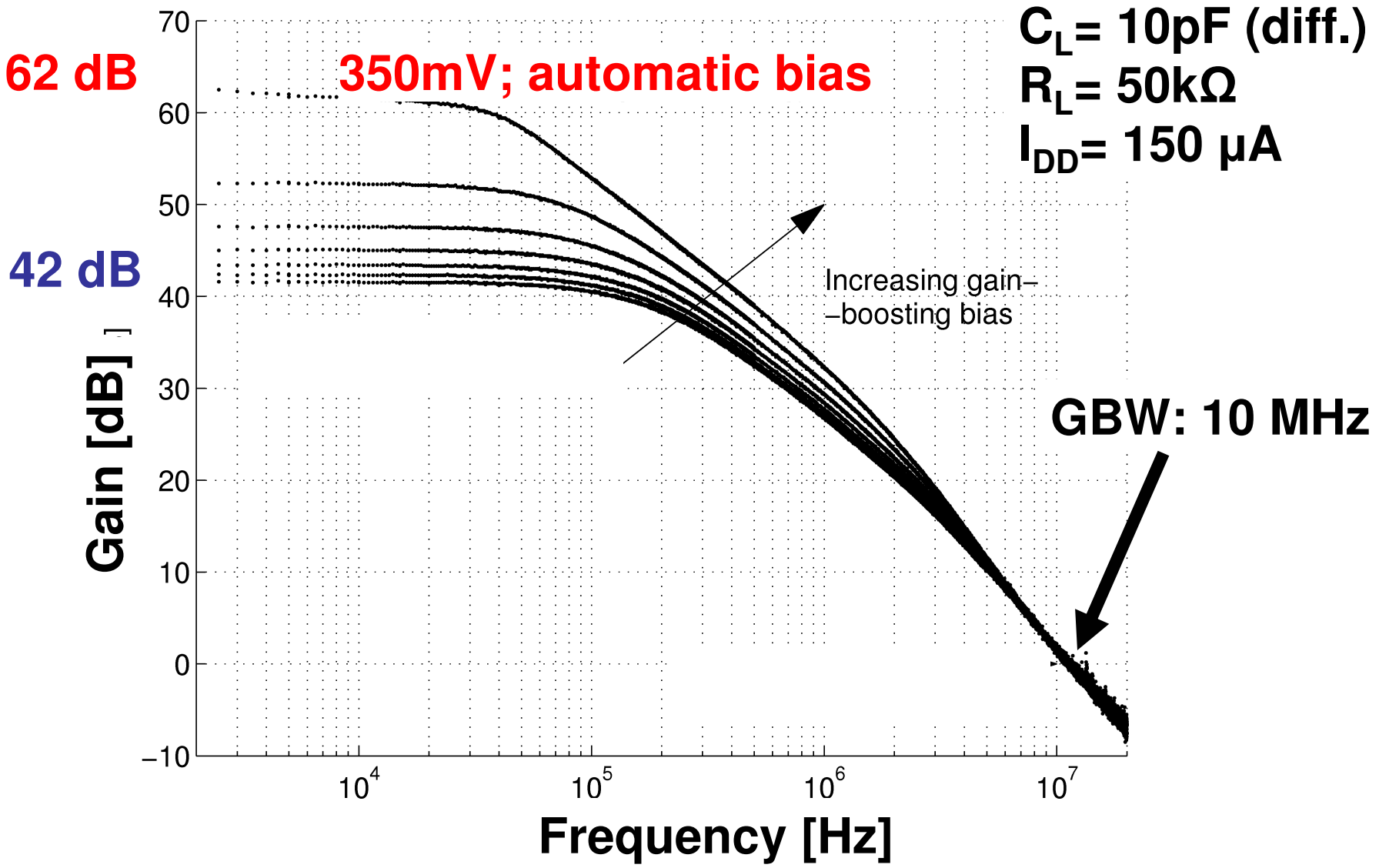
Two-stage fully differential 0.5 V OTA with Miller compensation



Setting common-mode voltages

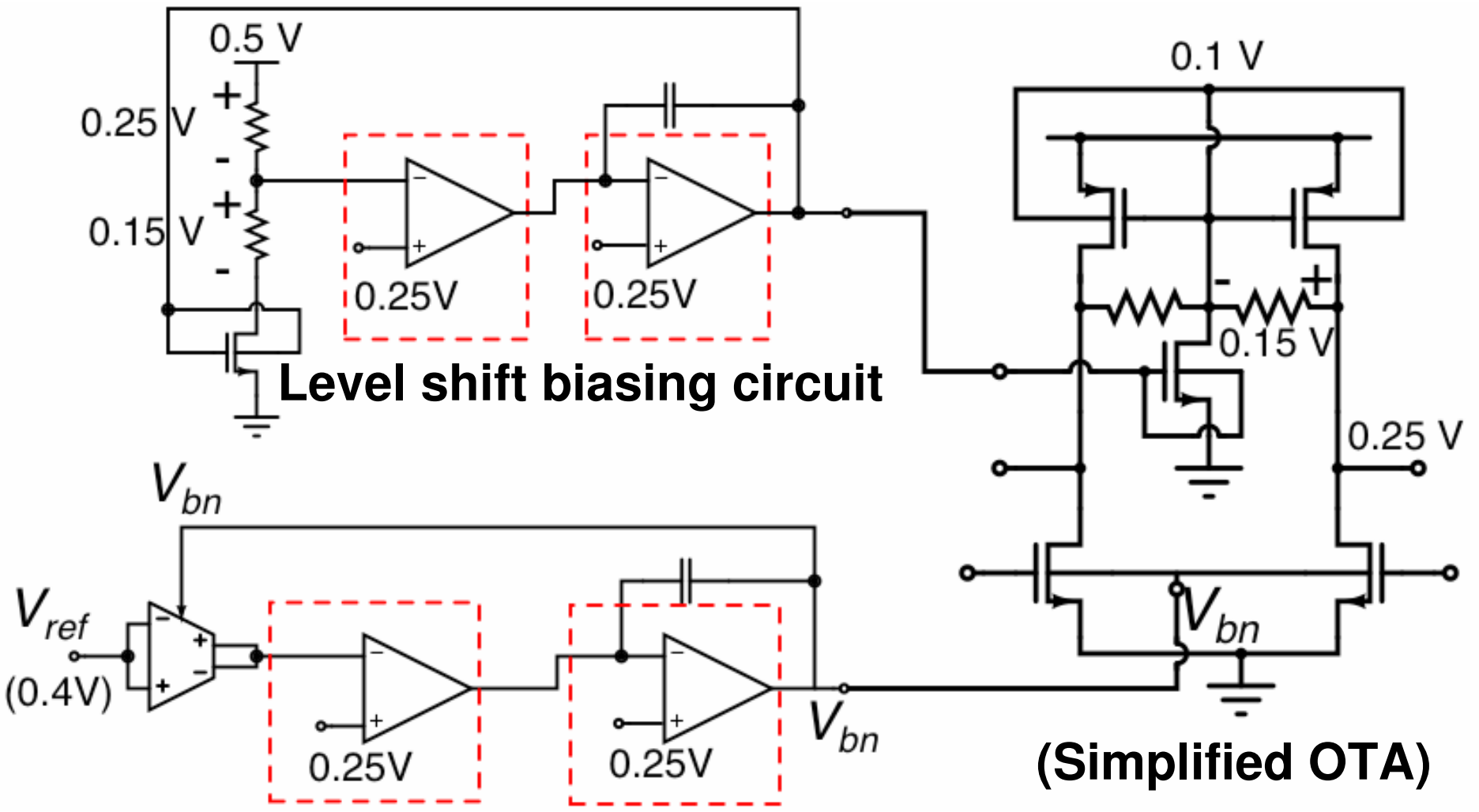


Open loop performance (meas.)

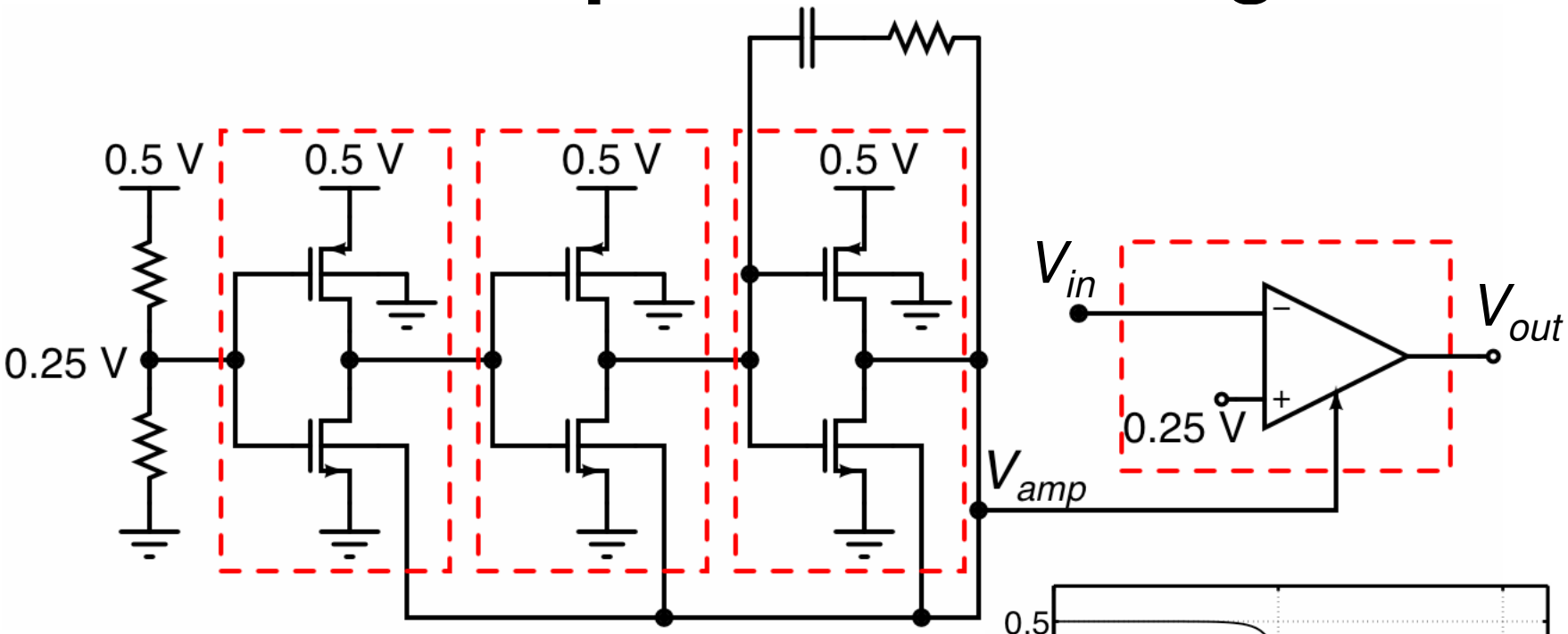


On-chip automatic biasing circuits

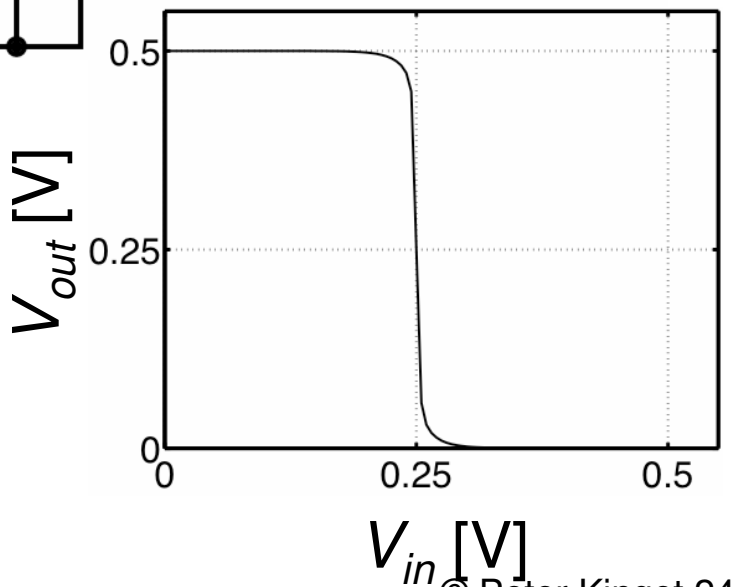
On-chip biasing circuits



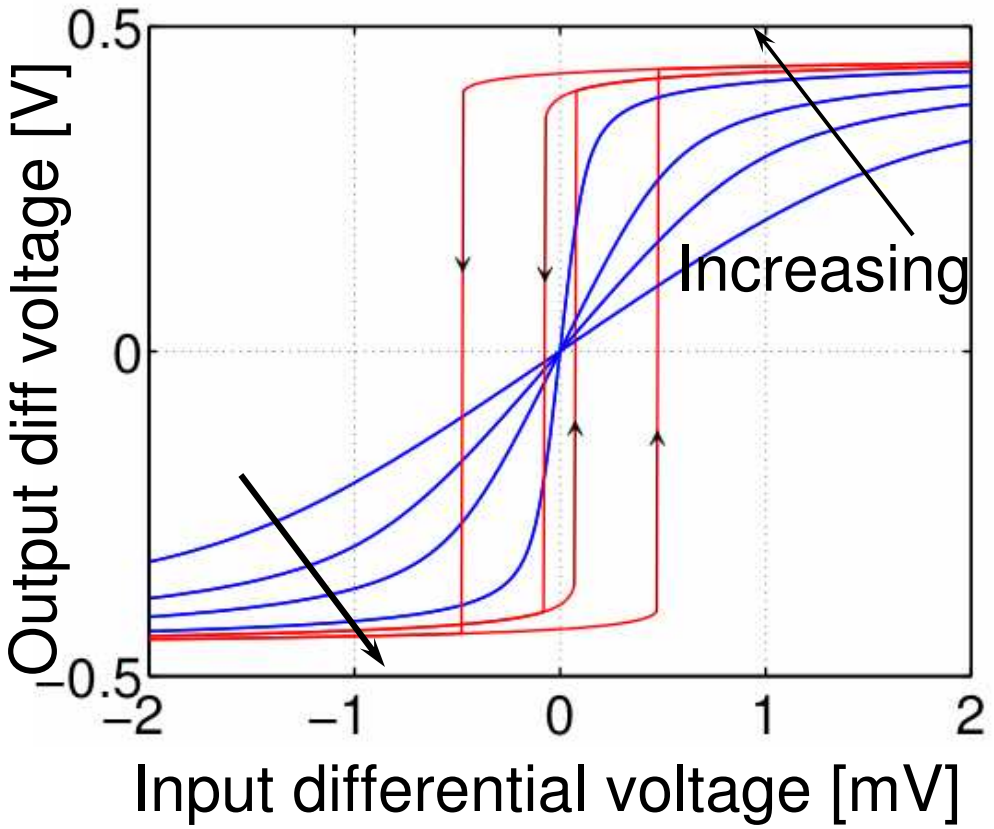
Error amplifier for biasing



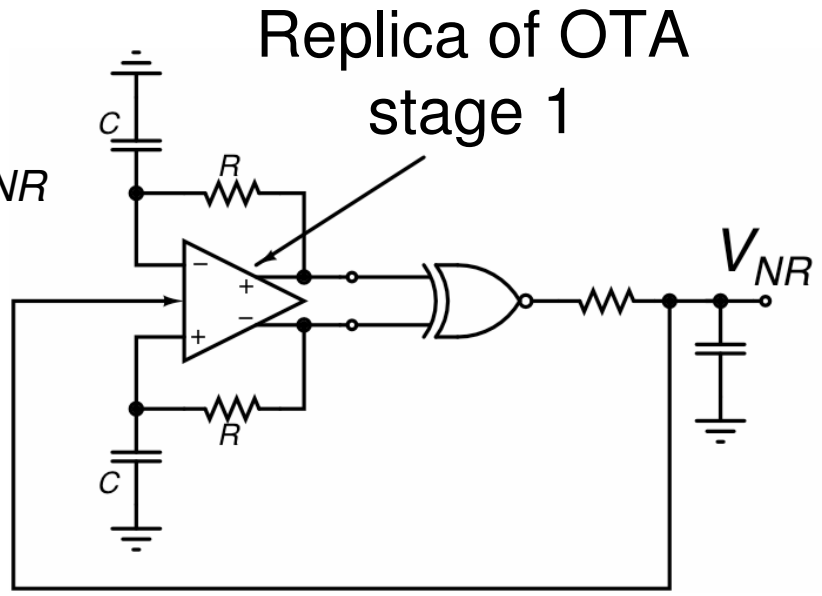
- 20 kHz GBW for 1 pF load
- 2 µA current
- Controlled body voltage sets the amplifier threshold



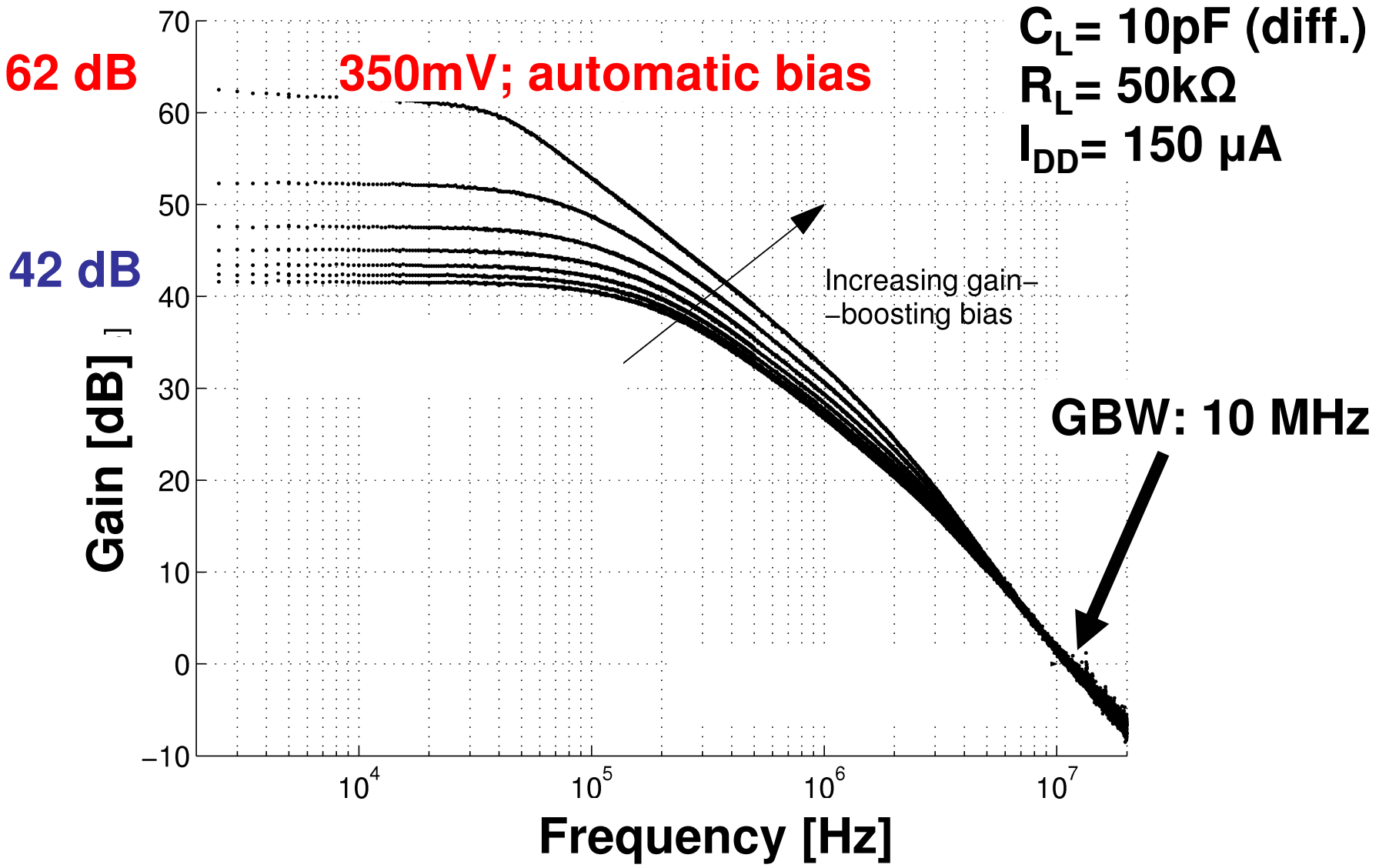
OTA DC transfer characteristics and V_{NR} generation



V_{NR} generating circuit

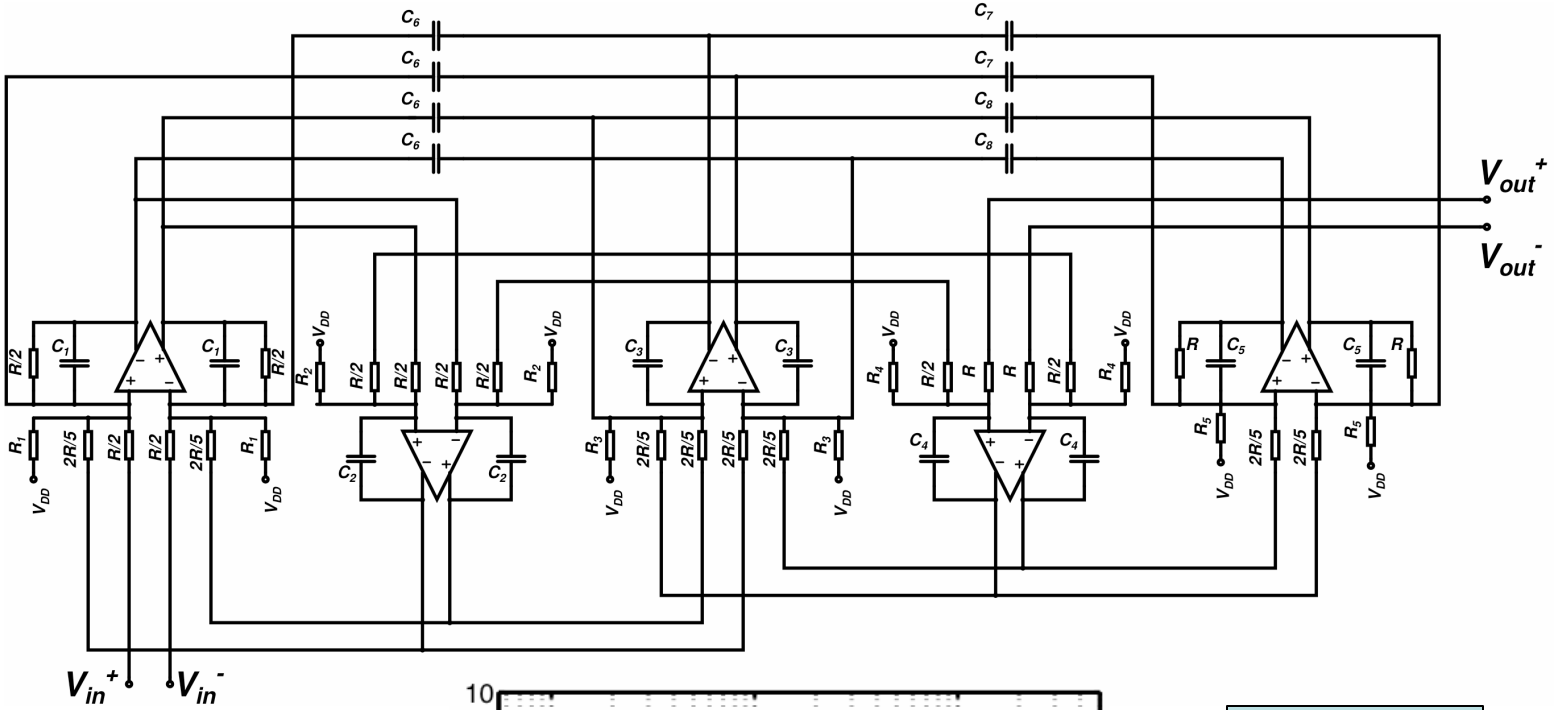


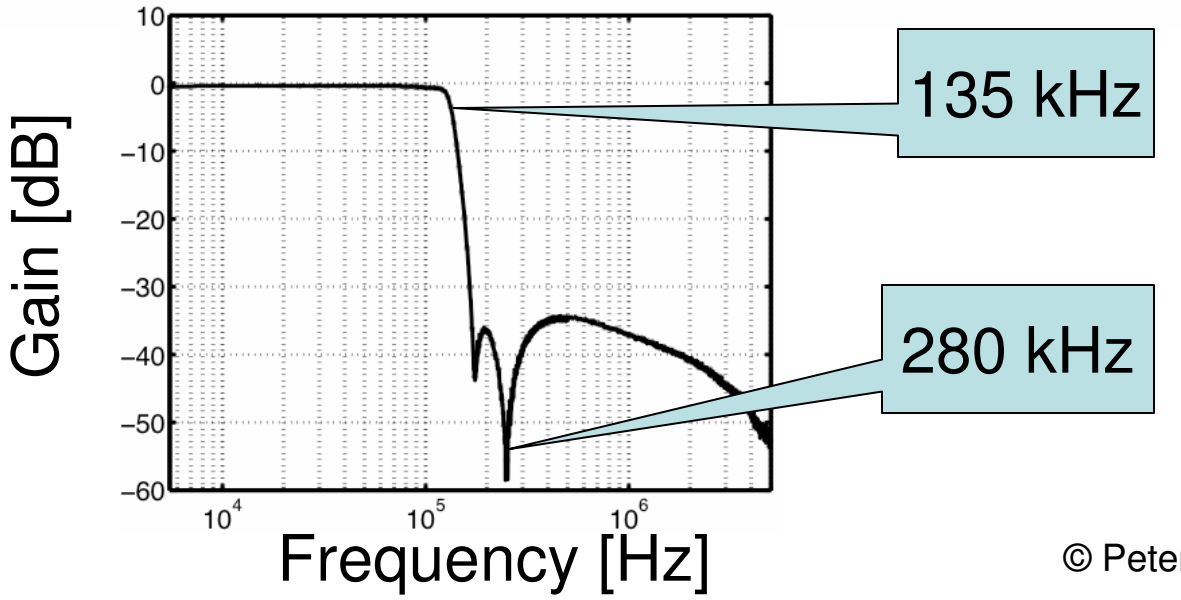
Open loop performance (meas.)



0.5 V Continuous time tunable active RC Filter

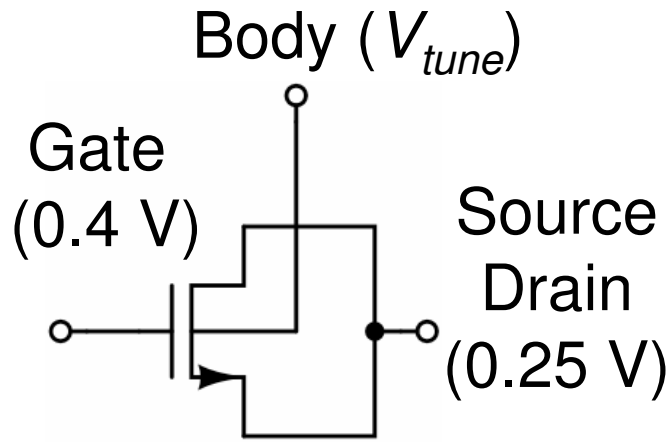
0.5 V 5th order elliptic LPF

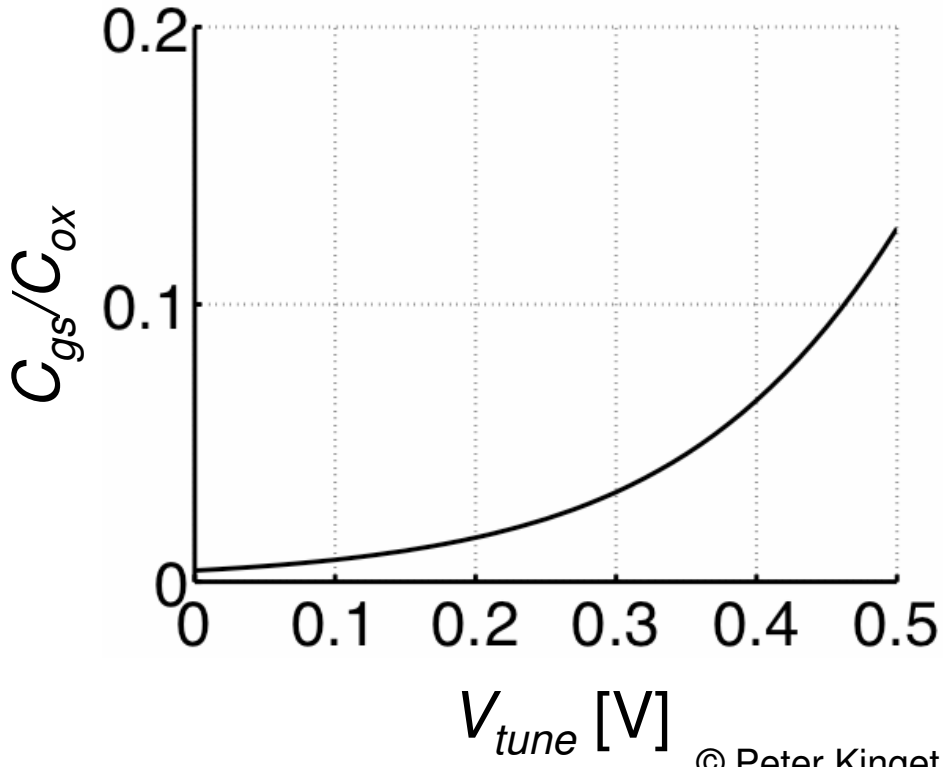




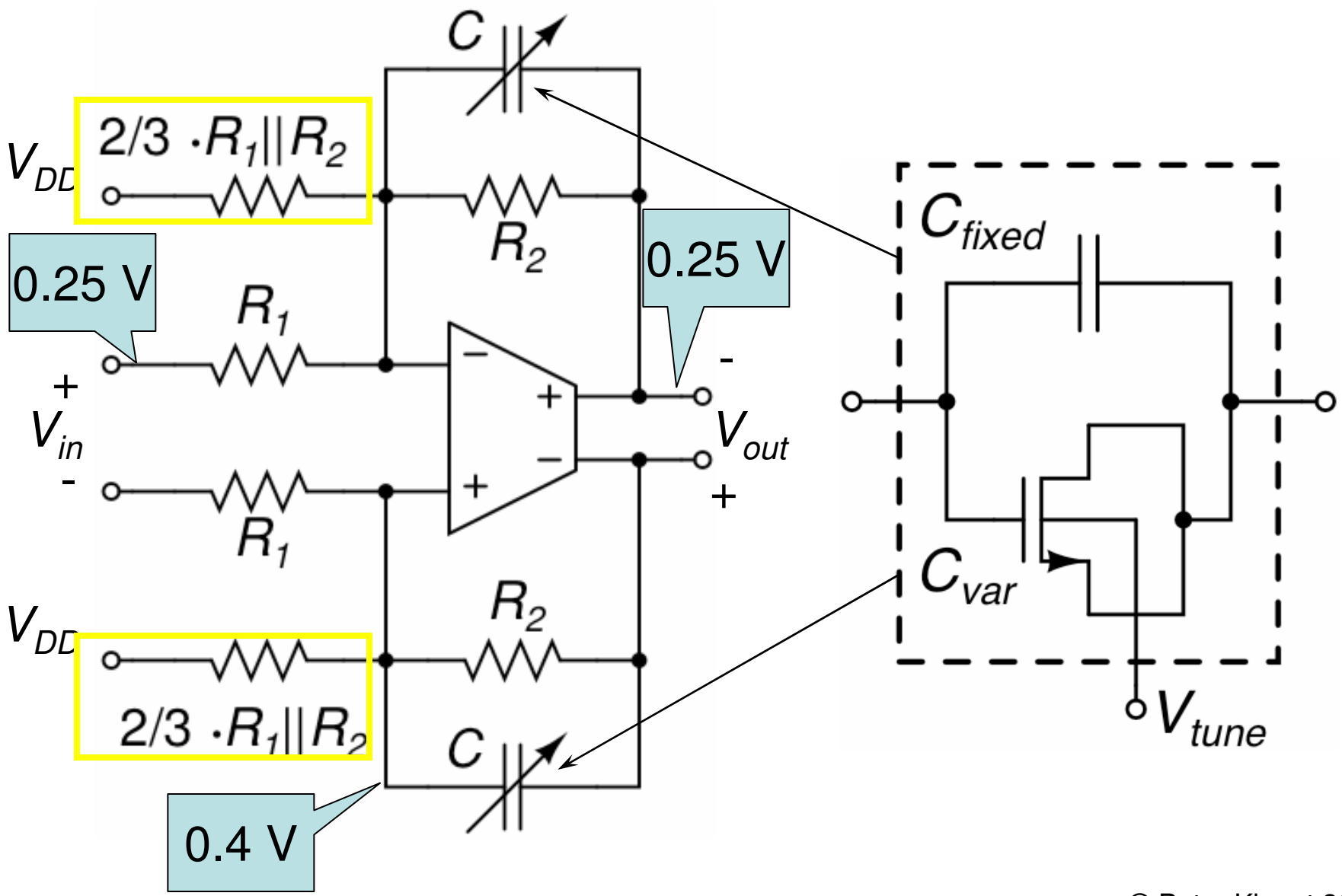
Filter tuning challenges at 0.5 V

- Gm-C
- MOSFET-C
- Switching banks of R's and C's
- **Varactor-R techniques**

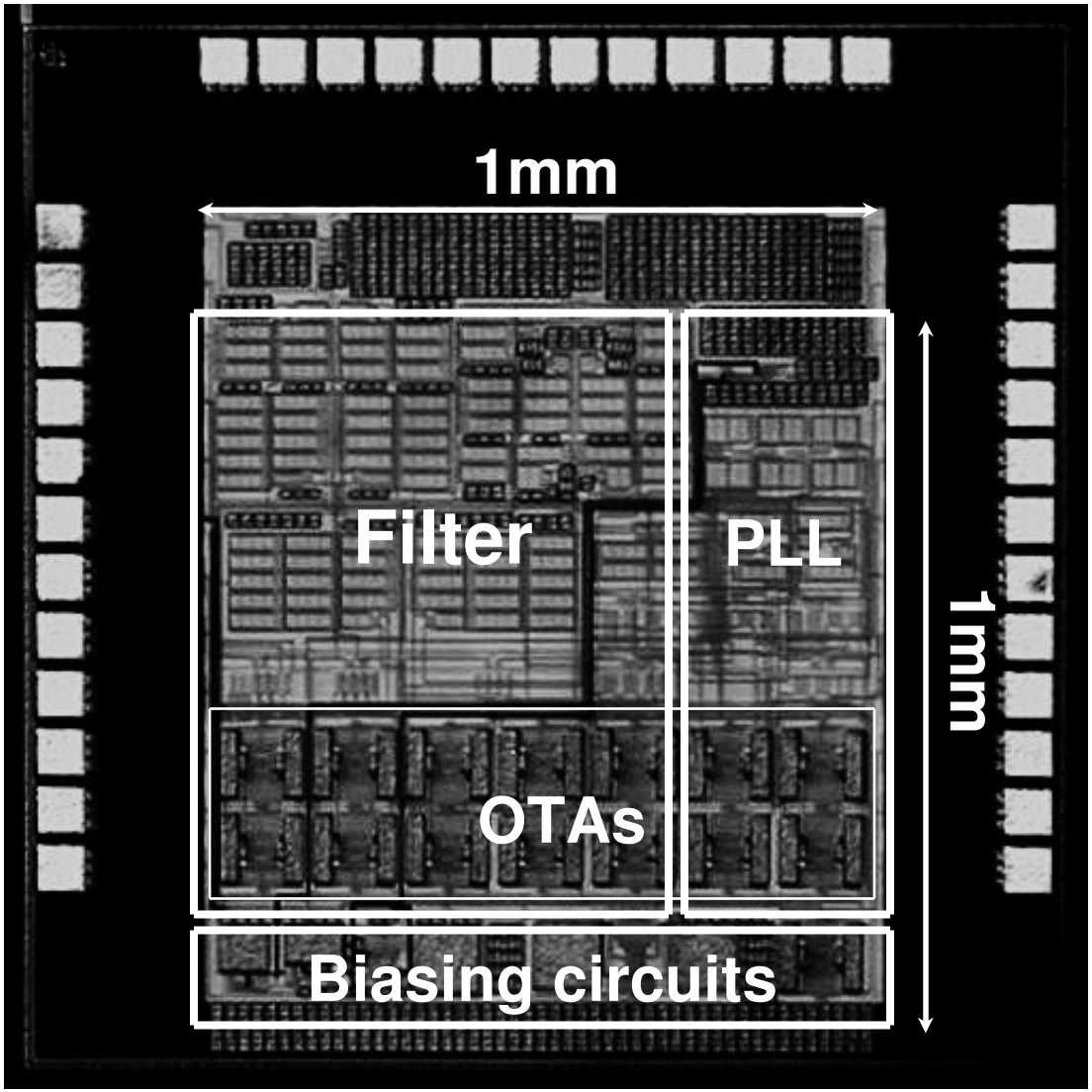




Low-voltage tunable integrator



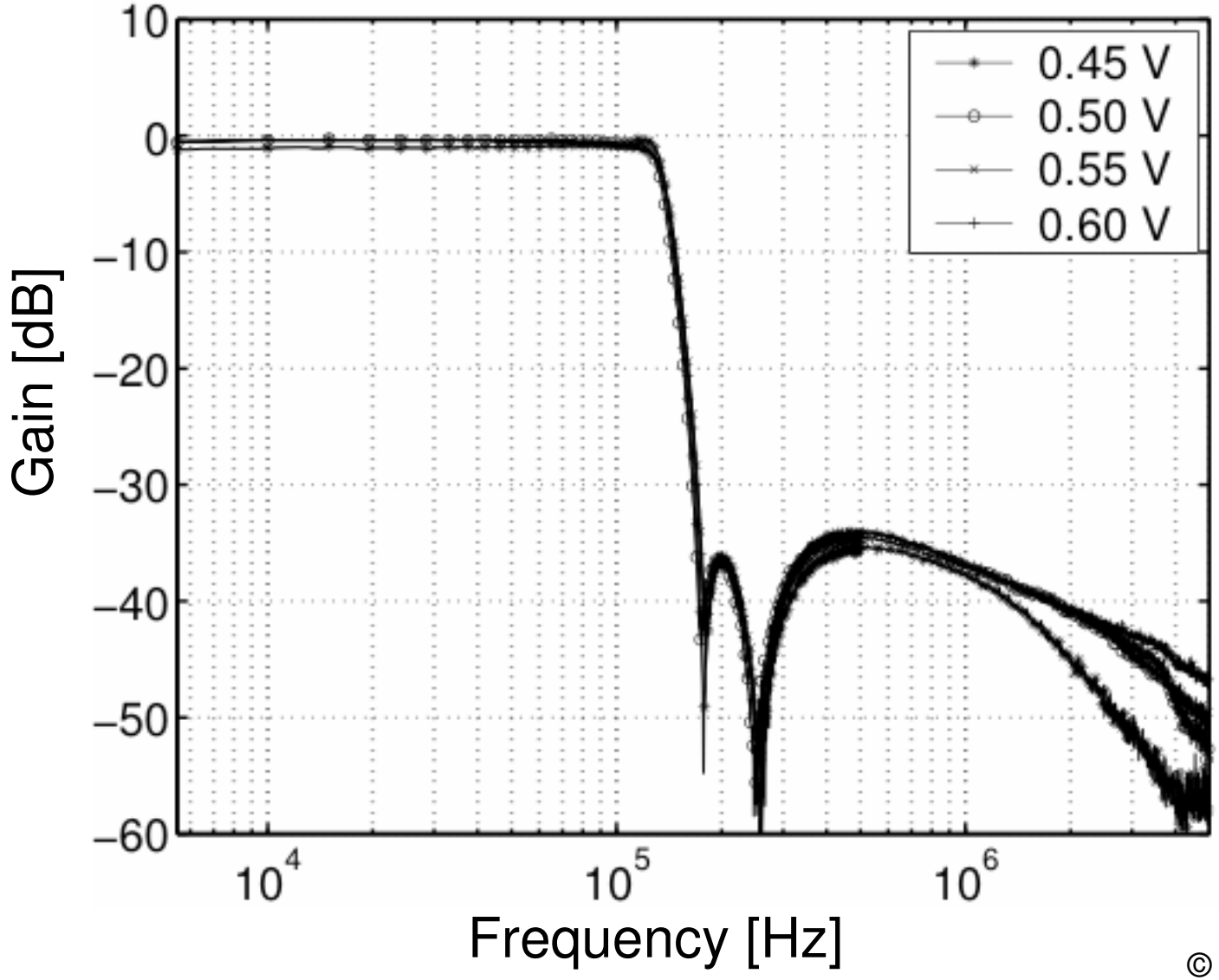
Die photograph



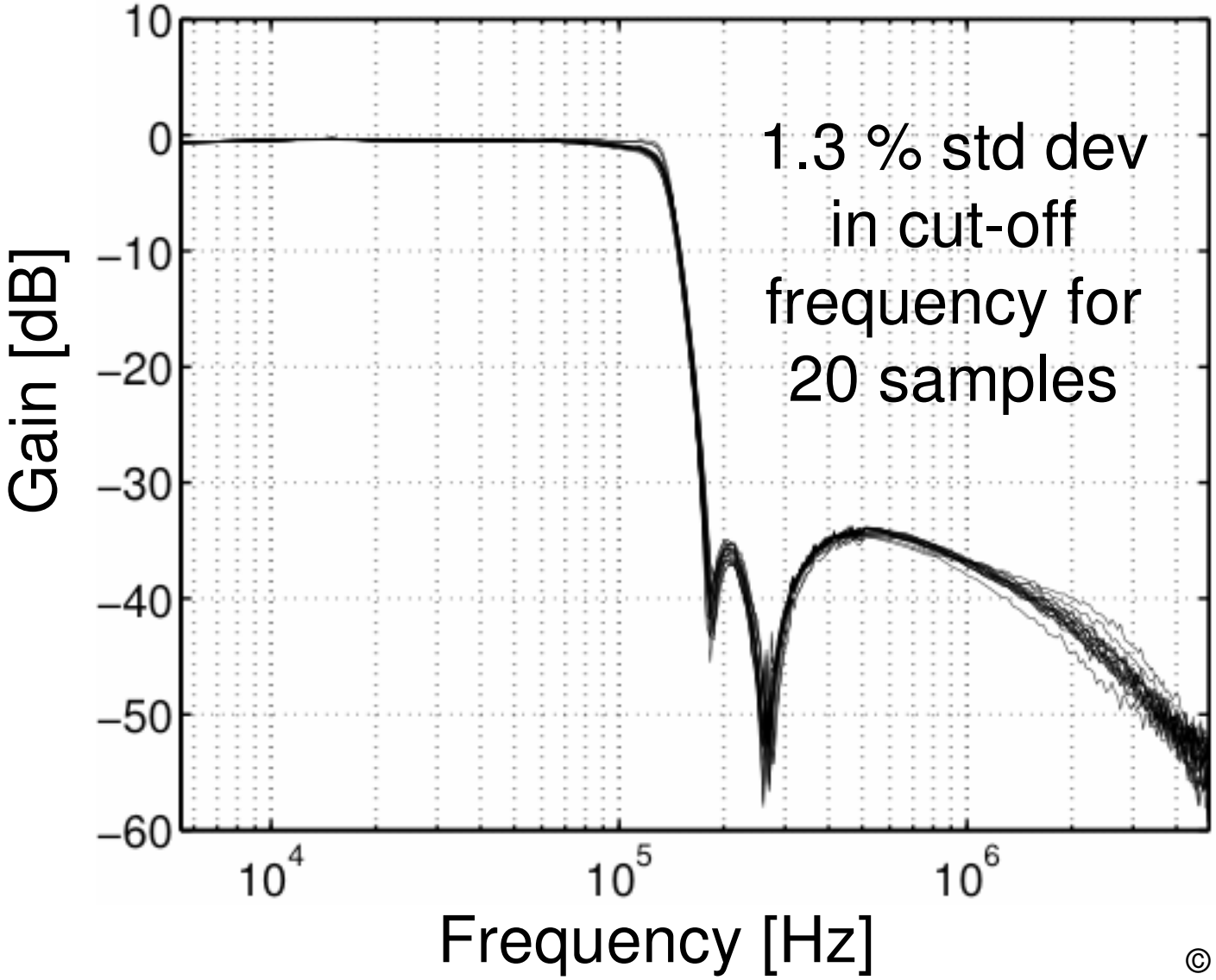
- 0.18 µm CMOS
- MIM capacitors
- High-res resistors
- Standard V_T
- Triple well devices

S. Chatterjee, Y. Tsividis, and P. Kinget, *"A 0.5 V filter with PLL-based tuning in 0.18 um CMOS technology,"* in IEEE International Solid-State Circuits Conference (ISSCC), pp. 506-507, February 2005.

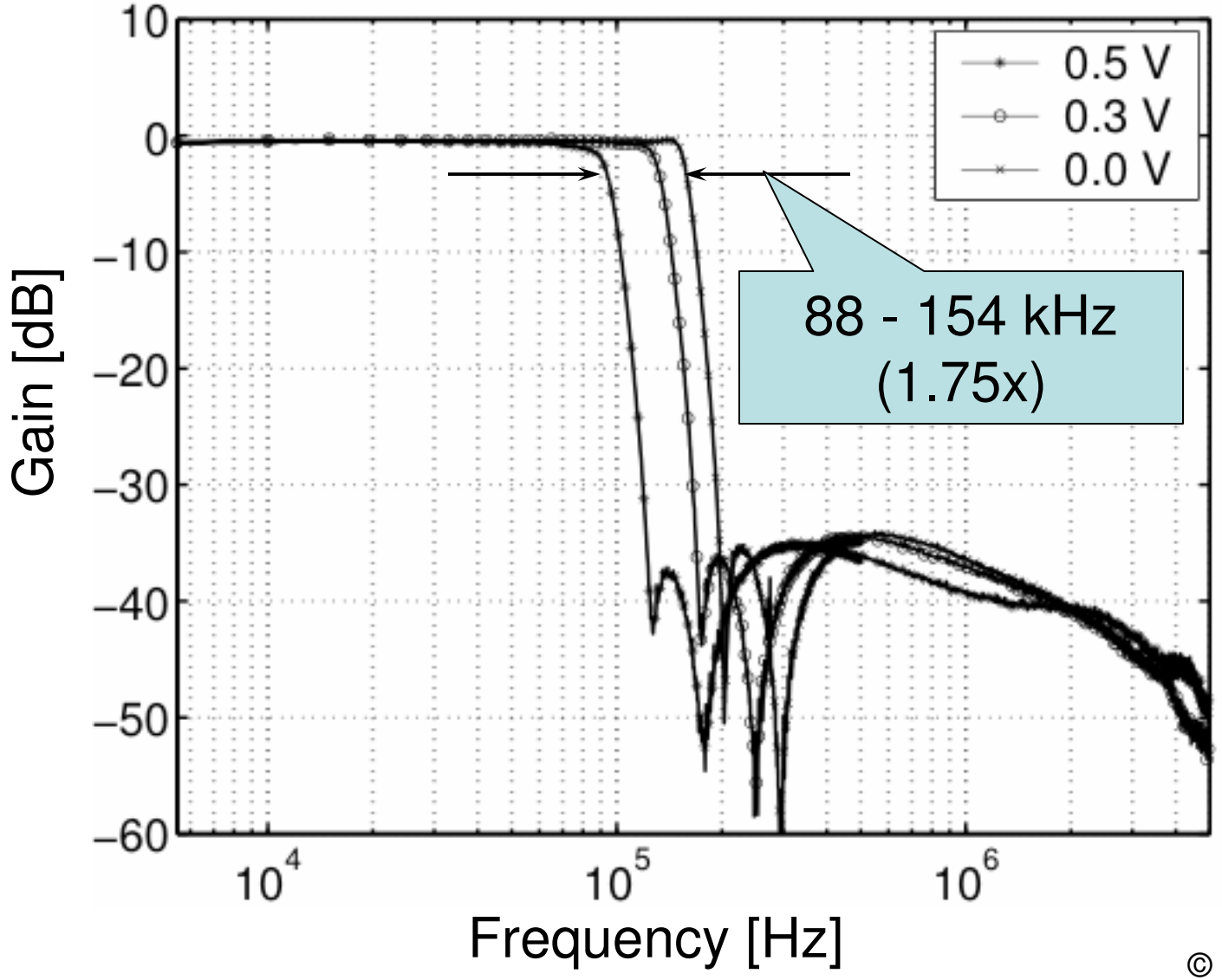
Measured filter response for different supply voltages



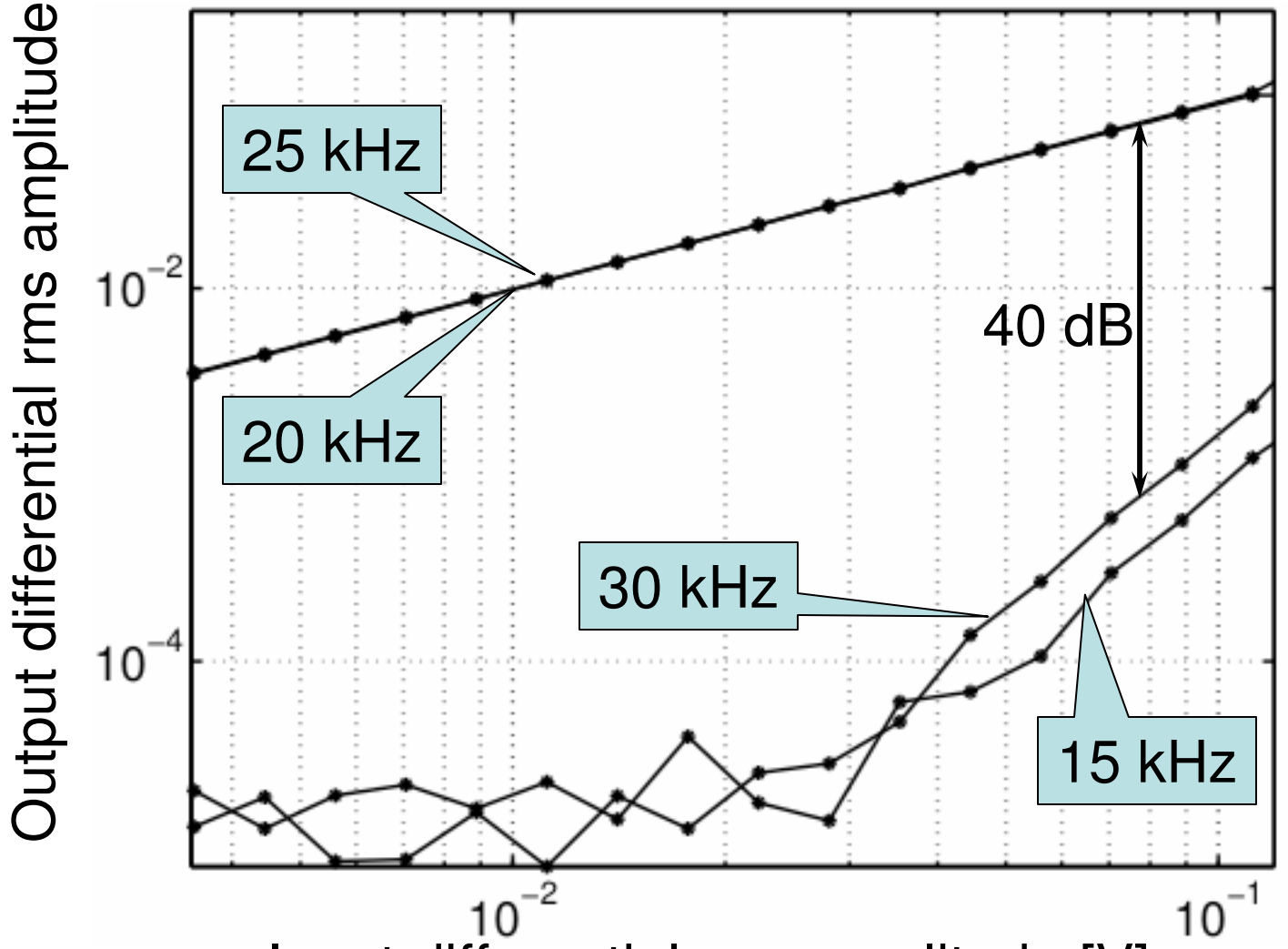
Measured filter response for different chips



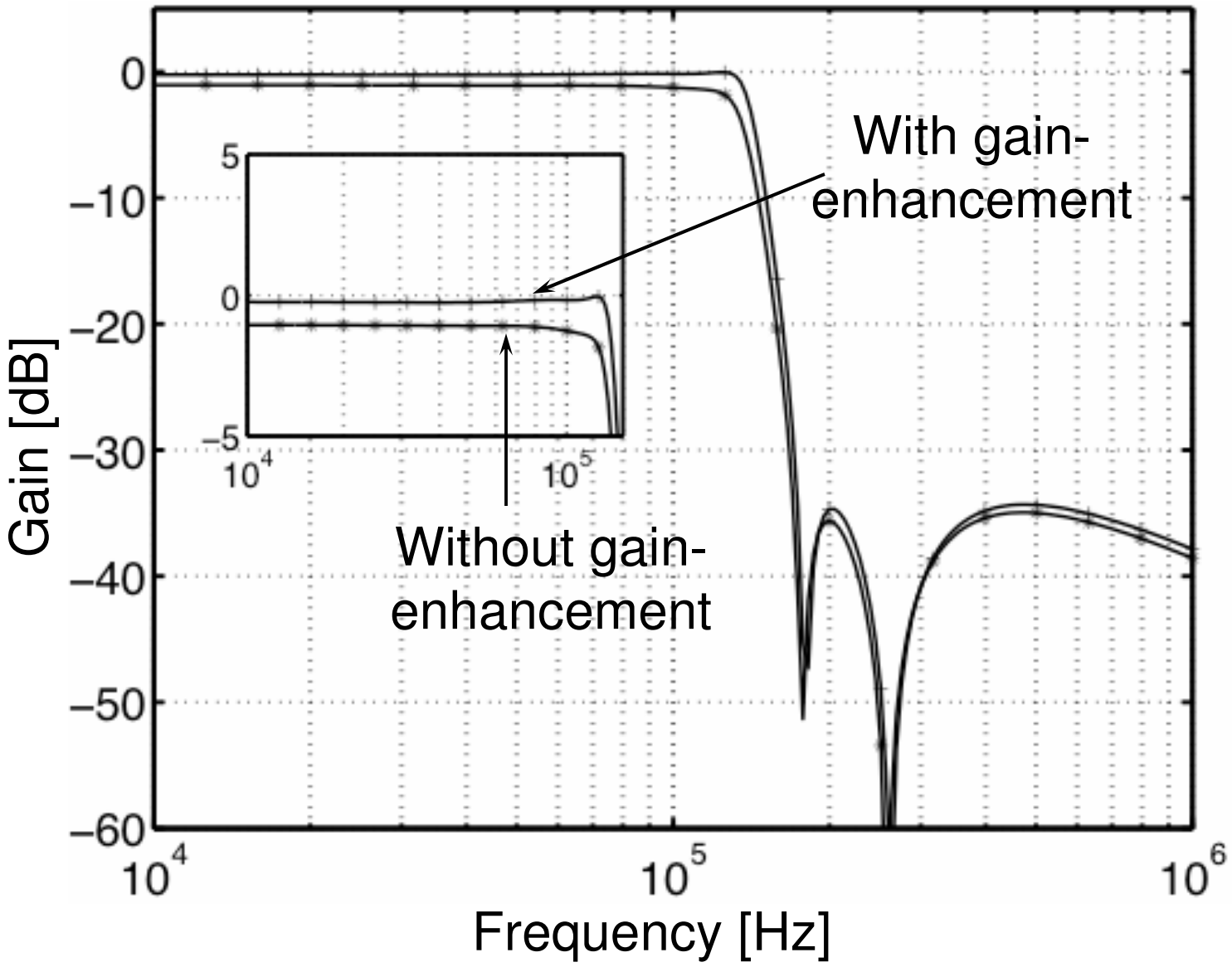
Measured filter response for different tuning voltages



Measured 3rd order inter-modulation



Effect of gain enhancement



Performance summary at 27C

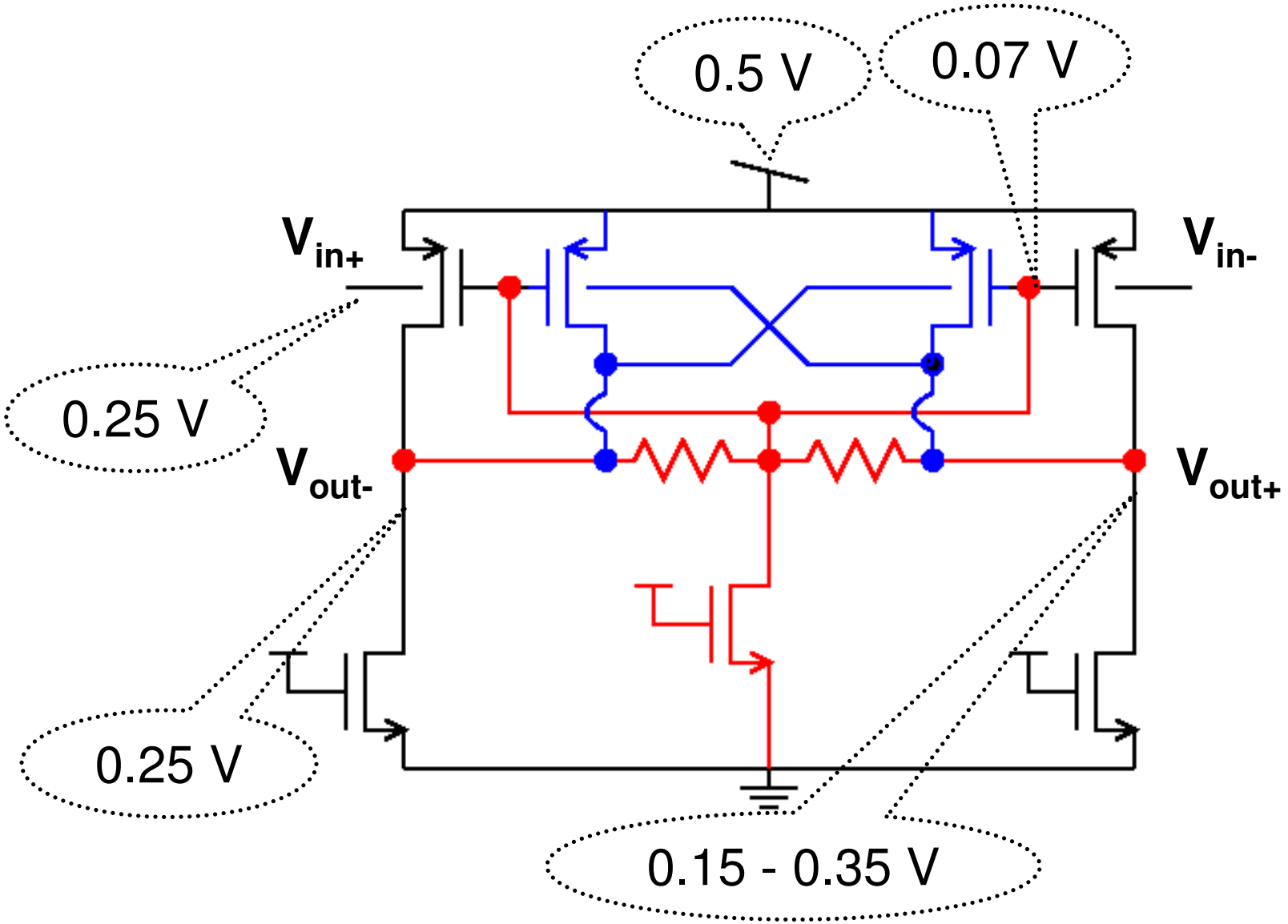
V_{DD} [V]	0.45	0.50	0.55	0.60
-3 dB cut-off frequency [kHz]	135.0	135.0	135.0	135.0
Total current [mA]	1.5	2.2	3.3	4.3
Noise [µV rms]	87	74	68	65
Input [mV rms] (100kHz / 1% THD)	50	50	50	50
In-band IIP_3 [dBV]	-5	-3	-3	-3
Out-of-band IIP_3 [dBV]	3	5	3	5
Dynamic range [dB]	55	57	57	58
Tuning range [kHz] $V_{tune} = V_{DD}$	96.5	88.0	84.5	69.0
V_{tune} = 0.0 V	153.0	154.5	148.0	150.5
VCO feed-thru @280kHz [µV rms]	104	85	72	72

- Measured CMRR (10 kHz common mode tone): 65 dB
- Measured PSRR (10 kHz tone on power supply): 43 dB

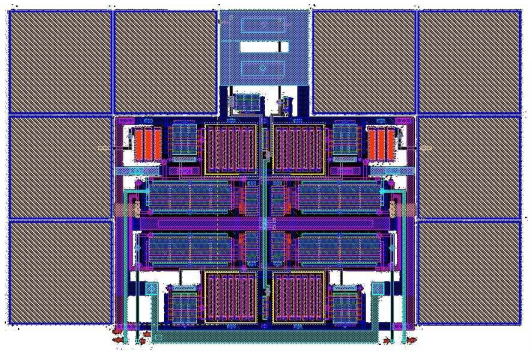
Functionality tested from 5C to 85C at 0.5 V

0.5 V Body-input OTA

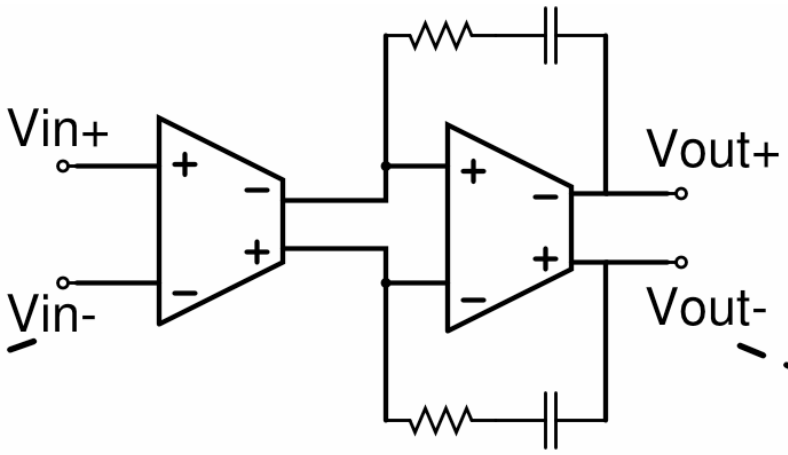
0.5 V Body-input OTA stage



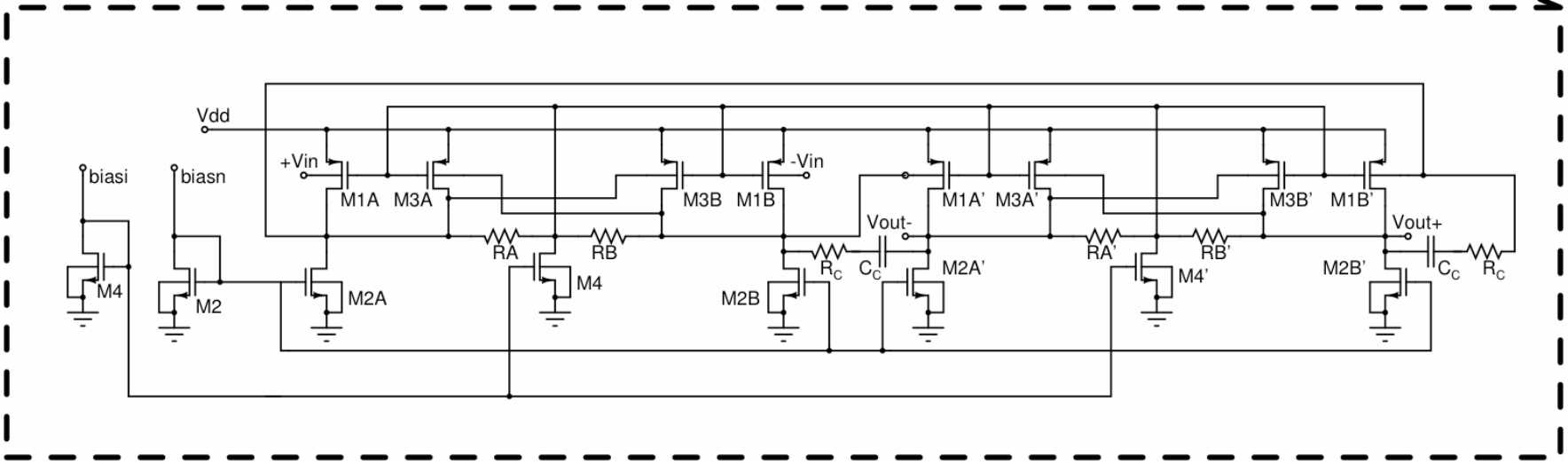
Two-stage fully-differential OTA



0.18 μm CMOS

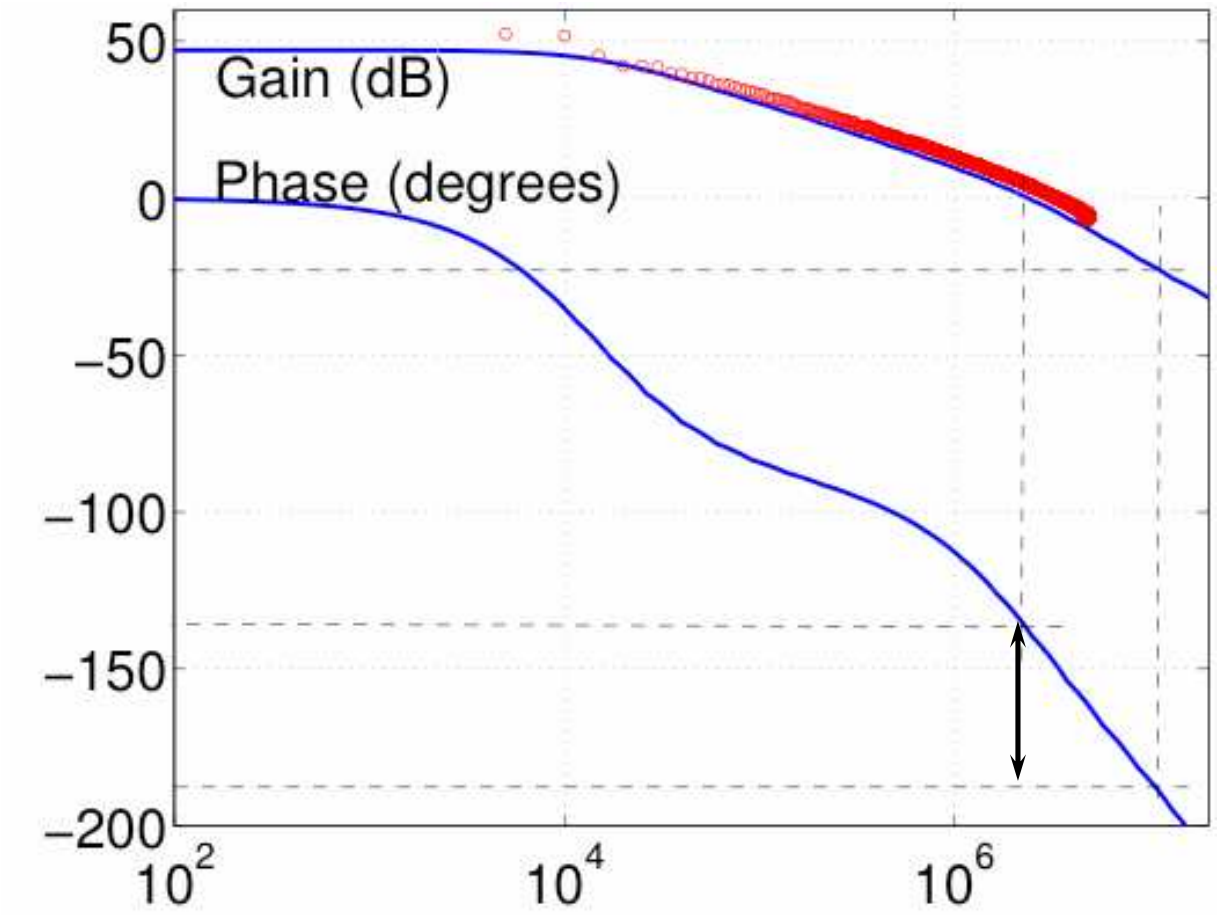


Pole splitting using
Miller capacitor



S. Chatterjee, Y. Tsividis, and P. Kinget, *"A 0.5 V bulk input fully differential operational transconductance amplifier,"* in European Solid-State Circuits Conference (ESSCIRC), pp.147-150, September 2004.

Open loop frequency response



DC gain: 52 dB

GBW: 2.5 MHz

Measurement

Simulation

Phase Margin: 45^0

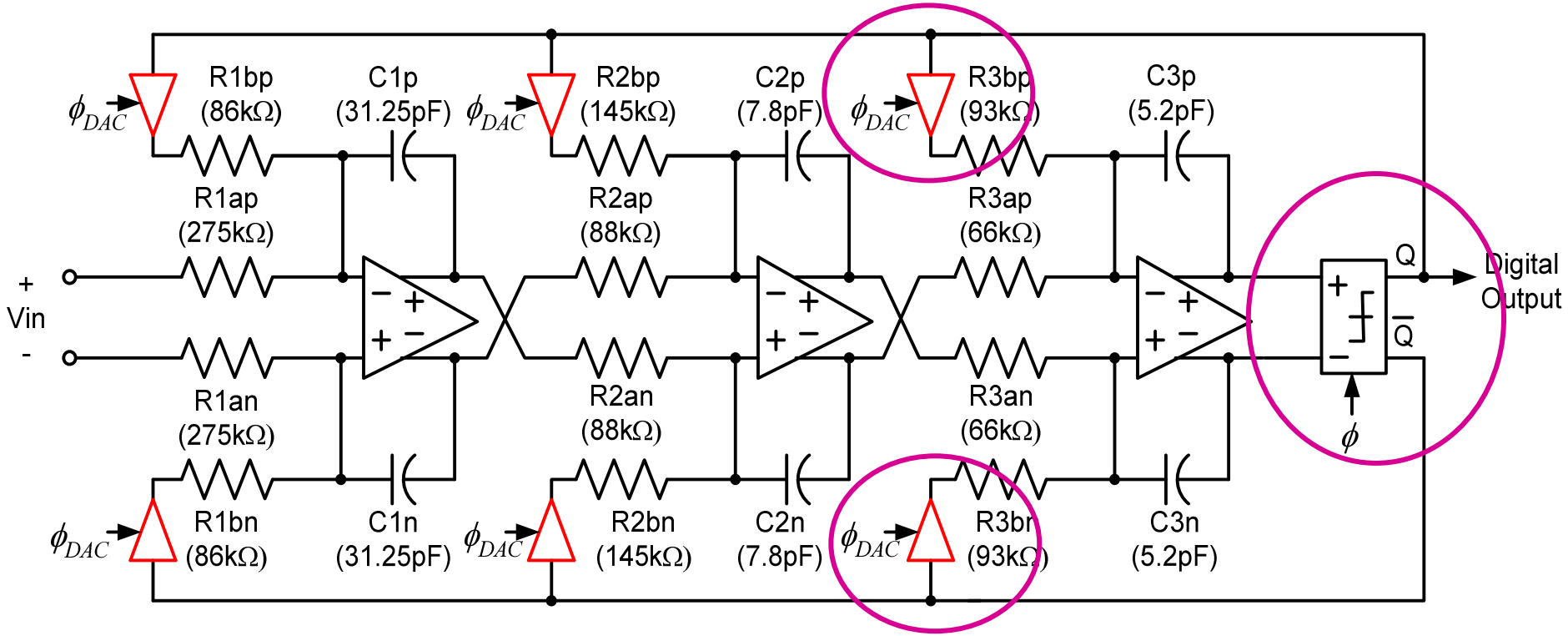
	[Bla 98]	[Las 00]	[Leh 01]	[Sto 02]	[Fer 96]	[Pel 98]	B-I	G-I
V_{DD} [V]	1	1	0.8	0.9	1.3	0.9	0.5	0.5
A_{DC} [dB]	49	70	53	70	84	59	52	50/62
GBW [MHz]	1.3	0.2	1.3	6e-3	1.3	4	2.5	10
Power [uW]	300	5	-	0.5	460	-	110	75
C_L [pF]	22	7	20	12	-	14	10	10
SE/Diff.	S	S	S	S	S	D	D	D
Techn. [um]	2	0.35	0.5	2.5	0.7	0.5	0.18	0.18
Special Devices	Lat. BJT	-	Lat. BJT	Depl. MOS	-	-	-	-
100 η [1/V]	9.5	28		13			11.4	66.7

S. Chatterjee, Y. Tsividis and P. Kinget, *"0.5 V Analog Circuit Techniques and Their Application in OTA and Filter Design,"* IEEE Journal of Solid-State Circuits (JSSC), vol. 40, no 12, pp. 2373 - 2387, December 2005.

$$\eta = \frac{\mathrm{GBW} \cdot C_L}{I_{\mathrm{supply}}}$$

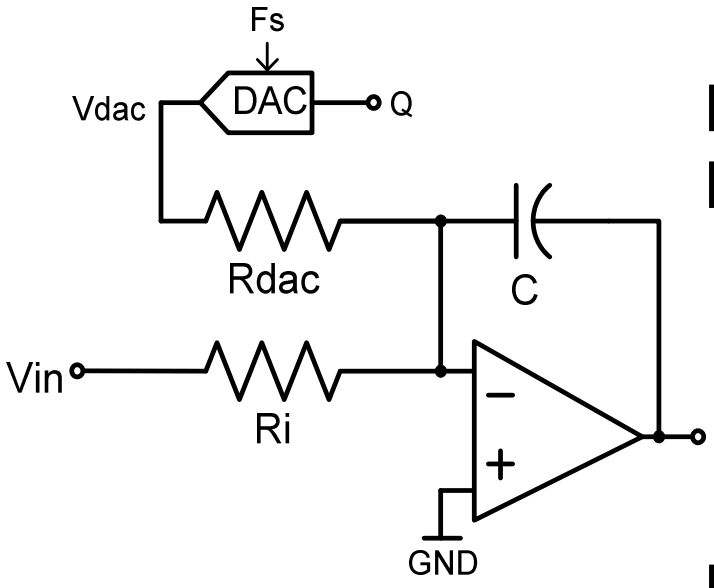
A 0.5V 74dB SNDR 25kHz CT ΣΔ Modulator with Return-to-open DAC

3rd order CT ΣΔ Modulator



Using Active RC integrators

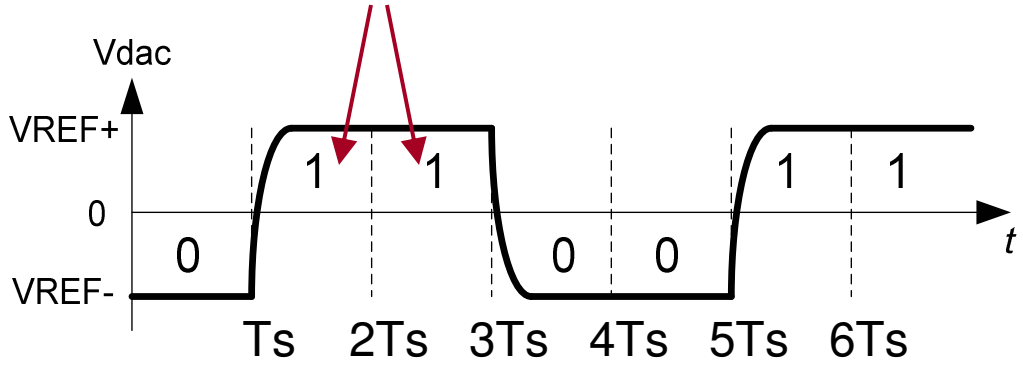
Continuous-time ΣΔ Modulator: Need of Return-to-zero DAC



A typical active-RC CT SDM stage

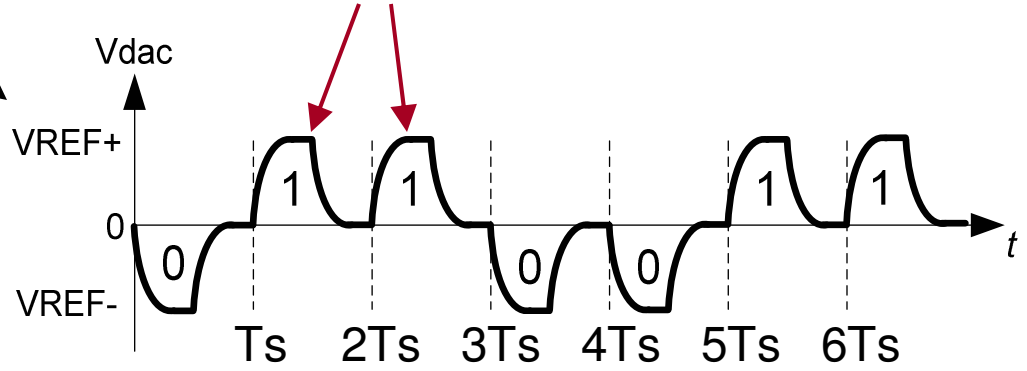
NRZ DAC

ISI exists: area for each "1" depends on its previous symbol.

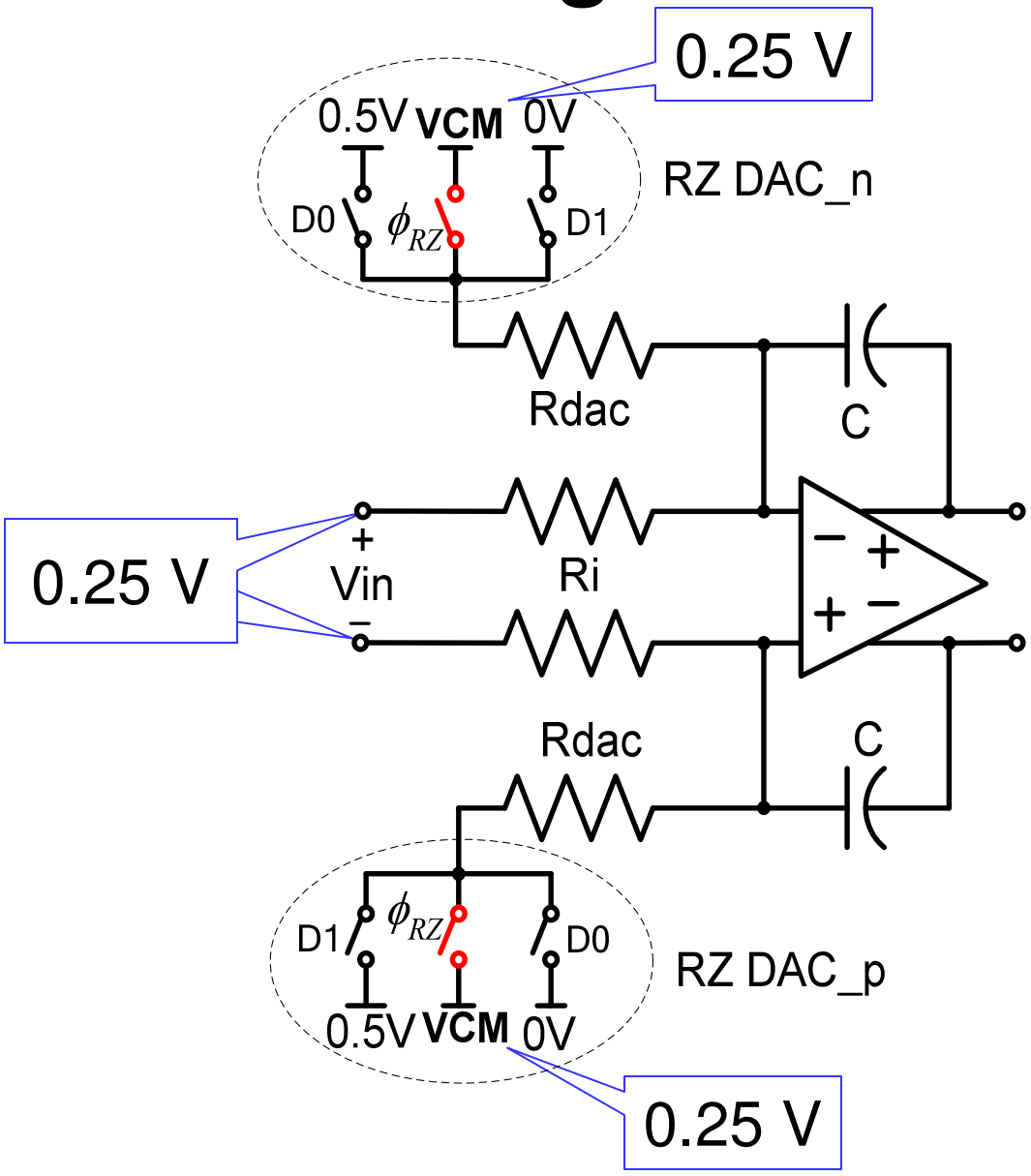


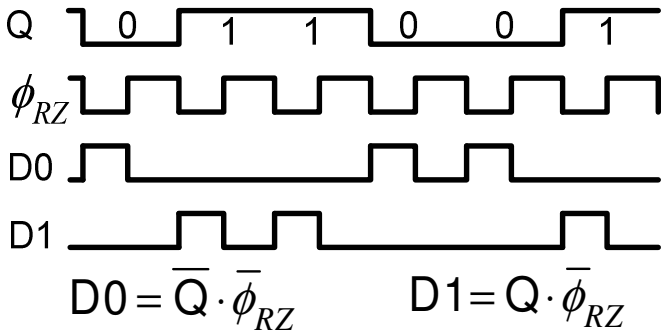
RZ DAC

No ISI: same area for all "1"s.



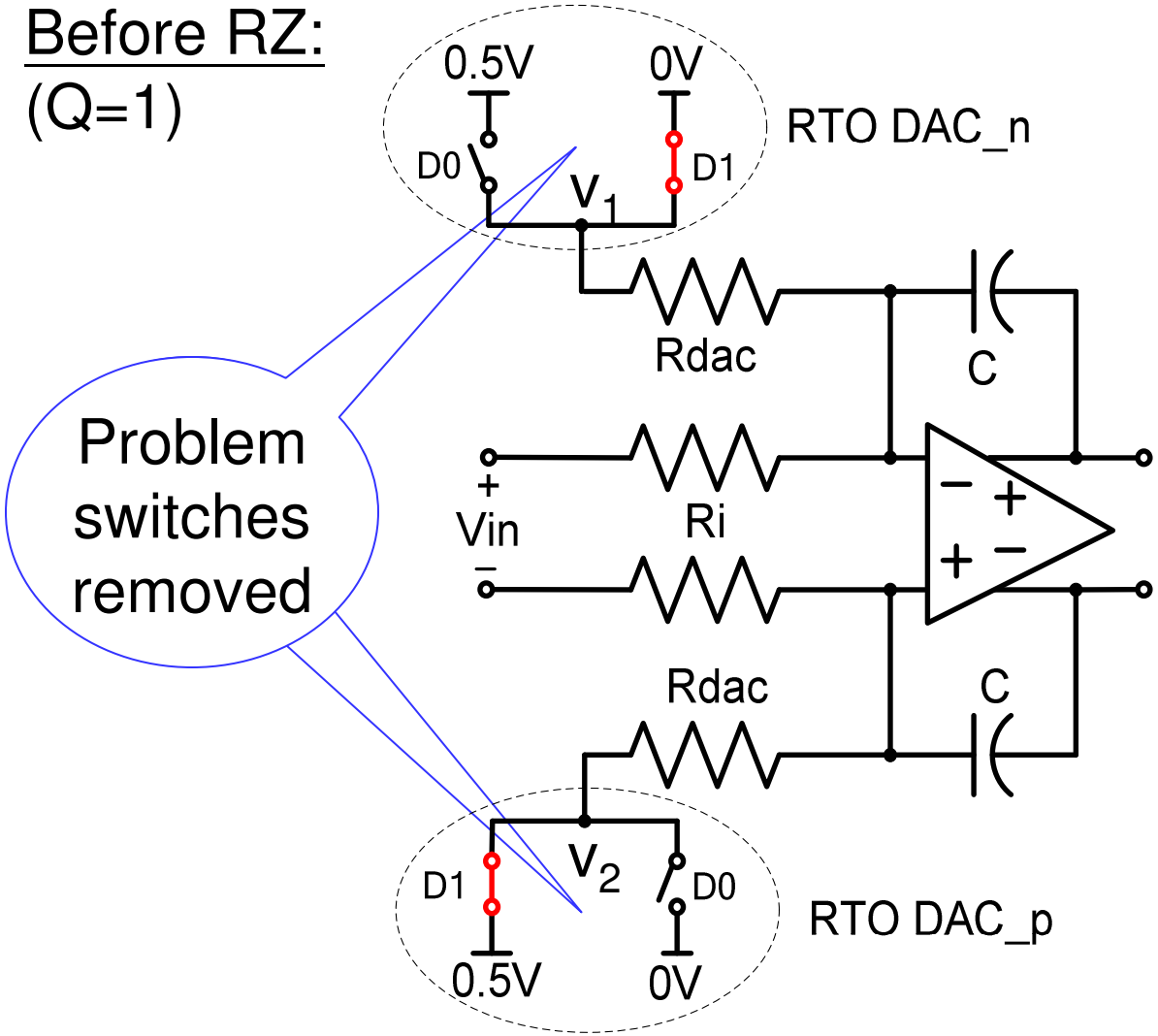
RZ Challenge: Switches at $V_{DD}/2$

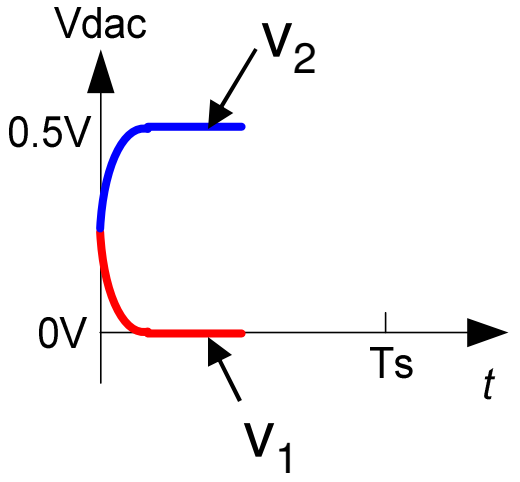


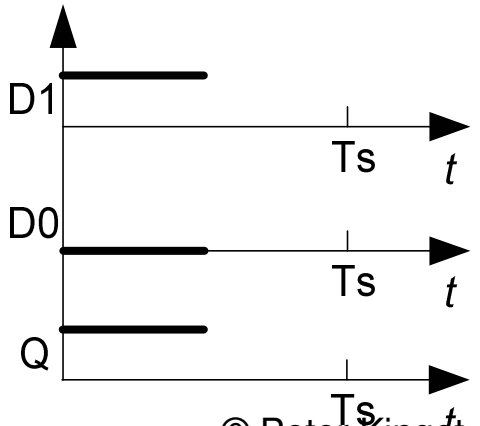


Solution: Return-to-open

Before RZ:
(Q=1)

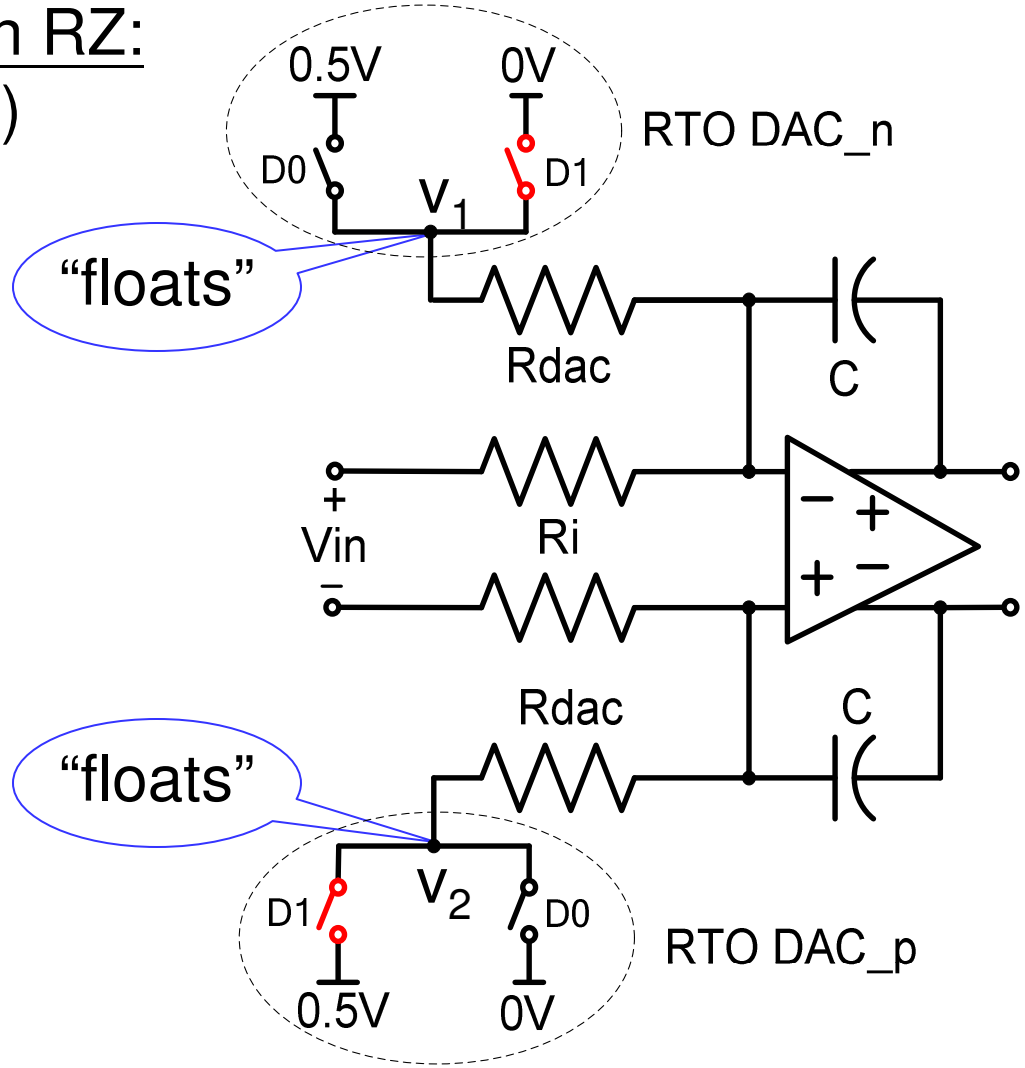


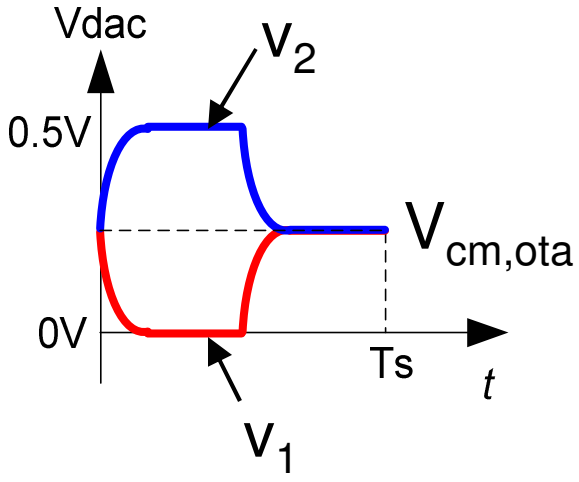


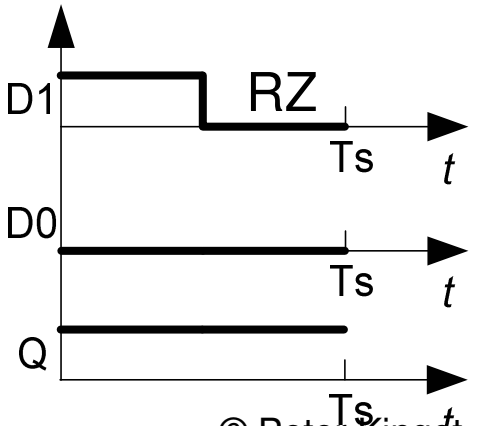


Solution: Return-to-open

When RZ:
(Q=1)

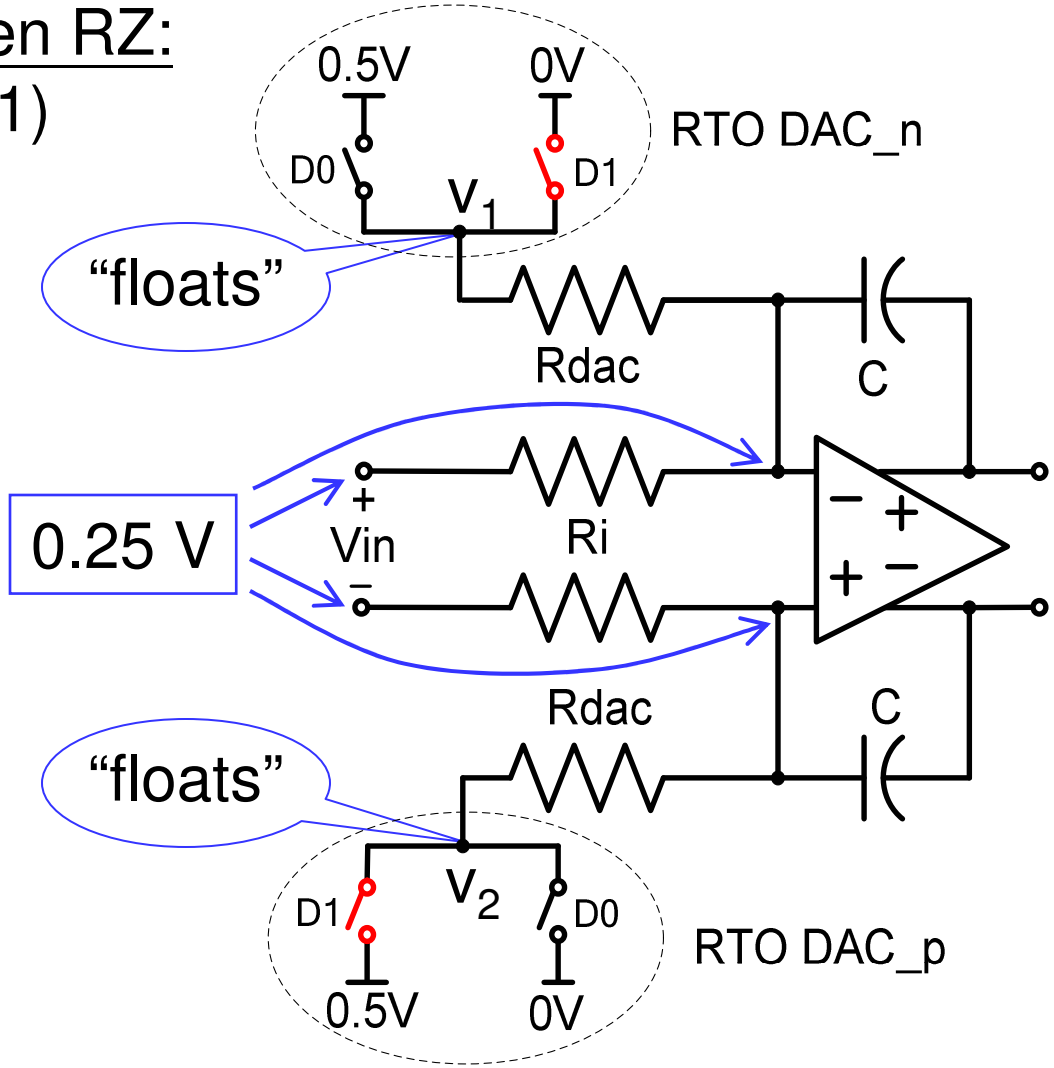


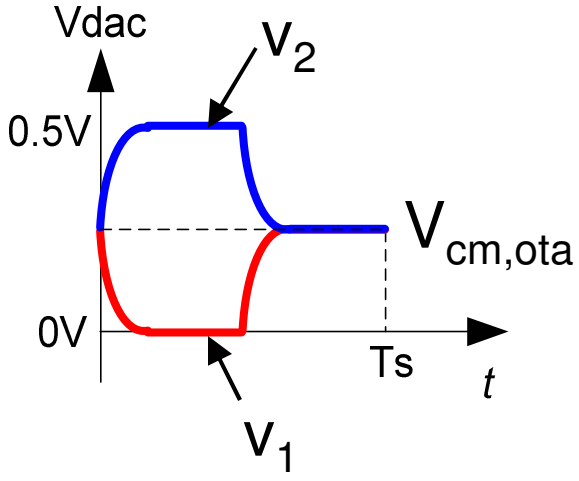


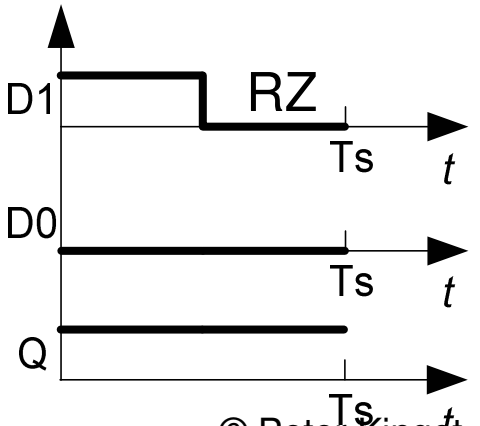


Solution: Return-to-open

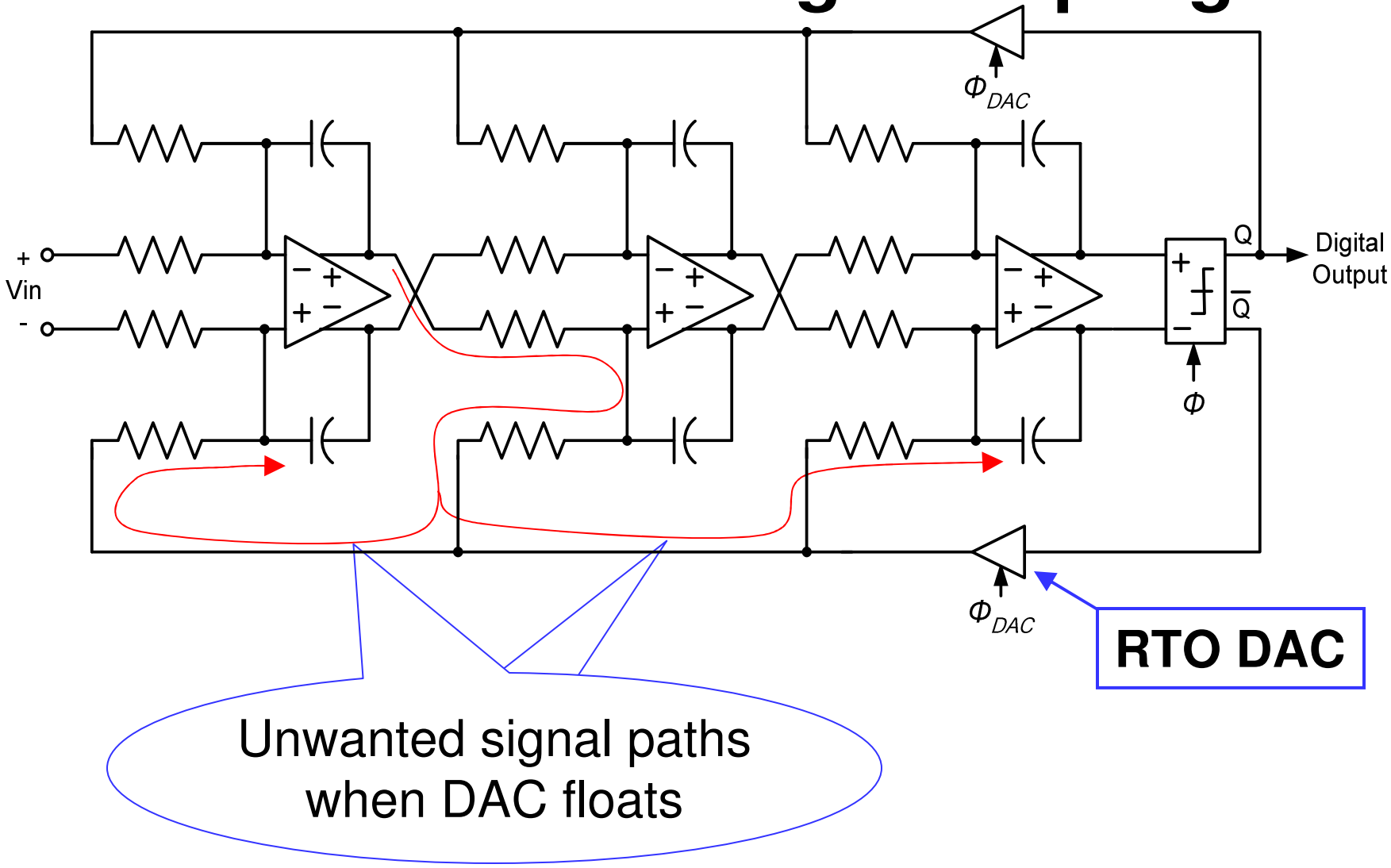
When RZ:
(Q=1)



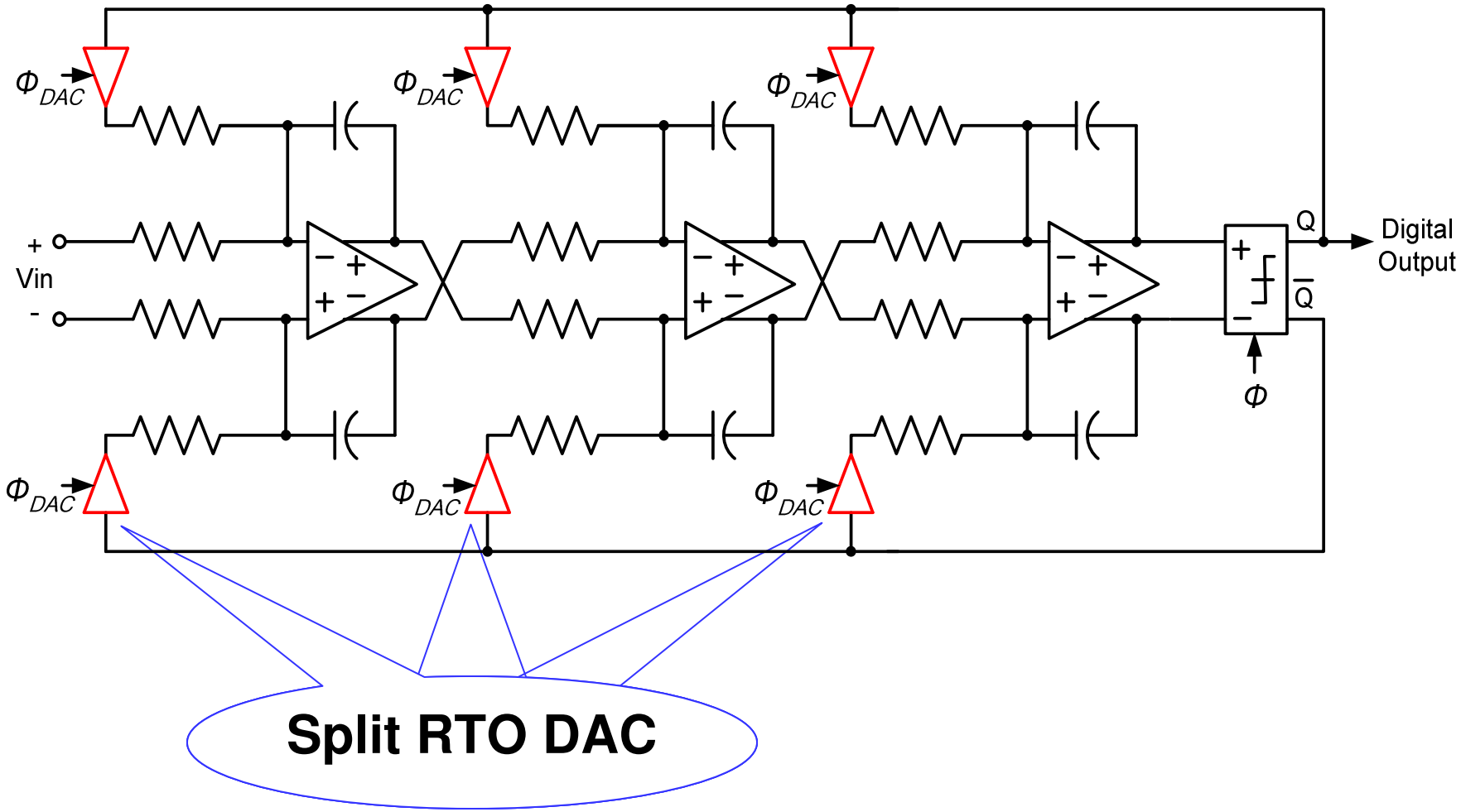




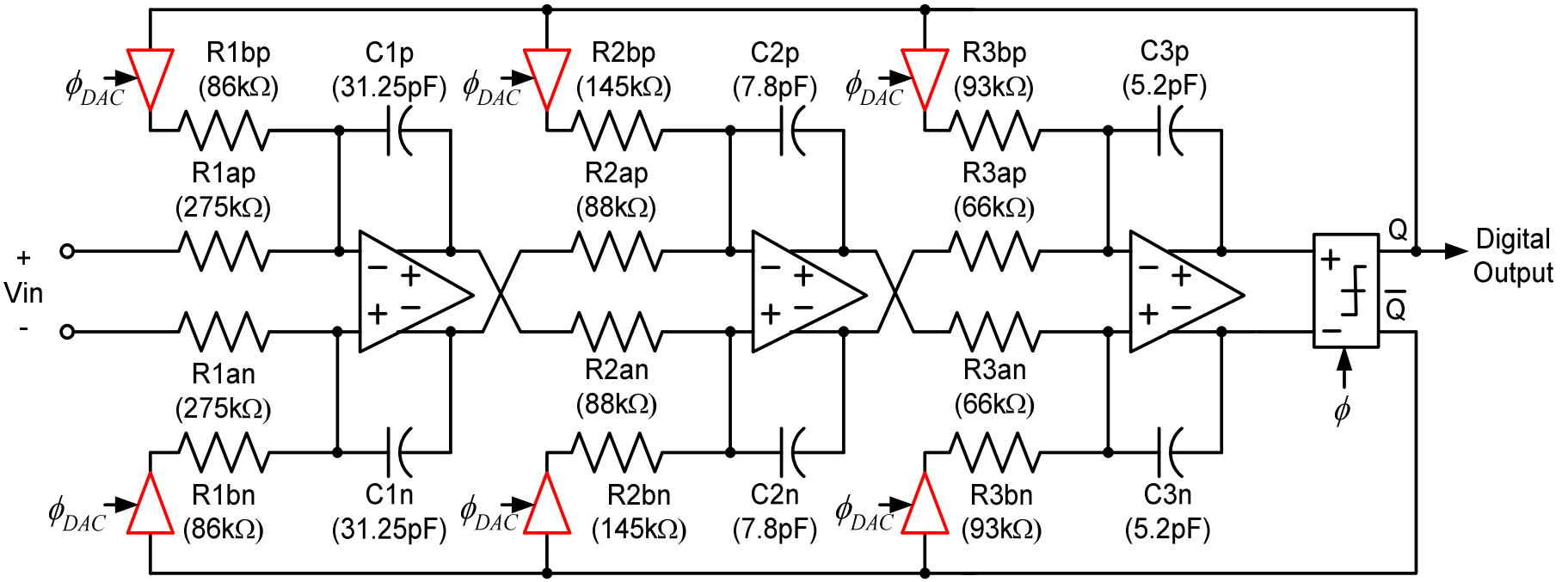
RTO SDM: Inter-stage Coupling

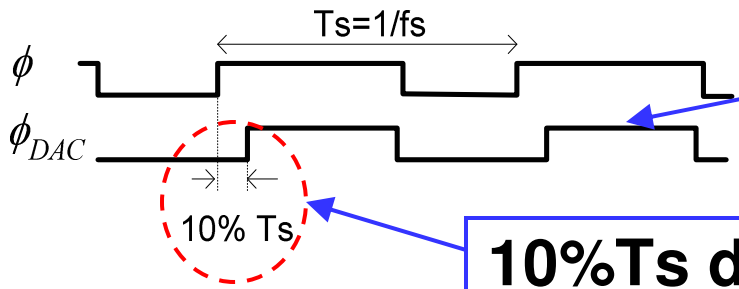


Split RTO SDM Architecture



Modulator Details





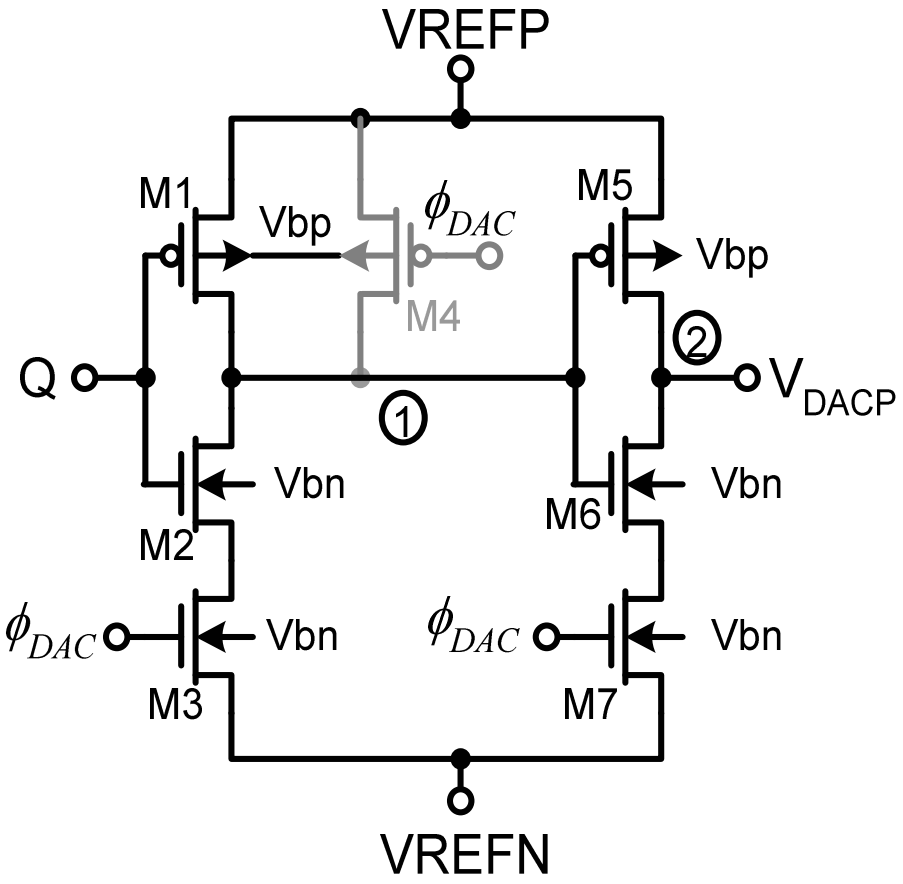
50% duty cycle

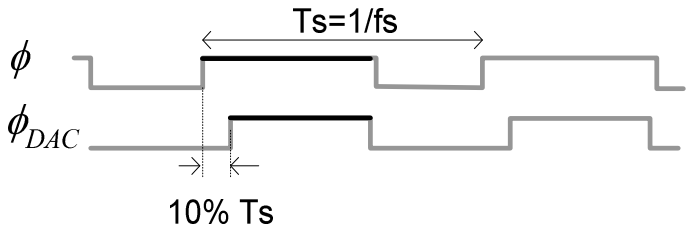
10%Ts delay: to allow the comparator outputs to fully settle before the DACs become active.

BW = 25kHz, fs = 3.2MHz,
Vin,max = 1Vppdiff.

RTO DAC Circuit

Φ_{DAC} High:

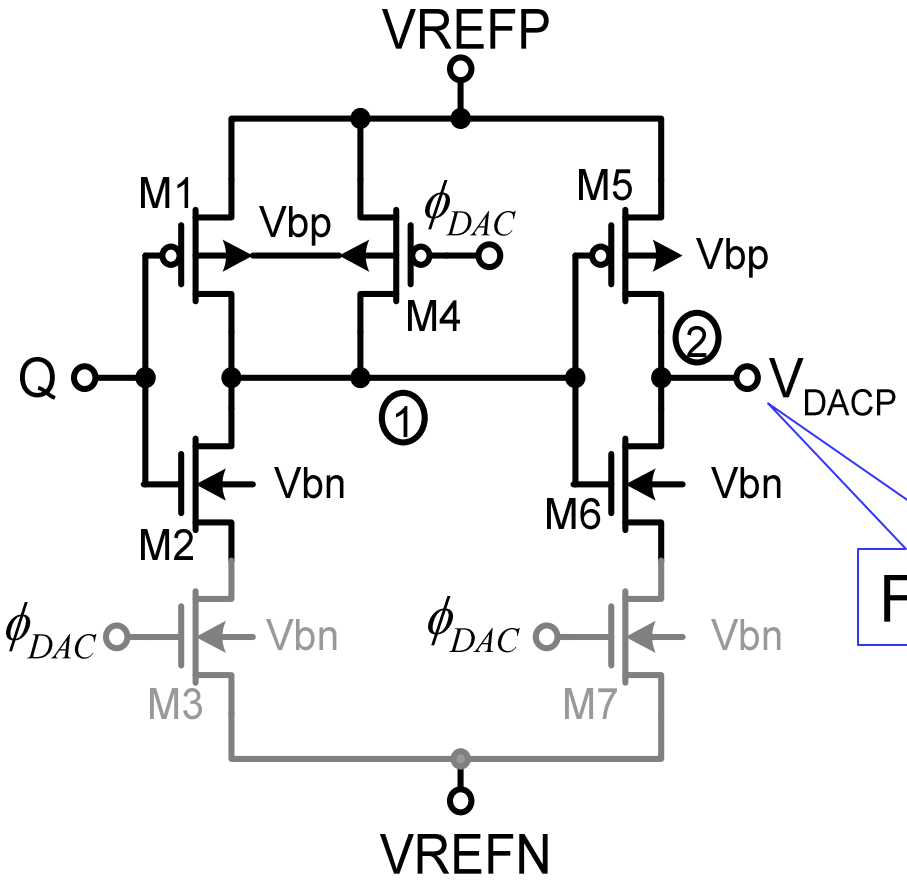




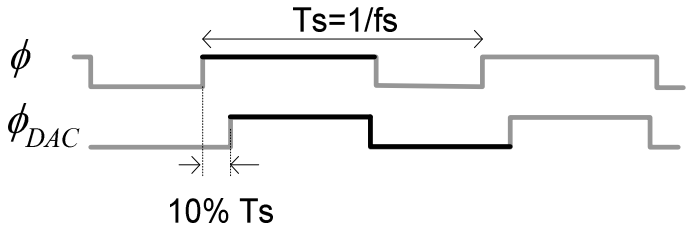
All the bodies tied to $V_{DD}/2$.

RTO DAC Circuit

Φ_{DAC} Low:



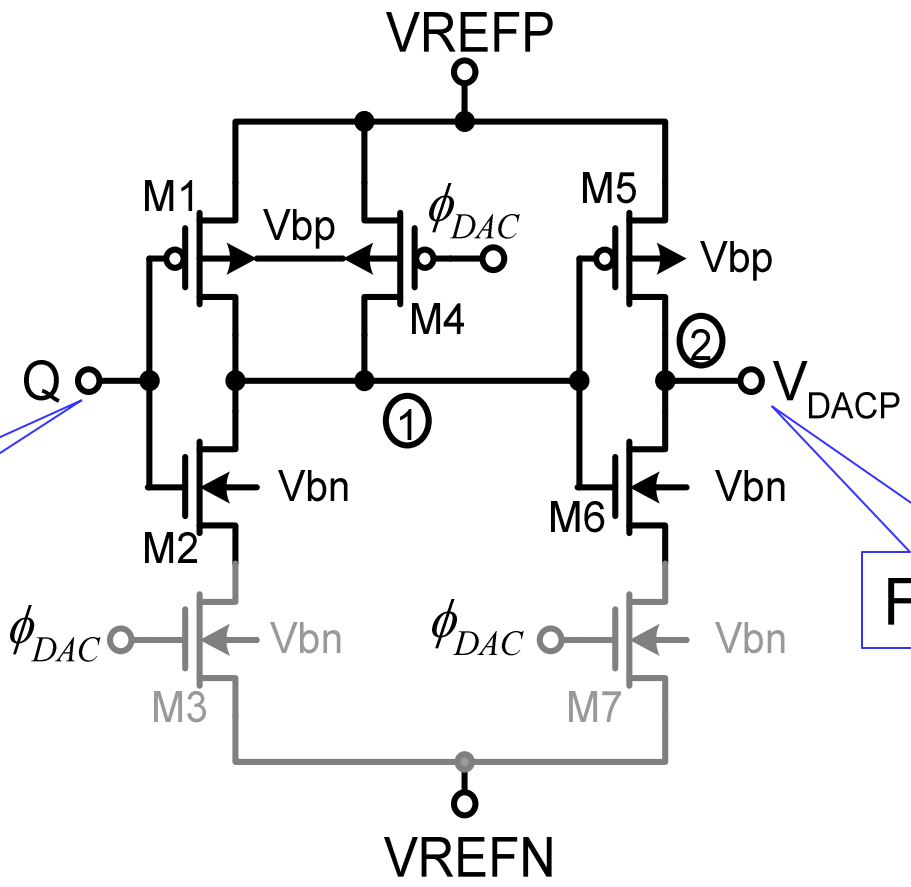
Floating.



All the bodies tied to $V_{DD}/2$.

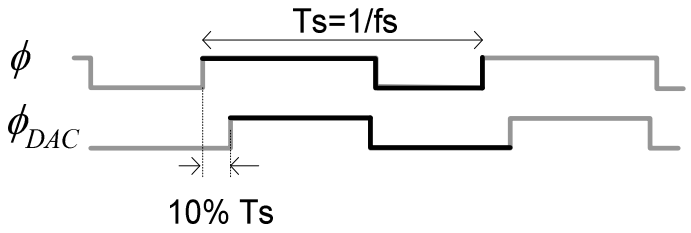
RTO DAC Circuit

Φ_{DAC} Low:



Q invalid for Φ low.

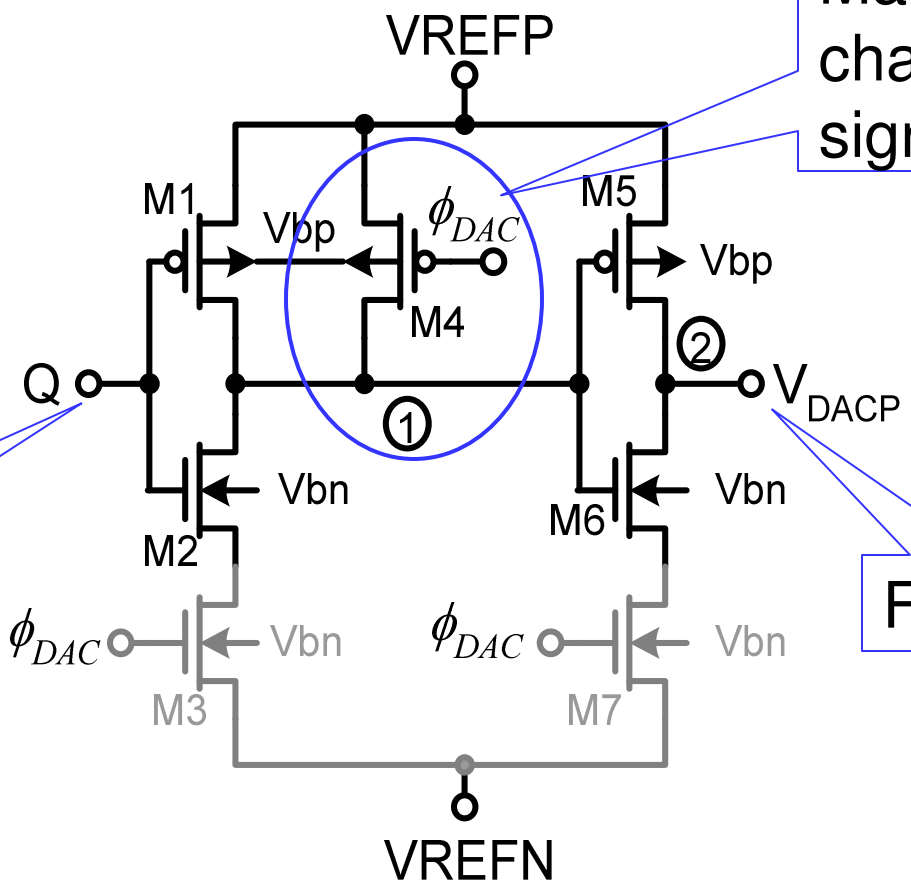
Floating.



All the bodies tied to $V_{DD}/2$.

RTO DAC Circuit

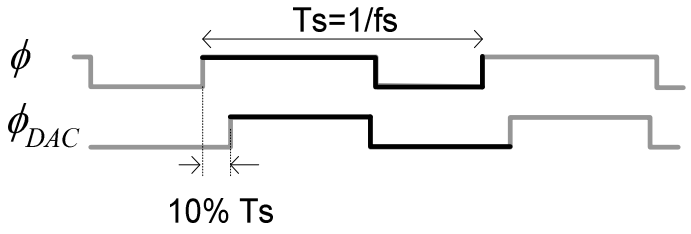
Φ_{DAC} Low:



Make charge-injection signal-independent.

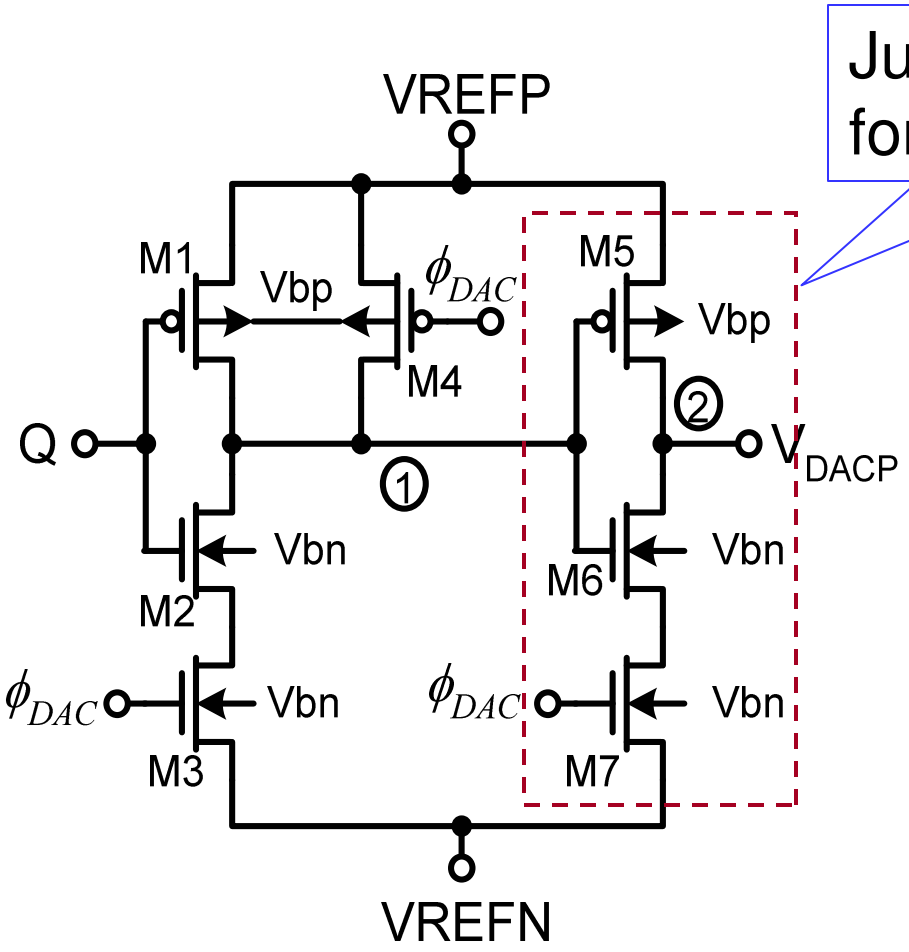
Q invalid for Φ low.

Floating.

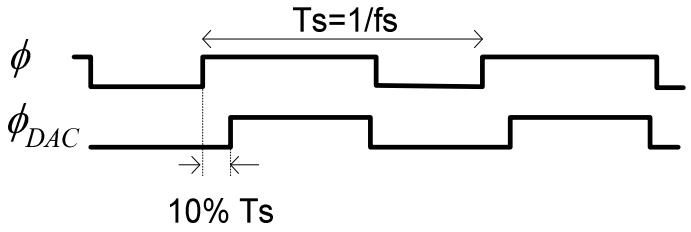


All the bodies tied to $V_{DD}/2$.

RTO DAC Circuit

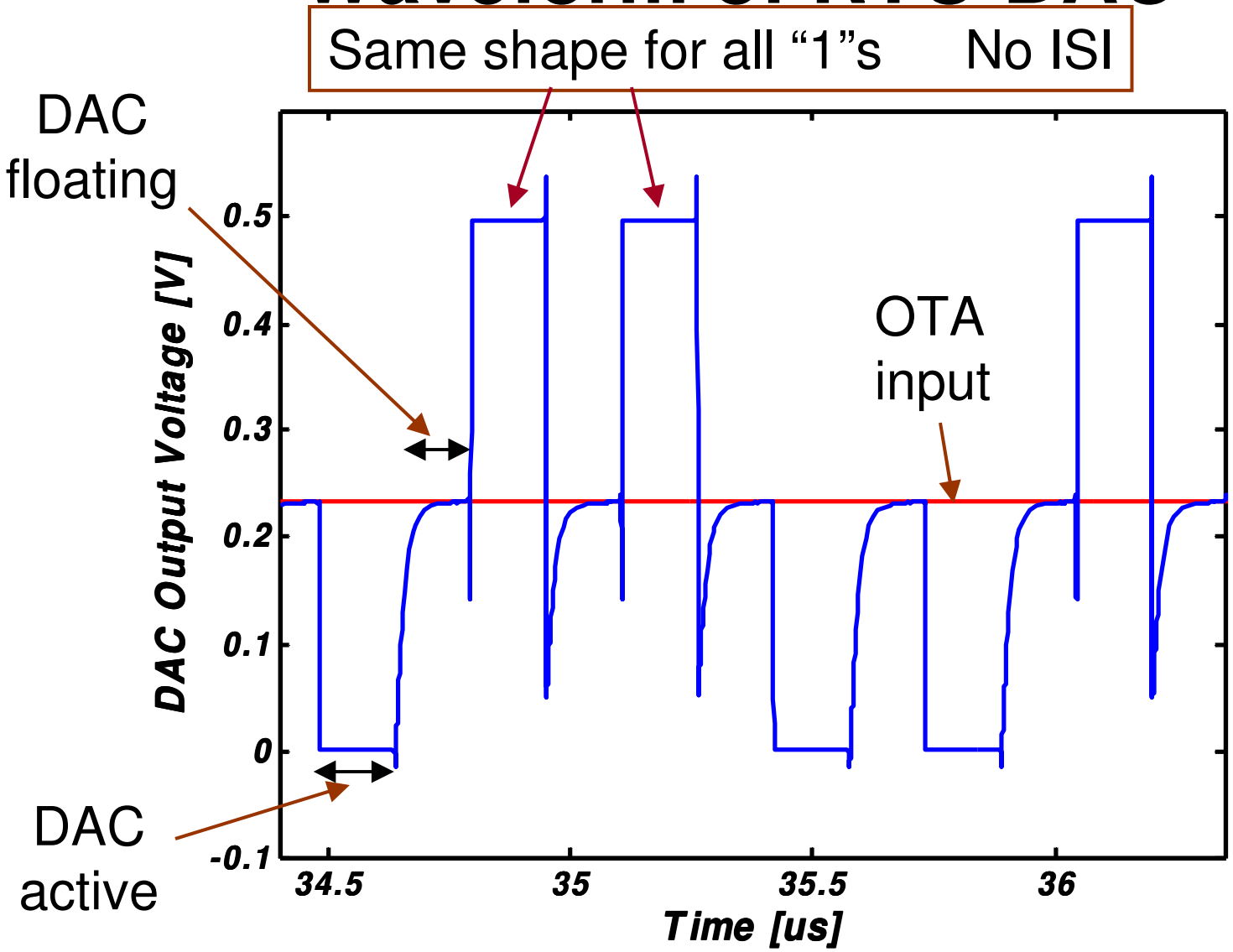


Just split M5-M7 for each FB path.



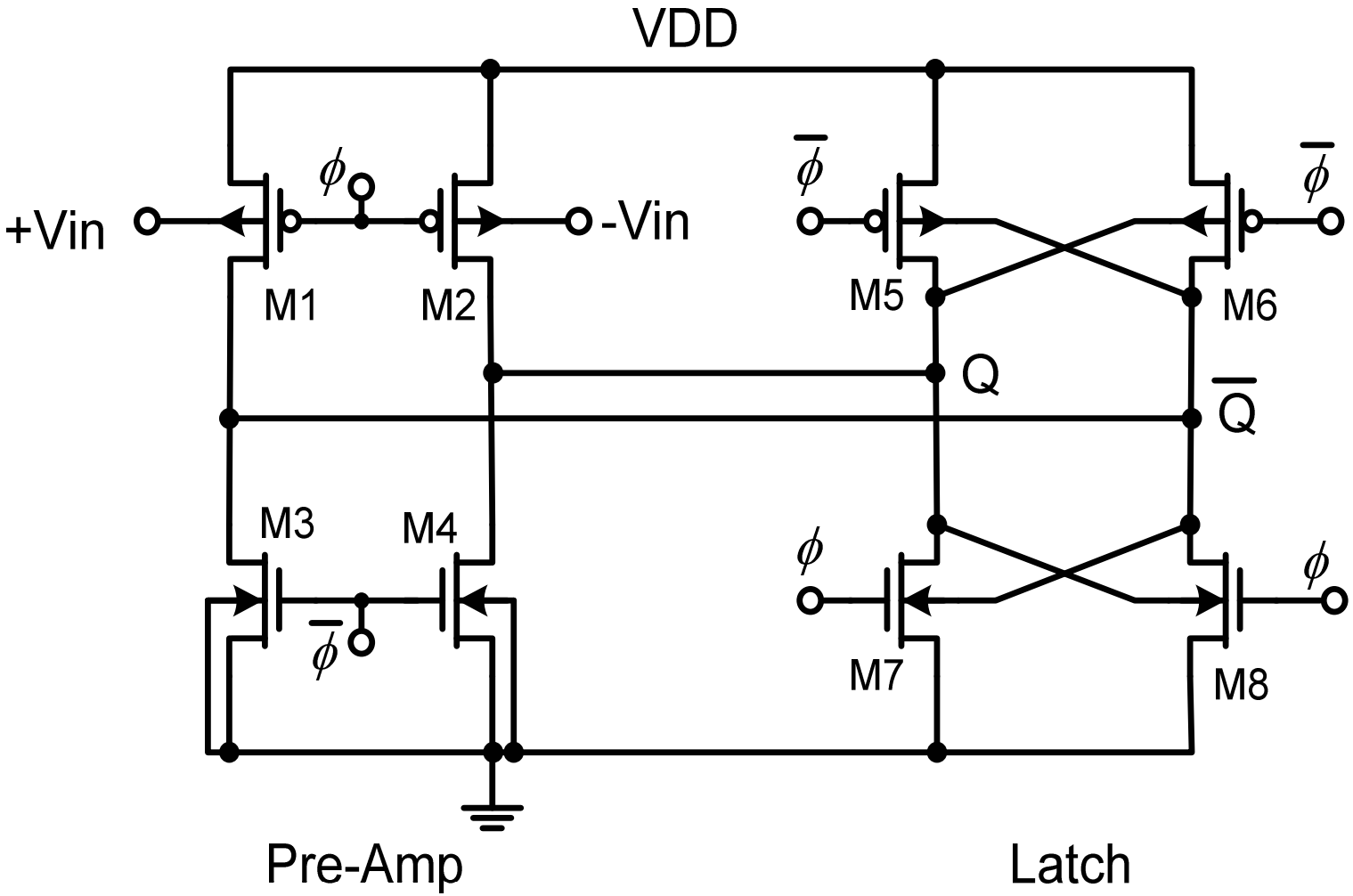
All the bodies tied to $V_{DD}/2$.

Waveform of RTO DAC

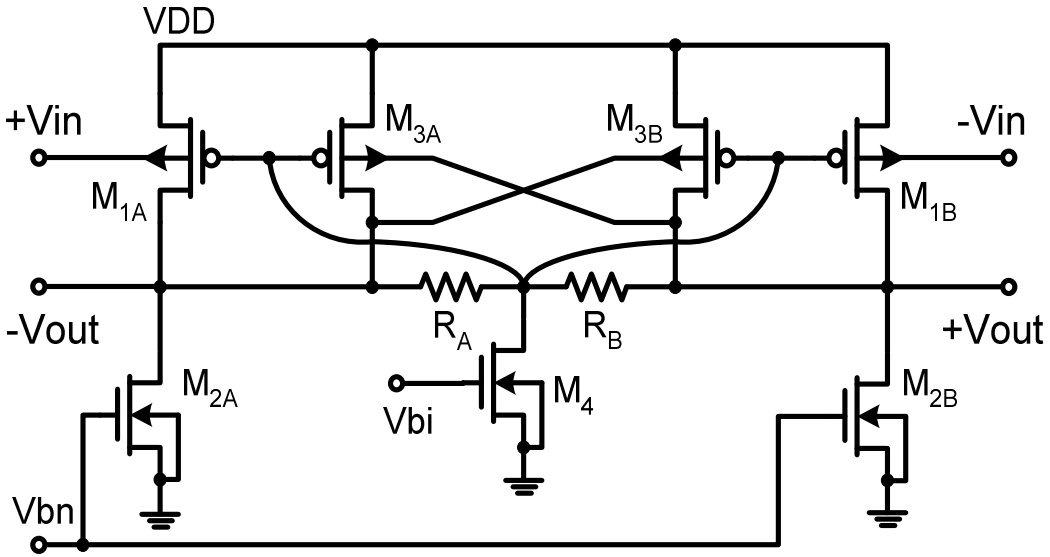


Simulated output waveform of 1st DAC

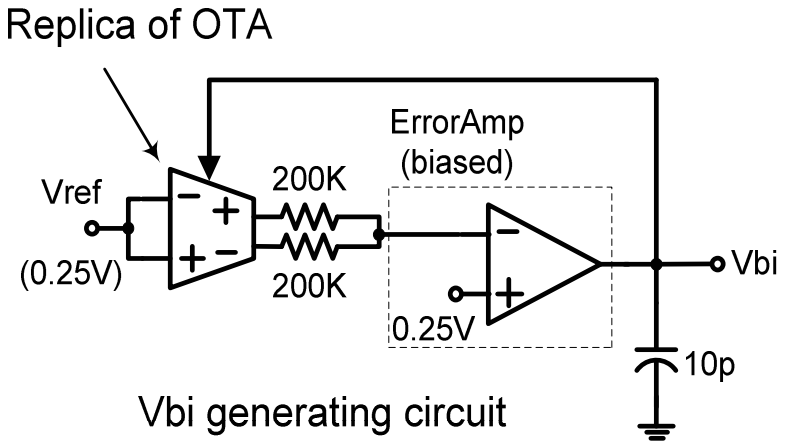
0.5V Body-input Gate-clocked Comparator



0.5V Fully Differential OTA



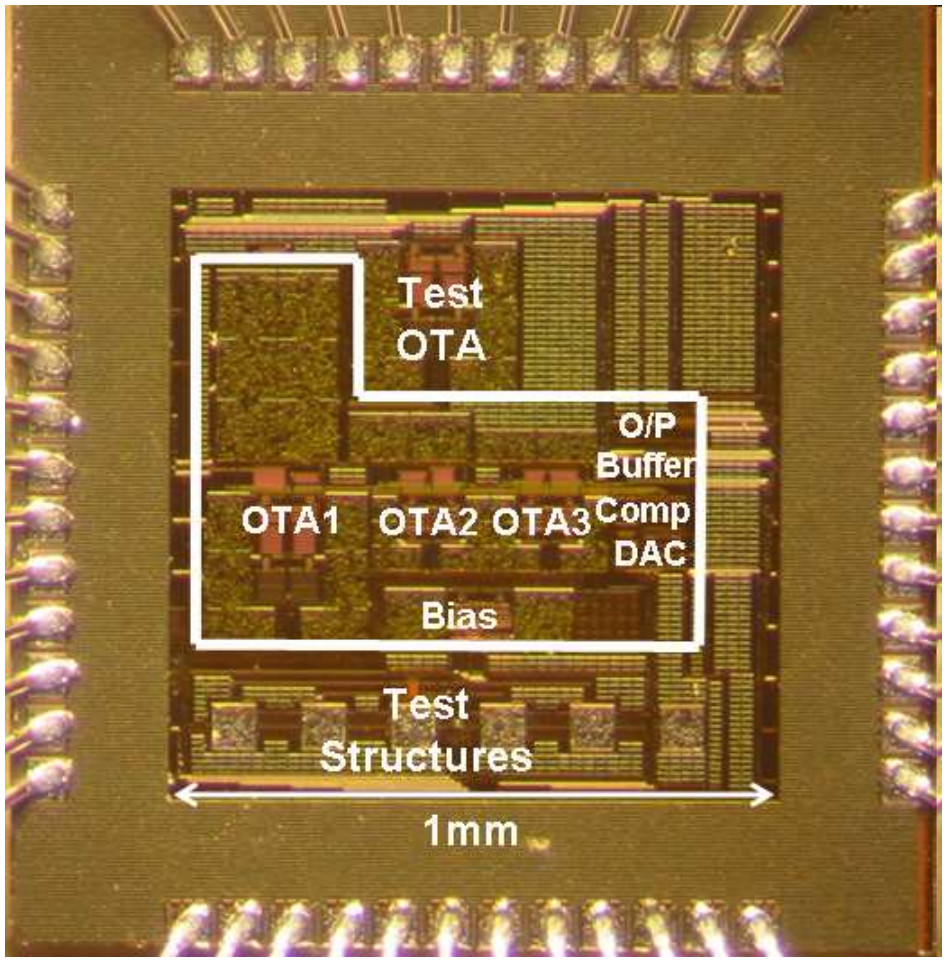
[Chatterjee ESSCIRC'05]



[Chatterjee ISSCC'05]

- Measurements on a replica of the 1st OTA:
  - A_{DC} = 46dB, UGB = 4MHz;
  - Input referred noise:
    $33nV_{rms}$ @10kHz and $12nV_{rms}$ @1MHz.

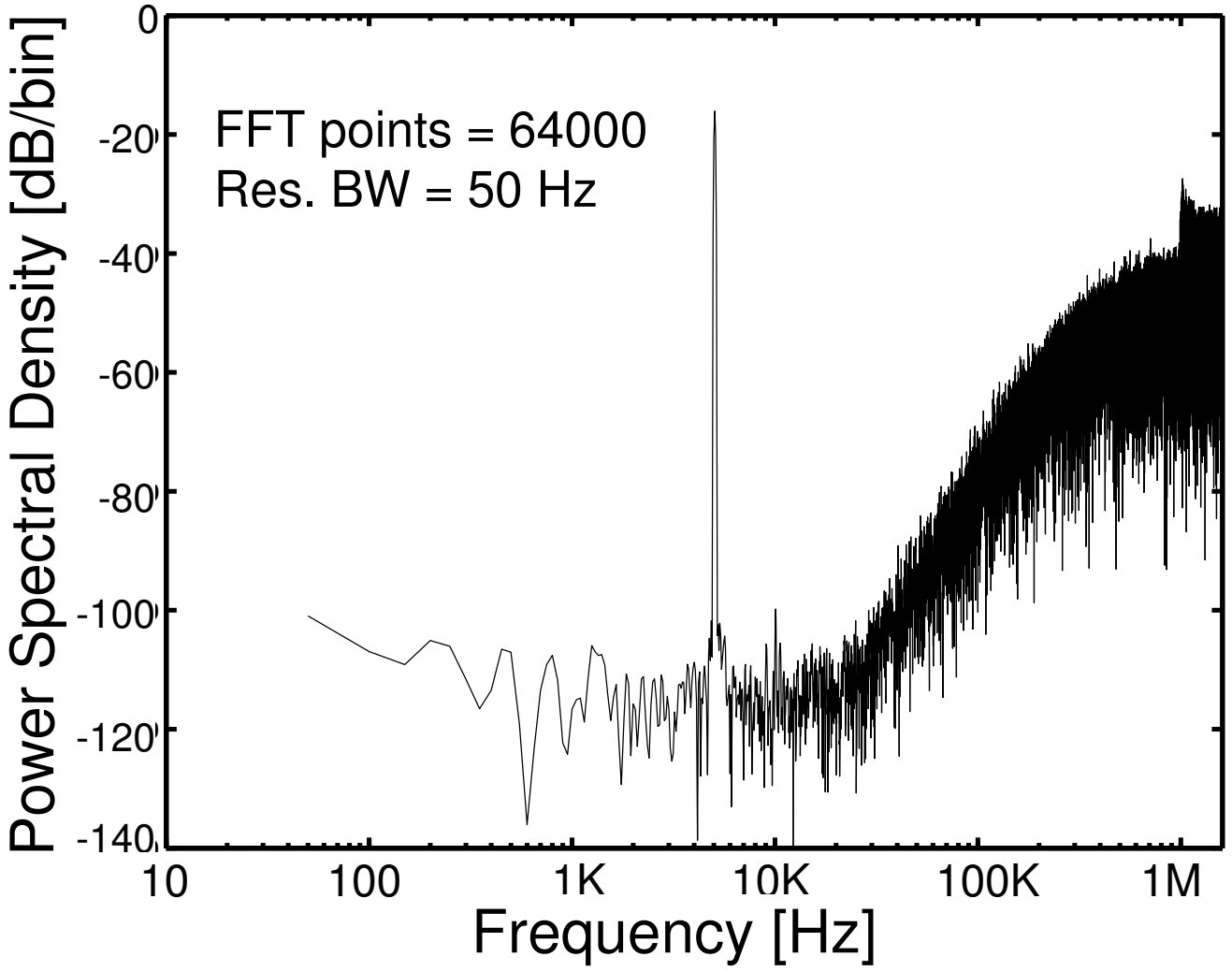
Die Photograph



- 0.18μm CMOS
- Standard V_T (0.5V)
- Triple-well devices
- 0.5V operation

K.P. Pun, S. Chatterjee, and P. Kinget, *"A 0.5 V 74dB SNDR 25kHz CT Delta-Sigma Modulator with Return-to-Open DAC"* in IEEE International Solid-State Circuits Conference (ISSCC), pp. 72-73, February 2006.

Measured Output Spectrum

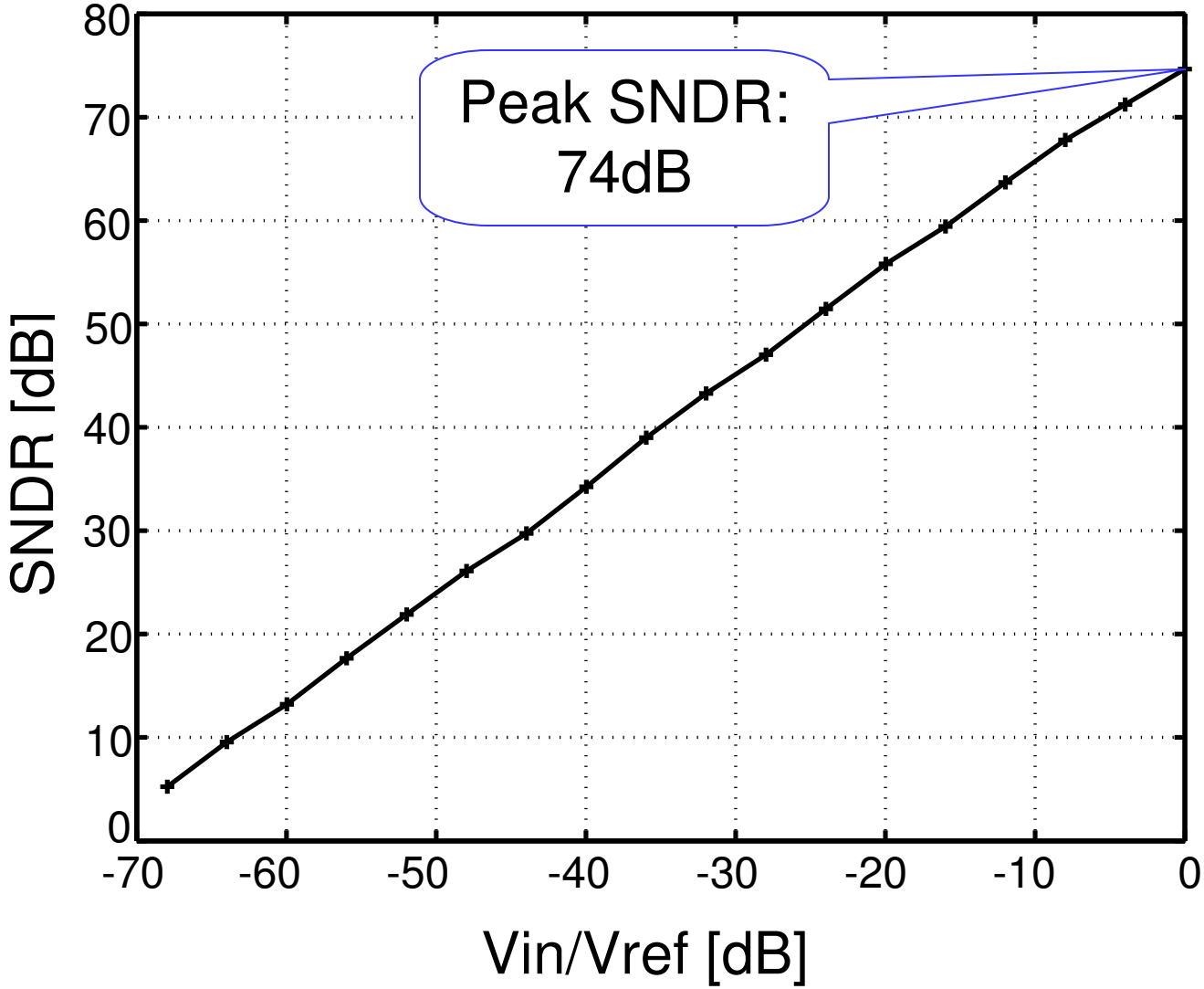


2^{nd} harmonic < 83dBc

3^{rd} harmonic < 88dBc

@Vin = -4dB Vref, fin = 5kHz
(Vref =1Vppdiff.)

Measured SNDR versus Vin

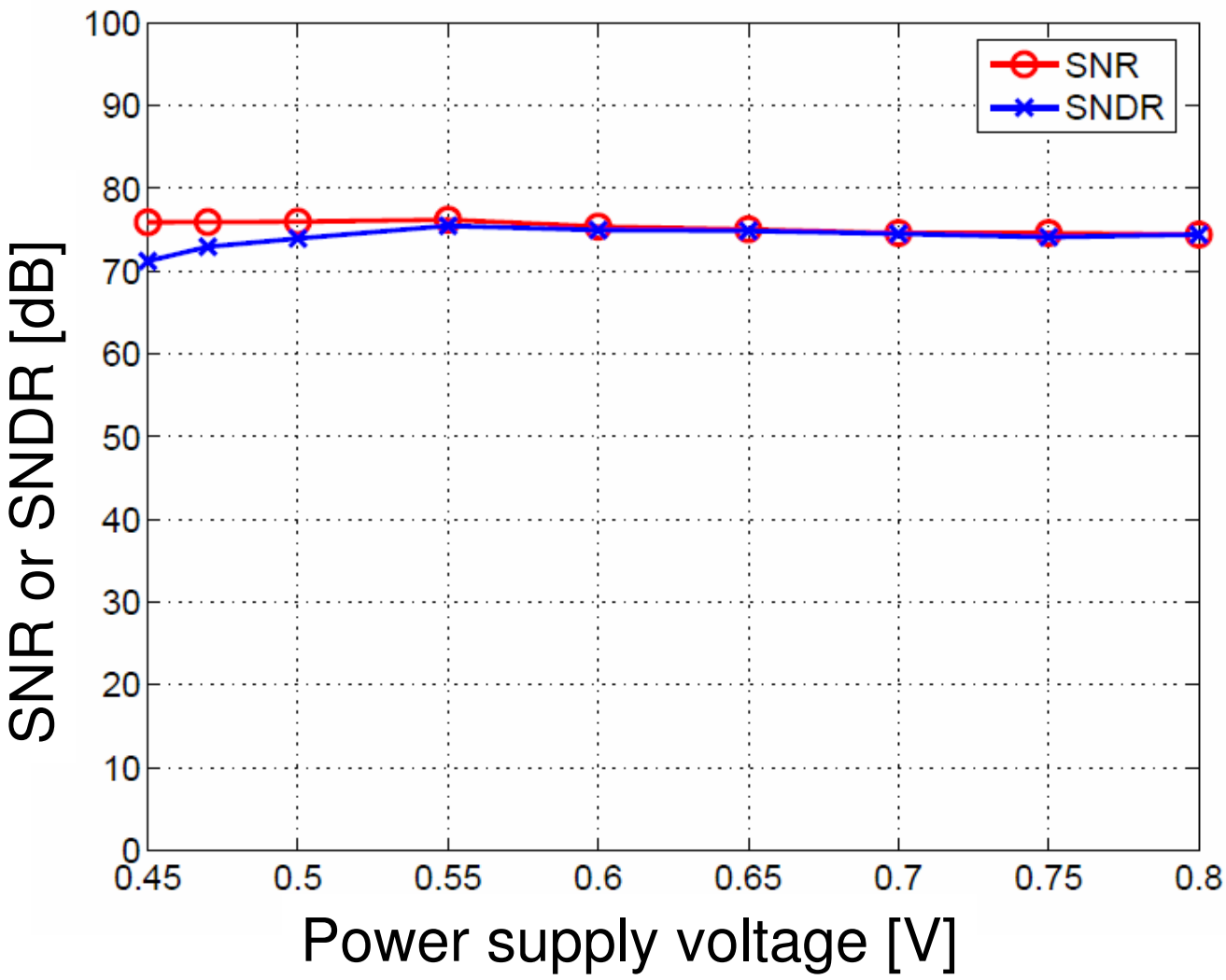


(Vref = 1Vppdiff.)

Performance Summary at 25°C

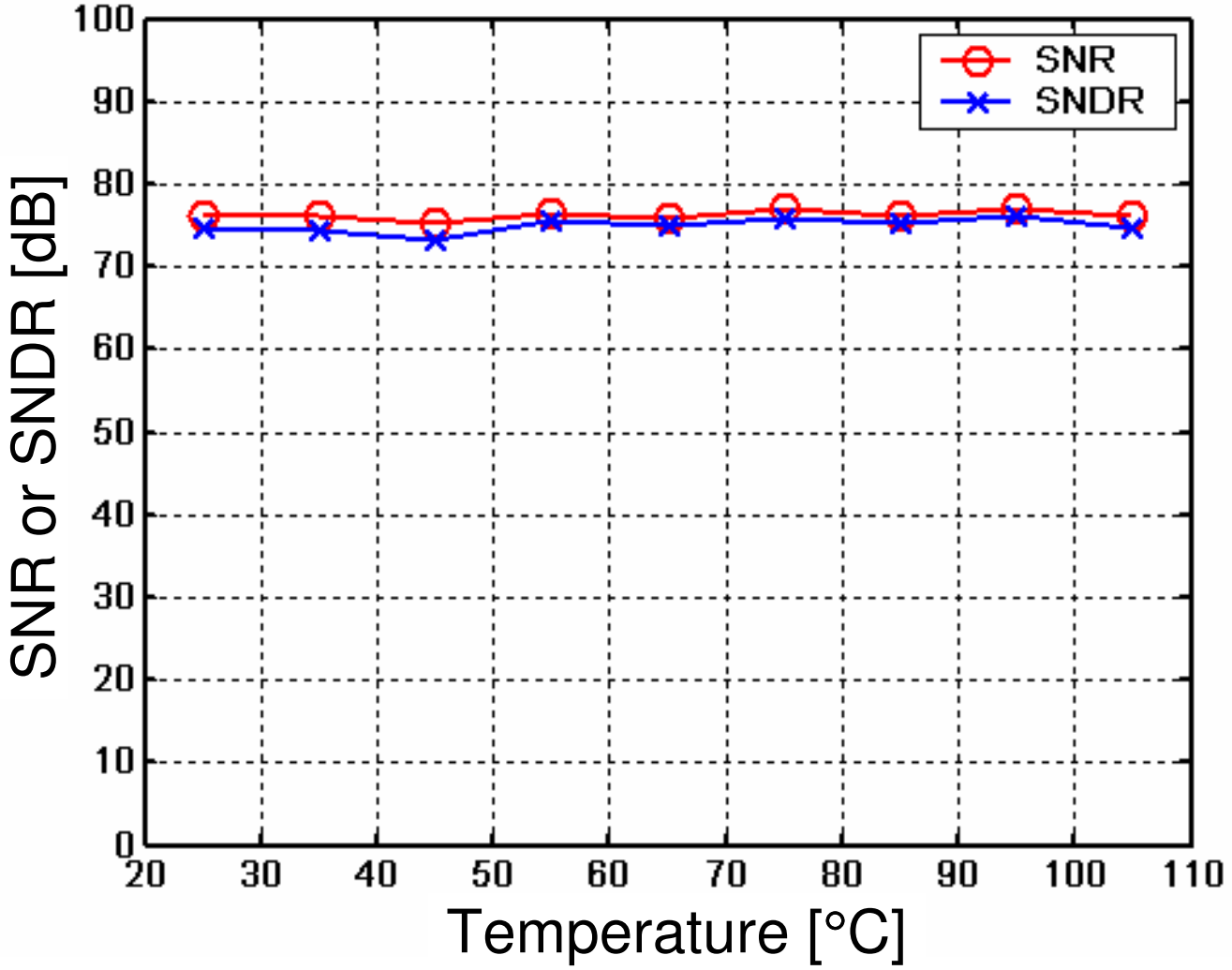
Modulator type	1-bit, 3rd order, continuous-time		
Signal bandwidth	25 kHz		
Sampling frequency / OSR	3.2 MHz / 64		
Input range	1 Vppdiff.		
Supply Voltage	0.45V	**0.5V**	0.8V
SNDR @ Vin = 1Vppdiff.	71 dB	**74 dB**	74 dB
SNR @ Vin = 1Vppdiff.	76 dB	**76 dB**	74 dB
Power consumption (total) Sigma Delta Modulator (filter + comparator + DAC) Output buffers		**370 μW** **300 μW** **70 μW**	
Active die area	0.6 mm^2		
Technology	0.18 μm CMOS (standard V_T, triple-well, MIM, and HiRes Poly)		

SNDR versus V_{DD}



@25°C and Vin = 1Vppdiff.

SNDR versus Temperature



@V_{DD} = 0.5V and Vin = 1Vppdiff.

Performance Comparison

	VDD [V]	Type	SNDR [dB]	Bandwidth [kHz]	Power [uW]	Area [mm^2]	CMOS [um]		FOM [10^9/J]
Grech 1999	1	SO	56*	3.9	1500	0.9**	0.8		1.3
Keskin 2001	1	RO	78	20	5600	0.41	0.35		23
Matuya 1994	**1**	**CT**	**51**	**192**	**1560**	**2.53**	**0.5**	**Low VT**	**36**
Dessouky 2000	1	SC	85	25	950	0.63	0.35	Gate boost	381
Yao 2004	1	SC	81	20	140	0.18	0.09		1310
Ueno 2004	**0.9**	**CT**	**50.9**	**1920**	**1500**	**0.12**	**0.13**		**366**
Peluso 1998	0.9	SO	62	16	40	0.85	0.5		410
Sauerbrey 2002	0.7	SO	67	8	80	0.082	0.18		58
Ahn 2005	0.6	SRC	77	24	1000	2.88	0.35	Low VT	138
This work	**0.5**	**CT**	**74**	**25**	**300**	**0.6**	**0.18**		**340**

*=SNR only; ** Estimated from die photograph;
SO = Switched Opamp; CT = Continuous Time;
SC = Switched Capacitor; RO = Reset Opamp;
SRC=Switched-RC

$$FOM = \text{resolution} \times \frac{BW}{P}$$

Analog design techniques at 0.5 V

- How to do CM rejection?
  - Use local CM feedback & rejection
  - Use CM feedforward cancellation
  - Separate CM signal rejection and CM DC biasing
- How to increase DC gain?
  - Use negative load conductance
- How to use strong inversion operation?
  - Forward Body Bias to reduce V_T

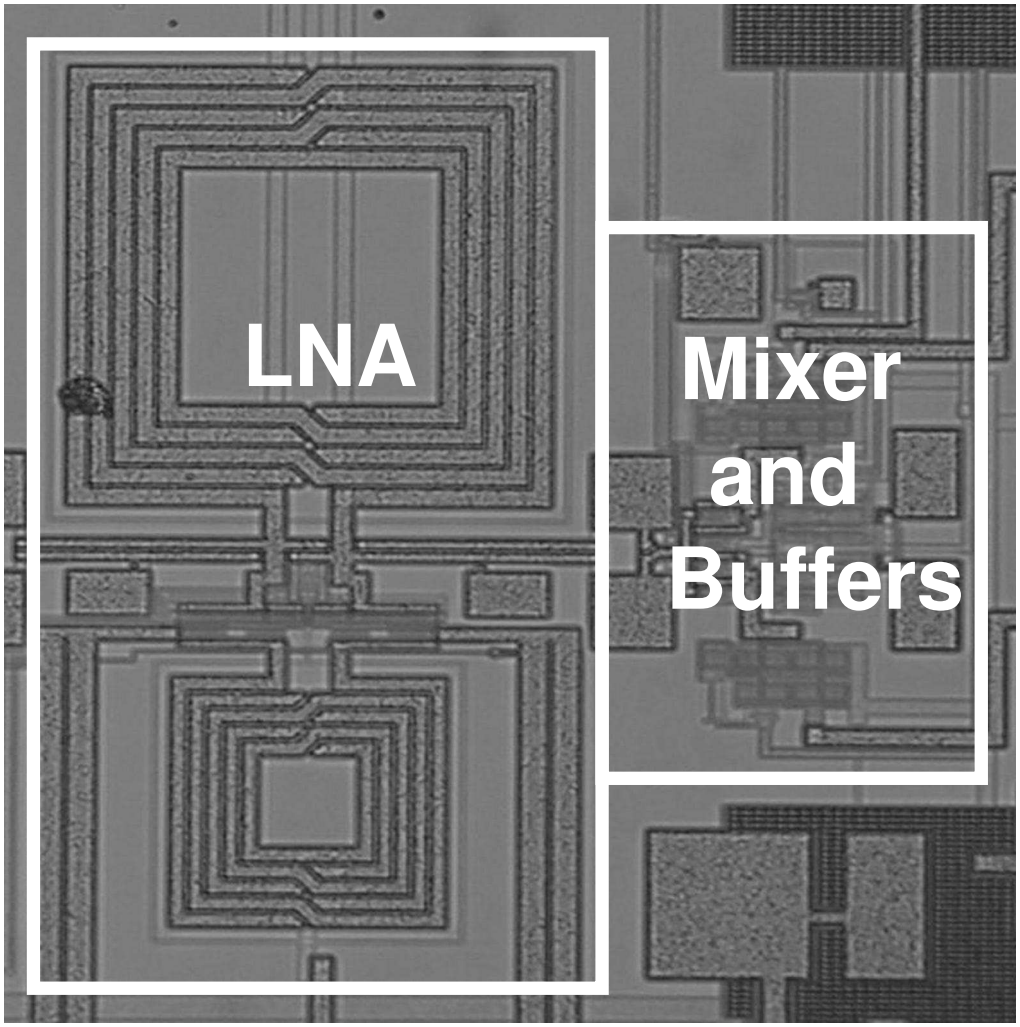
Extensive use of the body terminal

Extensive use of on-chip tuning & biasing

Architectural changes to eliminate signal path switches

Looking ahead

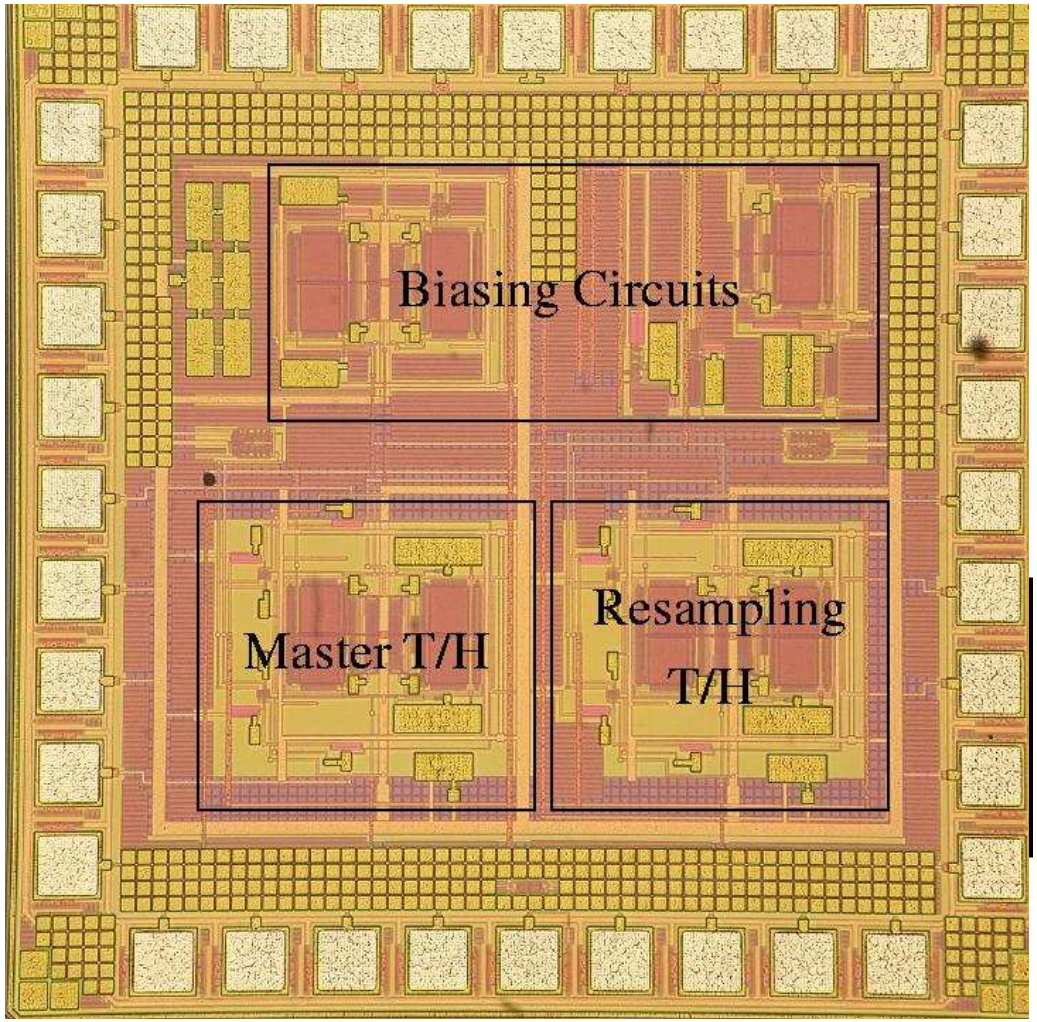
0.5V 900MHz RF Front-end



- 0.18 µm CMOS
- Low-V_T devices
- LNA/MIXER
  - NF 8.8 dB
  - Gain 11.5 or-7 dB
  - ICP -23 dBm
  - 5 mW
    (w/ LO Buffers)

N. Stanic, P. Kinget, and Y. Tsividis,*"A 0.5 V 900 MHz CMOS Receiver Front End,"*
IEEE Symposium on VLSI circuits, June 2006.

0.5 V 1 Msps 60 dB SNDR Track&Hold

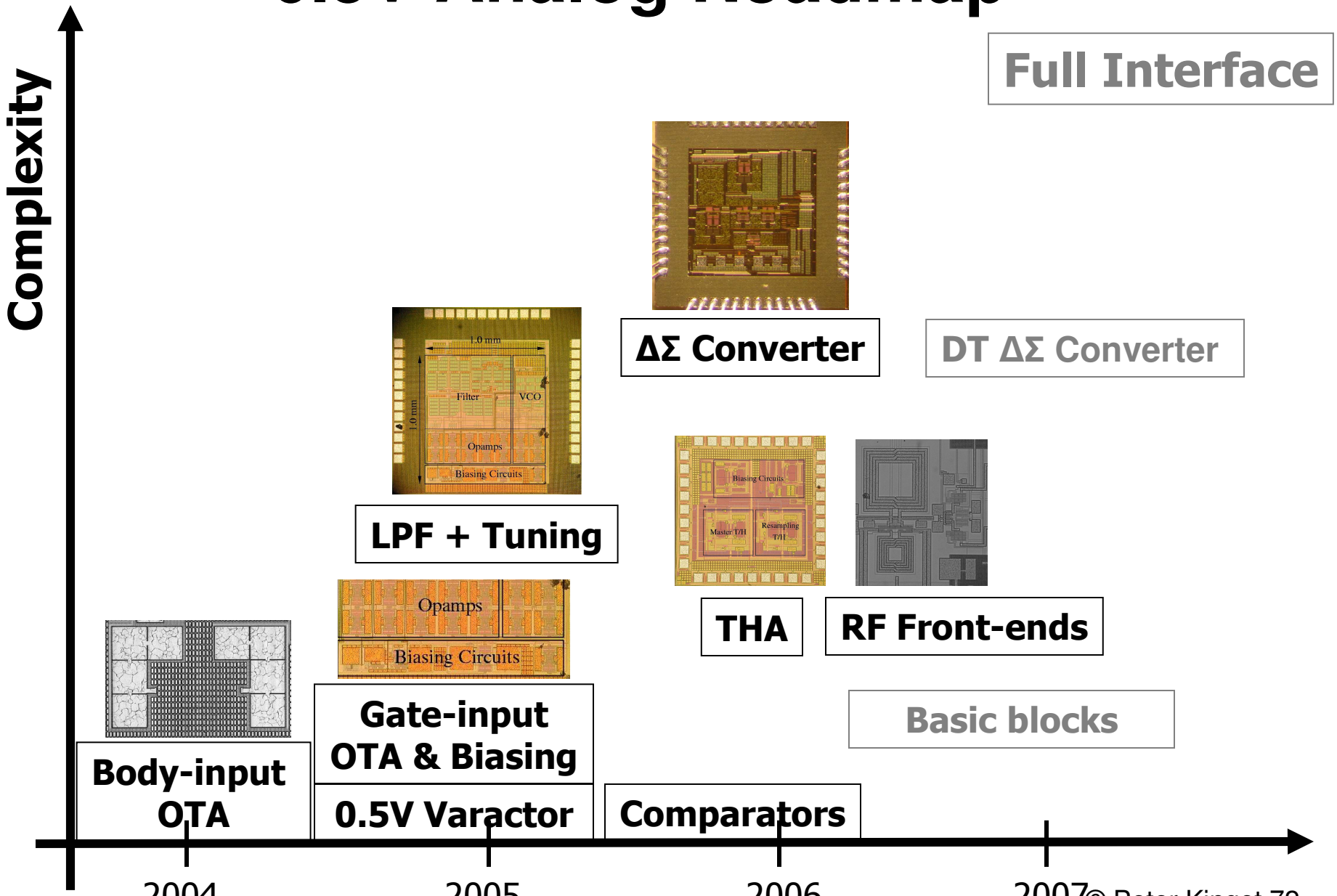


- 0.25 µm CMOS
- $|V_T|$=0.6V

- MIM caps
- High-res resistors
- Triple well nMOS

S. Chatterjee, and P. Kinget, *"A 0.5-V 1-Msample/s 60-dB SNDR Track-and-Hold Circuit,"* IEEE Symposium on VLSI circuits, June 2006

0.5V Analog Roadmap



Other Challenges in nanometer CMOS

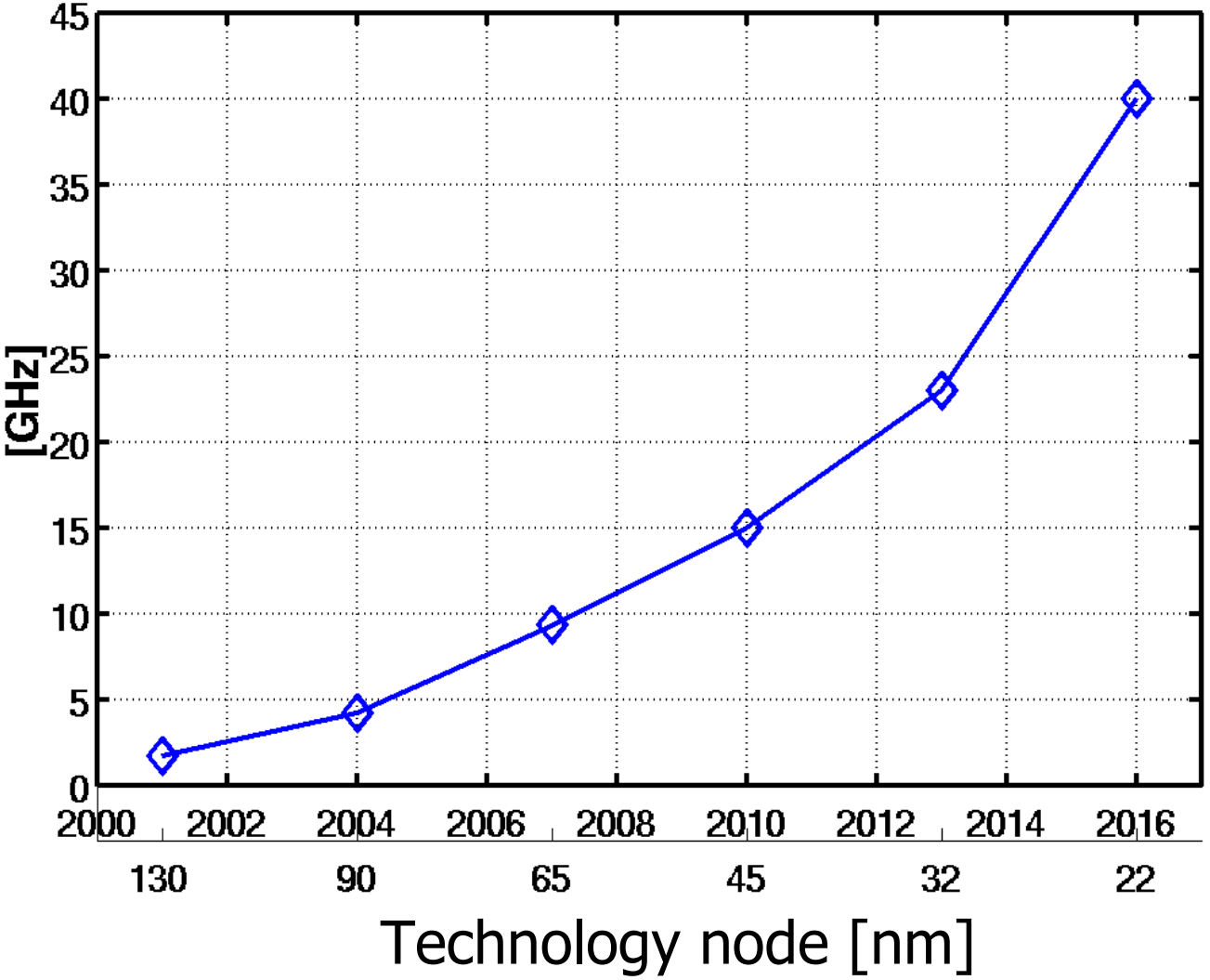
- Gate leakage.
- Sub-threshold leakage.
- Reduced body-effect [VonAmin05]:

$$V_T \uparrow \;\&\; t_{ox} \uparrow \qquad g_{mb} \downarrow$$

Other Opportunities in nanometer CMOS

- Many V_T choices !
- Novel devices.
- *Extensive* Digital Calibration & Correction.

CMOS Trends: On chip Clock Speed



[ITRS'04]

Acknowledgments

- Analog Devices, Intel and Realtek for supporting parts of this work.
- Europractice and Philips Semiconductors for 0.18um and 0.25um prototypes fabrication.

More details

- [Cha 05] S. Chatterjee, Y. Tsividis, and P. Kinget, ***"A 0.5 V filter with PLL-based tuning in 0.18 um CMOS technology,"*** in **IEEE International Solid-State Circuits Conference (ISSCC),** pp. 506-507, February 2005.
- [Cha 04] S. Chatterjee, Y. Tsividis, and P. Kinget, ***"A 0.5 V bulk input fully differential operational transconductance amplifier,"*** in **European Solid-State Circuits Conference (ESSCIRC),** pp.147-150, Sep. 2004.
- [Cha 05] S. Chatterjee, Y. Tsividis and P. Kinget, ***"0.5 V Analog Circuit Techniques and Their Application in OTA and Filter Design,"*** **IEEE Journal of Solid-State Circuits (JSSC),** vol. 40, no 12, pp. 2373 - 2387, December 2005.
- [Pun 06] K.P. Pun, S. Chatterjee, and P. Kinget, ***"A 0.5 V 74dB SNDR 25kHz CT Delta-Sigma Modulator with Return-to-Open DAC"*** in **IEEE International Solid-State Circuits Conference (ISSCC),** pp. 72-73, February 2006.
- [Abd 06] M. Abdulai and P. Kinget, ***"A 0.5 V Fully Differential Gate-input Operational Transconductance Amplifier with Intrinsic Common-Mode Rejection"*** in **IEEE International Symposium on Circuits and Systems,** May 2006.
- [Cha 06] S. Chatterjee, and P. Kinget, ***"A 0.5-V 1-Msample/s 60-dB SNDR Track-and-Hold Circuit,"*** **IEEE Symposium on VLSI circuits**, June 2006.
- [Sta 06] N. Stanic, P. Kinget, and Y. Tsividis***,"A 0.5 V 900 MHz CMOS Receiver Front End,"*** **IEEE Symposium on VLSI circuits,** June 2006.

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- [Leh 01] T. Lehmann and M. Cassia, *"1-V power supply CMOS cascode amplifier,"* **IEEE J. Solid-State Circuits,** vol. 36, pp. 1082--1086, July 2001.
- [Sto 02] T. Stockstad and H. Yoshizawa, *"A 0.9-V 0.5-µA rail-to-rail CMOS operational amplifier,"* **IEEE J. Solid-State Circuits**, vol. 37, no. 3, pp. 286--292, 2002.
- [Fer 96] G. Ferri and W. Sansen, *"A 1.3V opamp in standard 0.7µm CMOS with constant gm and rail-to-rail input and output stages,"* **IEEE International Solid State Circuits Conference**, pp. 382--383, 478, 1996.

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