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KEYNOTE SPEECH

Implementing a Successful Business Model for the IC Industry in China

- Ping K. Ko, Silicon Federation Internation and Hong Kong university of Science & Technology

PLENARY TALKS

Novel Device Structures for Sub-25nm Generation

- Jason Woo, UCLA, USA

Ultra-Low Voltage Analog Design Techniques for Nanoscale CMOS Technologies

- Peter Kinget, Columbia University, USA

INVITED TALKS

Si and Non-Si Nanotechnologies for High-Performance and Low Power Computational Applications

- Robert Chau, Intel Corporation, USA

Technology Platform Based on Comprehensive Device Modeling for RFIC Design

- Yuhua Cheng, SiliconLinx Inc., USA

A Compact, Analytical Two-dimensional Threshold Voltage Model for Cylindrical, Fully-depleted Surrounding-Gate(SG) MOSFETs

- T. K. Chiang, Southern Taiwan University of Technology, Taiwan

Dimensional and Other New Effects in Advanced SOI Devices

- Sorin Cristoloveanu, LPCS - ENSERG, France

Nondestructive Depth Profiling of Gate Insulators by Angle-resolved Photoelectron Spectroscopy

- Takeo Hattori, Musashi Institute of Technology, Japan

A Complete Carrier-Based Non-Charge-Sheet Analytica Model for Nano-Scale Undoped Symmetric Double-Gate MOSFETs

- Jin He, Institute of Microelectronics, Peking University, China

Novel Localized-SOI MOSFET's Combining the Advantages of SOI and Bulk Substrates for Highly-Scaled Devices

- Ru Huang, Institute of Microelectronics, Peking University, China

ESD Protection Design for Mixed-Voltage I/O Interfaces -- Overview

- Ming-Dou Ker, Institute of Electronics, National Chiao-Tung University, Taiwan

Lanthanum Oxide for Gate Dielectric Insulator

- Kuniyuki Kakushima, Tokyo Institute of Technology, Japan

Gate-Misalignment-Effect Related Capacitance Behavior of a 100nm Double-Gate FD SOI NMOS Device with n+/p+ Poly Top/Bottom Gate

- J. B. Kuo, National Taiwan University

Low-Voltage Embedded RAMs in Nanometer Era

- Takayuki Kawahara, Hitachi Ltd, Japan

The Quest for Universal Semiconductor Memory

- Chung H. Lam, T.J. Watson Research Center, IBM, USA

A Compact Model for Reliability Simulation of Deep-Submicron MOS Devices and Circuits

- J. J. Liou, University of Central Florida, USA

Multi-disciplinary Requirements for Accurate Simulation of Power Conversion System Design

- Timwah Luk, Fairchild Semiconductor, USA

Subthreshold Behavior of Undoped DG MOSFETs

- A. Ortiz-Conde, Simón Bolívar University, Caracas, Venezuela

Nanoanalytical Characterization of Breakdown Spots in Ultrathin Gate Dielectrics

- Kin Leong Pey, Nanyang Technological University, Singapore

Performance Trends of Si-Based RF Transistors

- Frank Schwierz, Technical University Ilmenau, Germany

Modeling Current Transport in Ultra-Scaled Field Effect Transistors

- Siegfried Selberherr, Technische Universitaet Wien, Austria

Advanced Germanium MOS Devices and Technology

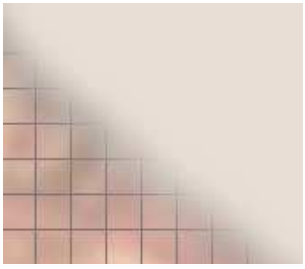
- Chi On Chui, Intel Corp, USA

A Fine-Tuned Low-Power LNA for Lower-Band UWB Transceiver

- Albert Wang, Illinois Institute of Technology, USA

An Analytic Theory of Dielectric and Optic Nonlinear Effects of Ferroelectrics

- Chuanren Yang, Institute of microelectronics and solid state electronics, University of Electronic Science and Technology of China, China



Device Simulation in Nanoelectronic Era

- Zhiping Yu, Institute of Microelectronics, Tsinghua University, China