CICC IEEE Custom Integrated Circuits Conference

...Innovation, Education, Communication

CICC Home
Registration
Papers & Presentations
General Information
Conference Events
Technical Program
Educational Sessions
Keynote Address
Conference Luncheon
Panel Discussions
Exhibits
Committee
Conference History

The Panel Discussions for 2005 are on Tuesday, September 20, 7:00 pm - 9:00 pm

Session 19 - Evening Panel Discussion
Oak Ballroom, Tuesday, September 20, 7:00 pm

Will Continued process-Node Shrinks Kill High-Performance Analog Design?

Organizer:
Jafar Savoj, Marvell Semiconductor

Moderator:
David Rich, Consultant

Panelists:
Brett Forejt, Texas Instruments
Peter Kinget, Columbia University
Un-Ku Moon, Oregon State University
Modest Oprysko, IBM
Behzad Razavi, University of California, Los Angeles
Hisashi (Sam) Shichijo, Texas Instruments
Albert Wang, Illinois Institute of Technology

Digital designers to take over the world when analog designers produce 10 Gbps 18-bit data converters that attach to antennas." This may be a dream, but many next-generation analog systems need high resolution (>12 bits) circuits that run at higher sampling rates. PLL designers can push the speed envelope, but what about other analog blocks? Has scaling finally driven analog design off the submicron roadmap as supply voltages dip below 1V and devices have more leakage paths than the average basement?

Come hear gurus debate the realities of the state-of-the-art transistor from now until the end of the decade. Learn what's ahead with transistors that will be able to do little more than divide by two at 500 GHz clock rates.

Session 20 - Evening Panel Discussion
Fir Ballroom, Tuesday, September 20, 7:00 pm

Foundries, EDA Vendors, and Designers: Who Shoulders the Blame When a Design Doesn't Work in Nano-Scale and Wireless Era?

Organizers:
Jamil Kawa, Synopsys
Yuhua Cheng, Siliconlinx Inc
Hiroshi Iwai, Tokyo Institute of Technology

Moderator:
Richard Goering, EE TIMES

Panelists:
Michael Campbell, Qualcomm
Raul Camposano, Synopsys
Jon Fields,Agere
Patrick Lin, UMC

Steve Lloyd, Beceem Communications
Joe Sawicki, Mentor Graphics
Ed Wan, TSMC

To support the significantly increased demand for compact, low cost, and low power design, both foundries and EDA vendors are heavily investing in developing the technology platform for nano-scale and RF technologies, which will become the mainstream chip manufacturing processes in the next 7-10 years. As both design and manufacturing technologies become more complex in the nano-scale and RF world, the technical challenges in designing and manufacturing chips with higher yields become much bigger, which escalates the time to market and the risk of failure of designed products. Also, the design and manufacturing cost in nano-scale technologies is much higher than ever before.

Here come the questions, when a very complex design targeting a very advanced technology does not work as intended the first time around, whose fault is it, the foundry's, the EDA vendor's, or the designer's? With a lot of fundamentals to be understood and a lot of technical barriers to be overcome in process technologies, device modeling, design methodologies, system architecture, & integration, can one part (either manufacturing foundries or EDA vendors) take the lead to be the driving force for the development of a solid technology platform? What will the new roles of foundries and EDA vendors be in the nano-scale and wireless technology era with these challenges and opportunities?

This panel is bringing together leading experts from foundries, EDA companies, and fabless chip design companies to review the new technology trend and technical barriers in the design cycle. It will be a discussion and debate to explore the direction of technology development in both foundries and EDA suppliers in nano-scale era. It promises to be a lively and animated event you don't want to miss!

Session 21 - Evening Panel Discussion
Pine Ballroom, Tuesday, September 20, 7:00 pm

Analog Behavioral Modeling: Fantasy, Fad, or Foundation for the Future?

Organizer:
Henry Chang, Designer's Guide Consulting
Colin McAndrew, Freescale Semiconductor

Moderator:
Colin McAndrew, Freescale Semiconductor

Panelists:
Asad Abidi, University of California, Los Angeles
Gayathri Bhagavatheeswaran, Freescale Semiconductor
Jim Holmes, Texas Instruments
Ken Kundert, Designer's Guide Consulting
Alan Mantooth, University of Arkansas
Tony Strachan, Philips

Bottoms-up verification and top-down design of large analog/mixed-signal ICs and systems clearly benefit the semiconductor industry in terms of shorter design cycles and fewer design iterations. An enabler for these processes is behavioral modeling, which makes simulation of large ICs and systems feasible for verification, and allows systems simulation for feasibility assessment, partitioning optimization, and specification development prior to schematic/physical implementation of low-level blocks.

There has been, and continues to be, a large investment by the CAD community in the development and enhancement of behavioral modeling languages, and in comprehensive multidisciplinary simulation environments that allow arbitrary mixing of behavioral and schematic/physical blocks derived from either digital or analog domains. However, the adoption of these capabilities by the design community appears to be progressing more slowly than originally anticipated.

The co-location of CICC2005 with BMAS2005 brings together experts from both the IC design side and on the CAD/modeling side, the major players and partners with a stake in behavioral modeling, and so presents an ideal opportunity for a joint panel to delve into the present status of analog

behavioral modeling for IC design.