Designing Analog and RF Circuits in Nanoscale CMOS Technologies: Scale the Supply,Reduce the Area and Use Digital Gates

講員： Prof. Peter Kinget

講題： Designing Analog and RF Circuits in Nanoscale CMOS Technologies: Scale the Supply,Reduce the Area and Use Digital Gates.

時間： 98年9月24日（四）pm 4：00 - 5：00

地點： 國立台灣大學電機二館105會議室

報名： 一律採線上報名

報名網址 http://wrl.ee.ntu.edu.tw/workshop/

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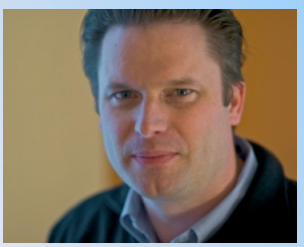

主講人簡介：

Peter R. Kinget received an engineering degree in electrical and mechanical engineering and the Ph.D. in electrical engineering from the Katholieke Universiteit Leuven, Belgium.

He has worked in industrial research and development at Bell Laboratories, Broadcom, Celight and Multilink before joining the faculty of the Department of Electrical Engineering, Columbia University, NY in 2002. His research interests are in analog and RF integrated circuits and signal processing using nanoscale CMOS technologies.

He has been an Associate Editor of the IEEE Journal of Solid State Circuits (2003-2007) and is currently an Associate Editor for the IEEE Transactions on Circuits and Systems II. He is also serving on the Technical Program Committees of the International Solid-State Circuits Conference and the European Solid-State Circuits Conference. He is a "Distinguished Lecturer" for the IEEE Solid-State Circuits Society.

主辦單位：國立台灣大學-聯發科技無線研究實驗室
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