Schedule

Tuesday Wednesday Thursday

Day 2 - Wednesday, January 5th, 2011

09:00	09:50	***Keynote:*** **The Future of Multicore** **Anant Agarwal (MIT, Tilera)**			
09:50	10:40	***Keynote:*** **Post-Silicon technologies: Prospects and Perspectives** **Kaushik Roy (Purdue University)**			
10:40	11:20	Break			
		Track A	Track B	Track C	Ind. Forum
11:20	12:35	**Session A4: Functional and Timing Verification** Chair: Praveen Tiwari	**Session B4: Embedded systems optimizations** Chair: Preeti Ranjan Panda	**Session C4: Analog Techniques_I** Chair: Shouribrata Chatterjee	**Session IFS3: Future Directions and Applications of Programmable Logic**
		A4.1: Auxiliary State Machines and Auxiliary Functions: Constructs for Extending AMS Assertions Subhankar Mukherjee and Pallab Dasgupta *IIT Kharagpur*	**B4.1:** Dual Code Compression for Embedded Systems Kartik Shrivastava and Prabhat Mishra *University of Florida, Gainesville*	**C4.1:** Design of a 20 MHz DC-DC Buck Converter with 84% Efficiency for Portable Applications Ashis Maity, Amit Patra, Norihisa Yamamura and Jonathan Knight *Indian Institute of Technology, Kharagpur and National Semiconductor, Tokyo, Japan*	**IFS3.1:** What's Next in Programmable Logic? Flexible Processing and Greater Applications Siddharth Rele *Xilinx*
		A4.2: Variation-Conscious Formal Timing Verification in RTL Jayanand Asok Kumar and Shobha Vasudevan *University of*	**B4.2:** A Scalable LDPC Decoder on GPU Kiran Kumar Abburi	**C4.2:** Low Offset, Low Noise, Variable Gain Interfacing Circuit with a Novel Scheme for Sensor Sensitivity and Offset Compensation for MEMS based, Wheatstone Bridge type, Resistive Smart Sensor A. Dutta and T.K. Bhattacharyya	**IFS3.2:** System-on-Chip Modeling using FPGA for Design Verification & HW-SW Co-Design Sabyasachi Dey *Qualcomm*

		Illinois at Urbana-Champaign		*IIT Kharagpur*	
		A4.3: A Novel Learning Framework for State Space Exploration based on Search State Extensibility Relation Maheshwar Chandrasekar and Michael Hsiao *Virginia Tech*	**B4.3:** Self-Immunity Technique to Improve Register File Integrity against Soft Errors Hussam Amrouch and Joerg Henkel *Karlsruhe Institute of Technology*	**C4.3:** A Low-Noise Low-Power Noise-Adaptive Neural Amplifier in 0.13um CMOS technology. Vikram Chaturvedi and Bharadwaj Amrutur *IISc Bangalore, India*	**IFS3.3:** Application Specific Designs for Embedded With Intel Atom Bhoopalgouda M P *Intel Embedded Communications Group* **IFS3.4:** Programmable Logic - From Glue Logic to System Platforms and Beyond Wikneswaran Pillai *CG-CoreEL*
12:35	13:45	**Lunch**			
13:45	14:35	***Keynote:* Designing Analog and RF Circuits in Nanoscale CMOS Technologies: Scale the Supply, Reduce the Area and Use Digital Gates.** **Peter Kinget (Columbia University)**			
14:35	15:50	**Session A5: Physical Design Optimizations for Design Closure** Chair: Sridhar Rangarajan	**Session B5: Nanoelectronics** Chair: Vaidyanathan Subramanian	**Session C5: Low Power Architectures and Algorithms** Chair: Madhurima Ghose	**Session IFS4: New Trends in Embedded Services and Solutions**
		A5.1: Improved timing window overlap check using statistical timing analysis Sachin Shrivastava and Harindranath Parameswaran *Cadence Design Systems*	**B5.1:** Modeling the Effect of Gate Fringing and Dopant Redistribution on the Inverse Narrow Width Effect of Narrow Channel Shallow Trench Isolated MOSFETs Srabanti Pandit and Chandan Kumar Sarkar *Jadavpur University*	**C5.1:** A General Algorithm for Energy-Aware Dynamic Reconfiguration in Multitasking Systems Weixun Wang, Sanjay Ranka and Prabhat Mishra *University of Florida, Gainesville*	**IFS4.1:** Trends in Embedded Design Services Gopi Bulusu *Sankhya*
		A5.2: An automated approach for minimum jitter buffered H-tree construction A. Mandal, N. Jayakumar, K. Bollapalli, S. P. Khatri and R. N.	**B5.2:** Development of a Micro-Mechanical Logic Inverter for Low Frequency MEMS Sensor Interfacing Subha Chakraborty and T K Bhattacharyya *IIT Kharagpur*	**C5.2:** Wakeup Time and Wakeup Energy Estimation in Power-Gated Logic Clusters Vivek T D, Olivier Sentieys and Steven Derrien *IRISA ENSSAT and IRISA IFSIC, France*	**IFS4.2:** Outsourced R&D in the Embedded Space Kunaal Mahanti *Wipro*

		Mahapatra *Texas A&M University, Juniper Networks and NVIDIA*			
		A5.3: Interconnected Tile Standing Wave Resonant Oscillator based Clock Distribution Circuits A. Mandal, V. Karkala, S. P. Khatri and R. N. Mahapatra *Texas A&M University*	**B5.3:** Performance Comparison of Thin-film Transistors Fabricated using Different Purity Semiconducting Nanotubes K. C. Narasimha Murthy and Roy Paily *IIT Guwahati*	**C5.3:** Trading Accuracy for Power with an Underdesigned Multiplier Architecture Parag Kulkarni, Puneet Gupta and Milos Ercegovac *UCLA*	**IFS4.3:** Trends in Embedded System Market: Accelerate To Win Rajarama Nayak *TCS*
15:50	16:15		Tea Break		
16:15	17:30	**Session A6: Embedded Tutorial 2** Chair: Adit Singh	**Session B6: Clock/interconnect** Chair: Ashok Balivada	**Session C6: Diagnosis and Debug** Chair: Mark Zwolinski	**Industry Forum**
		A6.1: Energy Efficient Designs with Wide Dynamic Range Vivek De *Intel*	**B6.1:** Feedback Based Supply Voltage Control for Temperature Variation Tolerant PUFs Vignesh Vivekraja and Leyla Nazhandali *Virginia Tech*	**C6.1:** Efficient Trace Signal Selection for Post Silicon Validation and Debug Kanad Basu and Prabhat Mishra *University of Florida, Gainesville*	**Panel IFP2:** Embedded Startups in an Emerging Market: Is there a Recipe for Success? Moderator: Vamsi Bopanna Panelists: Satya Gupta *(Concept2Silicon)* Manjunatha Hebbar *(HCL)* Hemant Kanakia *(VC)* Arnob Roy *(TEJAS)*
		A6.2 Test Scheduling for Deep Submicron Technologies Chunhua Yao, Kewal Saluja and Parameswaran Ramanathan *Univ. of Wisconsin-Madison*	**B6.2:** Ensuring On-Die Power Supply Robustness in High-Performance Designs S. Soman, A. Brahme, R. Venkatraman, R. Shaikh, S. Thiyagaraja and M. Patil *Texas Instruments India*	**C6.2:** Trace Buffer-Based Silicon Debug with Lossless Compression Sandesh Prabhakar, Rajamani Sethuram and Michael Hsiao *Virginia Tech and Qualcomm*	
			B6.3: Interconnect	**C6.3:** Multiple fault diagnosis	

		Modeling, Synchronization and Power Analysis for Custom Rotary Rings V. Honkote, A. More, Y. Teng, J. Lu and B. Taskin *Drexel University*	based on multiple fault simulation using Particle Swarm Optimization Subhadip Kundu, Santanu Chattopadhyay, Indranil Sen Gupta and Rohit Kapur *IIT Kharagpur and Synopsys*
17:30	18:30	**Break**	
18:30	20:30	***Awards and Banquet*** **Real Men Do Real Silicon** **Rajeev Madhavan (Magma)**	

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