

# ELEN6350

## High Dynamic Range Photodetector

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### Summary:

The use of image sensors presents several limitations for visible light spectrometers. Both CCD and CMOS one dimensional imagers typically use a global shutter, which is activated for a fixed time period determined by the control electronics. After the image is captured, each individual photodetector element is serially read out of the system through a multiplexer and shared charge amplifier. This process is time-consuming, and also relies on an estimate of the incoming signal to set the amplifier gain and integration time to avoid saturation of the brightest pixel. This effect also limits the dynamic range of the system. The nominal dynamic range is quite large – for the TAOS/ams 1401, for example, more than 1000:1 range can be achieved within a single exposure, and the exposure duration can be modulated over a further 3000:1 range. If the exposure time is incorrectly estimated or the difference between the bright and dark pixels is large, however, the net dynamic range is compromised and the full range is not realized. Overexposure/saturation can also lead to blooming and contribute noise to neighboring pixels.

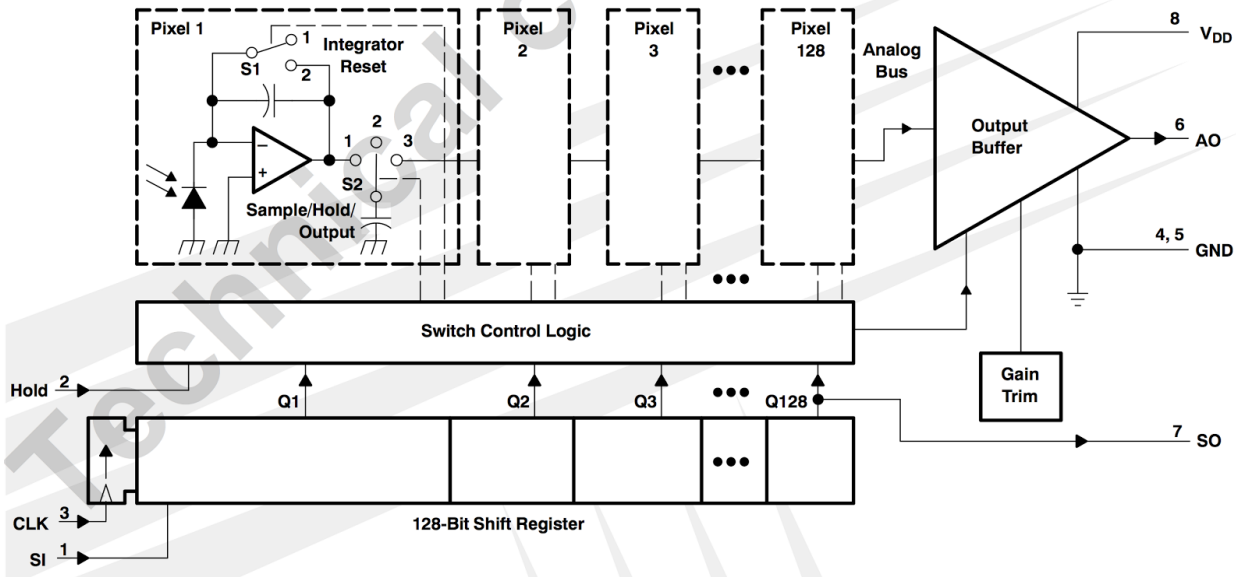


Figure 2a, 2b. Probed output voltage, comparator voltage, and photodiode voltage. Light intensity is proportional to the output voltage frequency. Figure 2b. illustrates the simplified pixel layout with the photodiode idealized as a current source and capacitor.

In this project, we design an image sensor integrated circuit that offers the potential for high dynamic range operation by digitizing light output at the pixel level. The design was carried out using the 180nm, IBM 7RF technology development kit. In what follows is a brief account of the design process , and some simulation and measured results.

## Concept overview:

The basic schematic of one pixel of the proposed imager is shown below. Incident light is sensed using a reverse biased CMOS photodiode. The photodiode can be modeled as a current source representing charge generation from incident light and a parasitic capacitor, corresponding to the diode junction capacitance, in parallel with the current source. The capacitor is initially charged to the supply voltage  $V_{DD}$  and the reset transistor is open circuited. Incident light causes the capacitor to discharge and subsequently the capacitor voltage decreases. As soon as the capacitor voltage crosses a threshold  $V_{ref}$ , the comparator block switches low. The switching output of the comparator passes through an inverting buffer and turns on the reset switch. The reset switch charges the capacitor back to  $V_{DD}$ . As the capacitor voltage increases, the comparator switches high. Once again the switching output of the comparator propagates through the inverting buffer, and after some delay depending on the buffer capacitance, the reset switch is open circuited once again. Subsequent illumination of the diode repeats the above cycle. At the output node, Pixel Output, a pulse edge is observed.

As a result of the above operation, the circuit converts a quantum of incident light into a pulse train. The intensity of the incident light is encoded in the frequency of the pulse train with larger frequency corresponding to higher illumination intensity and vice versa. The waveforms below demonstrate the operation of the pixel by highlighting the outputs of three nodes in the circuit during operation.

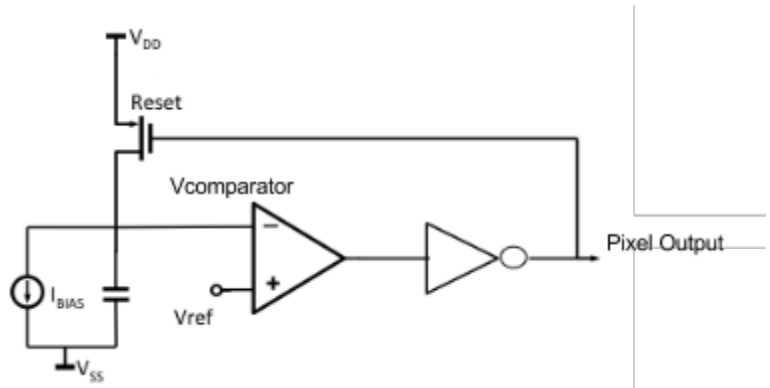
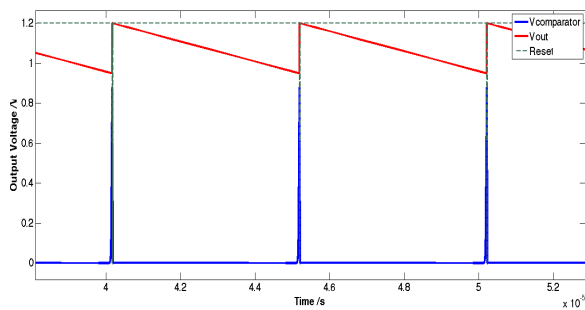


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## Circuit Architecture

	Pixels	Multiple PD Types	Decoder	Bias Network
Proposed	7 Single Pixels	NA	NA	NA
Taped-out	7 Single Pixels	4 Types of PD	32 Pixel Decoder	Improved

Table 1. Circuit architecture that we originally proposed vs. taped-out architecture

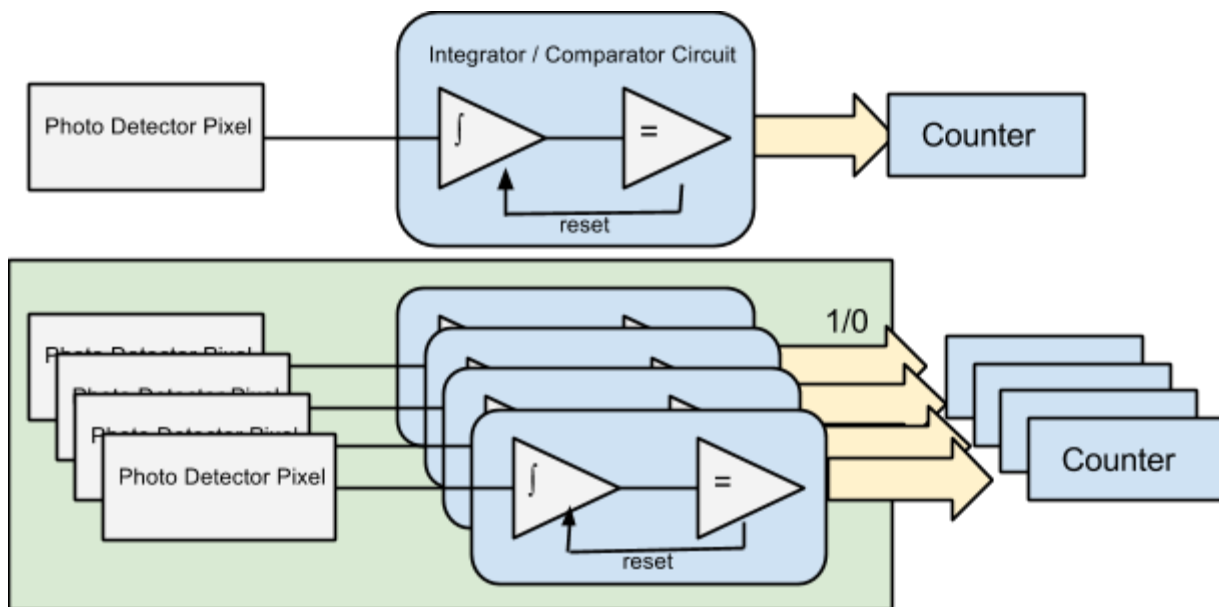


Figure 3. Idealized circuit architecture.

### Photodiode:

Each photodiode must be coupled to its own integrator/comparator circuit, because of this high amount of integration size is critical and the width must contain both the photodiode and the pixel control circuitry since both the photodiode and control circuitry are implemented in the silicon layer. Photodiode dimensions of  $100\mu\text{m}$  by  $0.5\mu\text{m}$  were chosen for the above reason. A photodiode area of  $100\mu\text{m}$  by  $0.5\mu\text{m}$  leads to a parasitic capacitance of approximately  $1\text{fF}$  [2]. The photodiode can be modelled as a current source in parallel with a parasitic resistance and capacitor.

During design, to estimate the expected photo-diode current output, we assumed a minimum illumination intensity of  $1\mu\text{W}/\text{cm}^2$ . From published literature, photodiodes fabricated in standard CMOS processes have demonstrated measured conversion efficiencies of  $0.378\text{A}/\text{cm}^2$  [2]. With an active area of  $100\mu\text{m} \times 0.5\mu\text{m}$  as mentioned above, the minimum photodiode output current is therefore, one can expect an output current magnitude of approximately  $0.2\text{pA}$ .

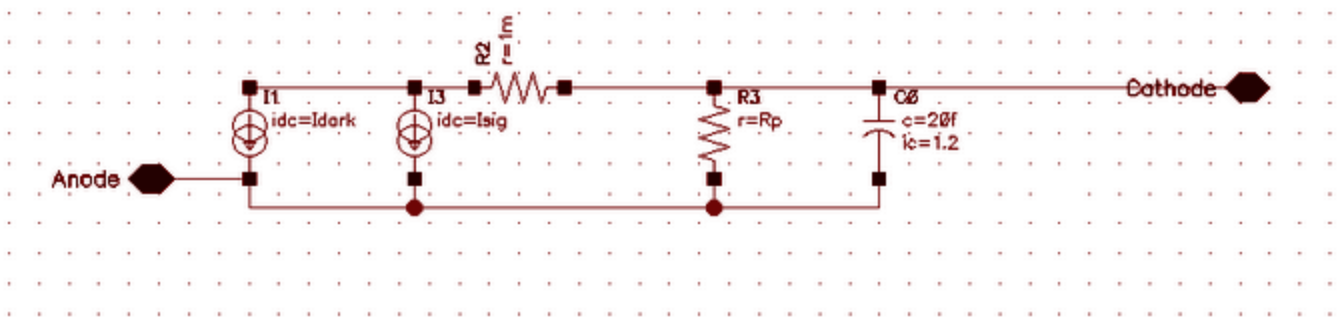


Figure 4. Idealized photodiode schematic.

### Pixel Design

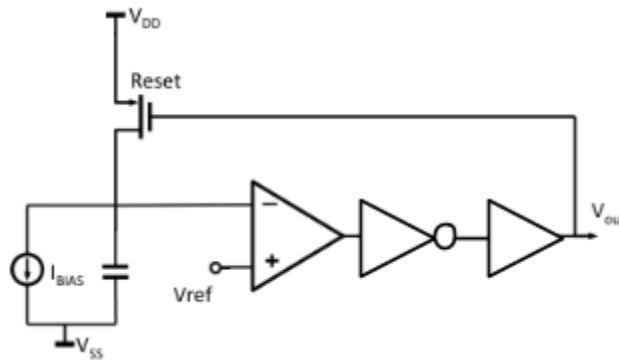


Figure 5 Pixel Layout. A photodetector pixel consists of a photo-diode, simulated using a capacitor and current source, a comparator and inverter plus buffers.

In figure 5, each photodiode is coupled to its own integrator/comparator circuit. Therefore, for the sake of array implementations, the width of each pixel contains both the photodiode and the pixel control circuitry since both the photodiode and control circuitry are implemented in the silicon layer. Photodiode dimensions of  $100\mu\text{m}$  by  $0.5\mu\text{m}$  are chosen for the above reason. A photodiode area of  $100\mu\text{m}$  by  $0.5\mu\text{m}$  leads to a parasitic capacitance of approximately  $1\text{fF}$  [2].

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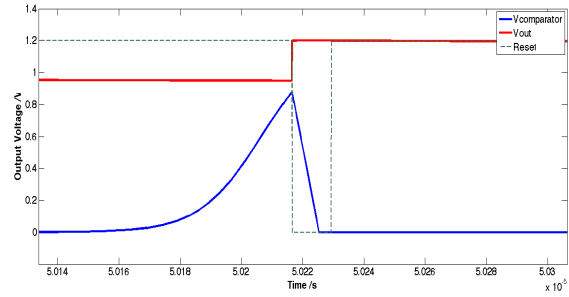
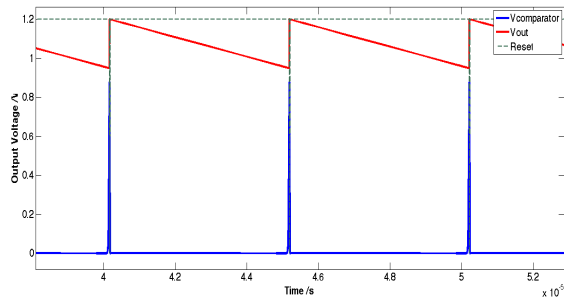


Figure 5a, 5b. Probed output voltage, comparator voltage, and photodiode voltage. Light intensity is proportional to the output voltage frequency. Figure b. is a zoomed in version of figure a. showing the reset signal detail.

The core of each pixel circuit is the integrator/comparator block. The integrator integrates the output current of the photodiode over a specified integration time. Once, the output of the integrator crosses a threshold set by an external analog voltage reference, a count is triggered in a digital counter and the integrator is reset

The output of the integrator is defined by the following:  $\int_0^{T_{int}} \frac{I_{in}}{C_{int}}$ . For a constant input current, the output voltage is given by  $V_{out} = \frac{I_{in} * T_{int}}{C_{int}}$ . Therefore, it is clear that the degree of signal amplification (transimpedance gain) is directly determined by the magnitude of the integration capacitor and the integration time. From the above **minimum current limit** of 0.2pA, combined with an integration capacitor of 200fF and an integration time of 1s, the output voltage is 750mV which can easily be discriminated by a comparator circuit.

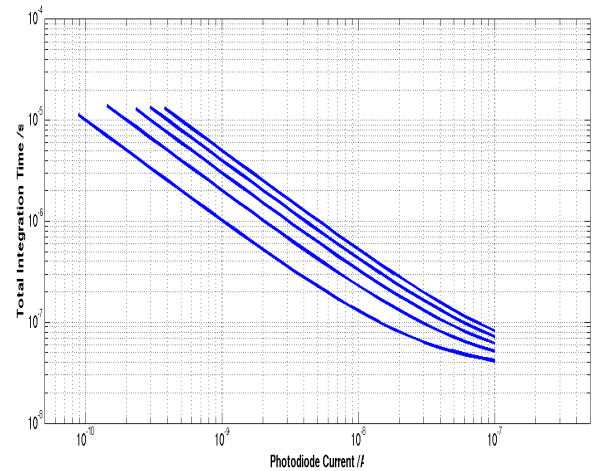
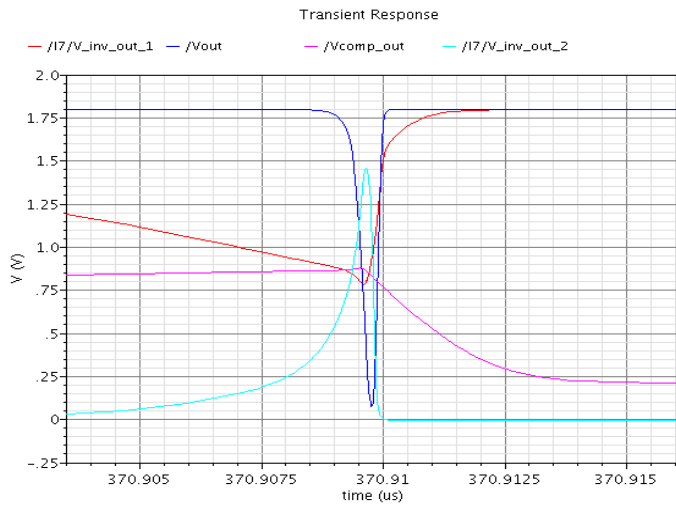


Figure 6a, 6b. Transient response of the switching waveform, comparator output and the reset signal for a diode current of 10nA and the following inverter stages. 6b is the system linearity vs the photodiode current for increasing  $V_{ref}$

### Dynamic Range:

The most important parameter of the photodetector is its ability to detect faint signals as well as strong signals with a range of 100dB.

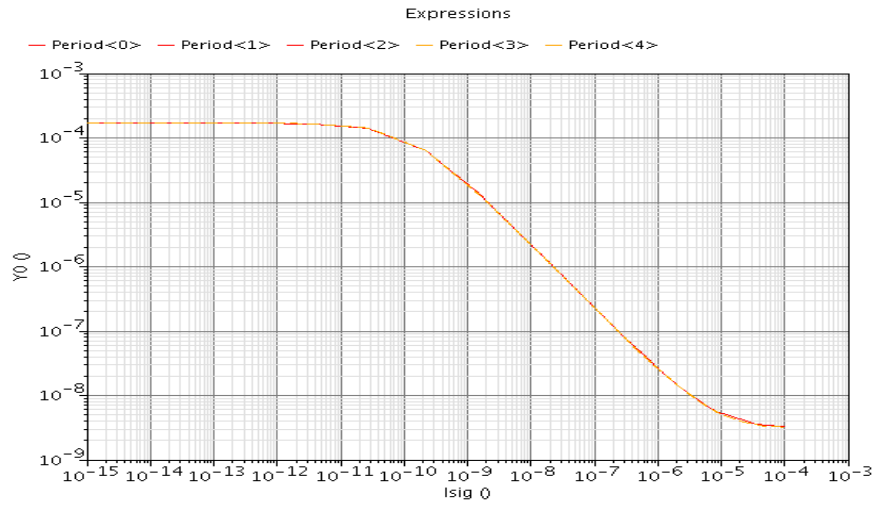


Figure 7. Diode current of the photodetector array at 80°C and 0°C vs. integration time. The dynamic range is roughly 100dB.

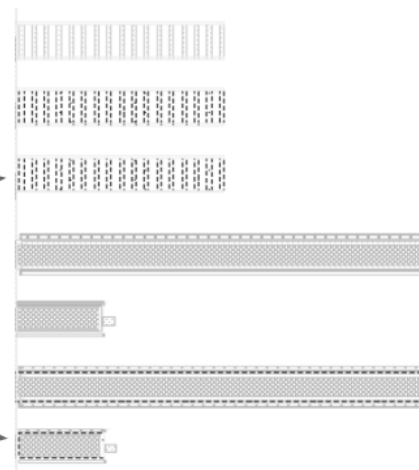
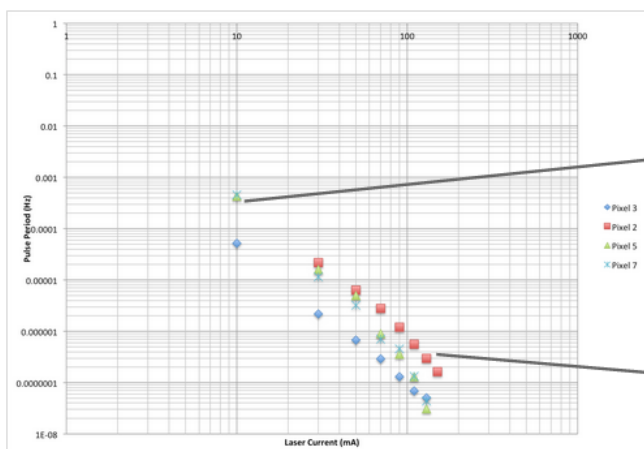
### Measurement Setup and Results

**Different Diode Topologies were used:**

N+/P-substrate and N-well/P-substrate non-fingered diodes in two sizes (10umx35um and 10umx100um) and fingered N+/P-substrate and N-well/P-substrate diodes in one size (100umx35um).

**Pixel Photodiodes**

**Measured Dynamic Range ( Preliminary)**



**Operating Parameters:**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	$V_{supply}$		1.6	1.8	2	V
Photodiode Charging Voltage Range	$V_{cref}$		0		1.8	V
Comparator Reference Voltage Range	$V_{ref}$		0		1.8	V
Enable Voltage	$V_{en}$			1.8		
Decoder input voltage	$V_{dec}$			1.8		V
Max output load capacitance	$C_{load}$				10	pF
Max Power Consumption	$Power_{max}$			1.2	4	mW
Dynamic Range	$DR_{25}$	$T_c = 25^\circ$		100		dB
Dynamic Range	$DR_0$	$T_c = 0^\circ$		100		dB
Dynamic Range	$DR_{80}$	$T_c = 80^\circ$		100		dB
Inverter Delay	$Delay_{inv}$			11		pS
OTA Current Consumption				45		uA
OTA Slew Rate				1		MV/s
Maximum Frequency	$F_{max}$			10		MHz
Configuration	conf			39		Pixels
Photo Diode Dark Current	$I_{dark}$			20		pA
Photo Diode Capacitance	$C_{diode}$			200		fF
Min PD Current	$I_{min}$			0.2		pA
Max PD Current	$I_{max}$			10		nA

**References:**

1. Fossum, Eric. "The Quanta Image Sensor (QIS): Concepts and Challenges." *Imaging Systems and Applications*. Optical Society of America, 2011.

2. Tavernier, Filip, and Michiel Steyaert. *High-Speed Optical Receivers with Integrated Photodiode in Nanoscale CMOS*. Vol. 5. Springer, 2011.
3. Baker, Bonnie C. "Improved noise performance of the ACF2101 switched integrator." *Application Bulletin, Burr-Brown* (1993).
4. Johns, David A., and Ken Martin. *Analog integrated circuit design*. Wiley. com, 2008.