# EE6350: Class-D Audio Amplifier Datasheet

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## 1 Key Features

- 1.5% THD+N
- 30dB Dynamic Range
- PSRR $>$ 30dB
- Efficiency $>$ 85%
- 170mA (rms) output stage drive strength
- Output power of 150mW
- Filterless design

## 2 Introduction

Class D amplifier is a type of power amplifier that is typically used in mobile systems due to its high efficiency. The basic operating principle of the amplifier utilizes transistors as switches instead of analog amplifiers. The input signal is first used to pulse width modulate a high frequency signal (outside the audio band). This pulse width modulated signal is then used to connect the load to either $V_{DD}$ or $GND$. Since the duration of a given current flow direction through the load is determined by the amplitude of the signal, the low frequency component at the output accurately tracks the applied signal.

This is a datasheet of bridged three-level class-D amplifier. As opposed to conventional half-bridge and full-bridge variants of the class-D amplifier, this topology eliminates the need for the low pass filter at the output, thereby improving the efficiency of the amplifier. The top-level schematic for the system can be seen in Figure1.

## 3 Pin Configuration

The pin configuration of the proposed amplifier is shown in Table 1. Pin out view of the chip is shown in figure 2. Each of the observation points are connected to the corresponding pads through a transmission gate. During debugging, the transmission gates are enabled so that the observation points in the circuit are connected to the pads. However, during normal operation, the transmission gates are disabled so that the circuit does not see the effects of the pad parasitics.

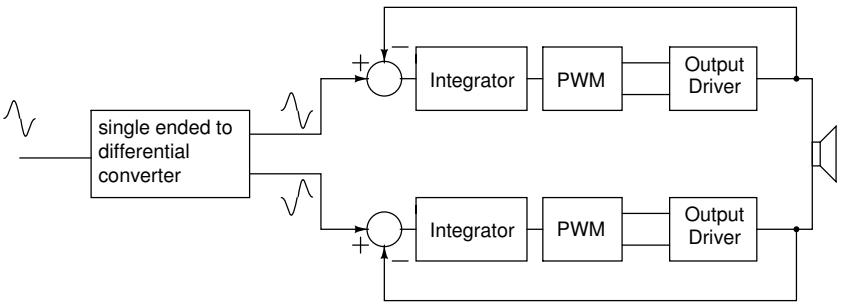


Figure 1: Top-level schematic of the class-D amplifier

| Section | S.No. | Pin Name | Pin Count | Comments |
|---|---|---|---|---|
| Supply Pins | 1 | $PV_{DD}$ | 3 | Driven from high current limit 1.8V supply |
| | 2 | $AV_{DD}$ | 1 | Driven from 1.8V supply |
| | 3 | $V_{SS}$ | 6 | Analog and digital $V_{SS}$ internally shorted |
| Observation Pins | 4 | Triangle wave | 1 | Check output of generated triangle wave |
| | 5 | Non overlap generator | 2 | Observe dead time and its effect on THD |
| | 6 | Comparator | 1 | Check PWM comparator output |
| Inout Pins | 7 | Output+ | 3 | 80mA per pin |
| | 8 | Output- | 3 | 80mA per pin |
| | 9 | Input | 1 | Single ended input |
| | 10 | Bias current | 1 | $10\mu A$ current source |
| | 11 | Reference Voltage | 1 | Connect to nominal voltage of 0.9V |
| Bypass Pins | 12 | Triangle Bypass | 2 | 1 for supplying triangle wave, one for controlling bypass |
| Control Pins | 13 | Buffer enable | 1 | Disable observation transmission gates during normal use |
| | 14 | Feedback | 2 | One pin per channel for closing the feedback loop |
| | | **Total pins** | 28 | |

Table 1: Pin Configuration

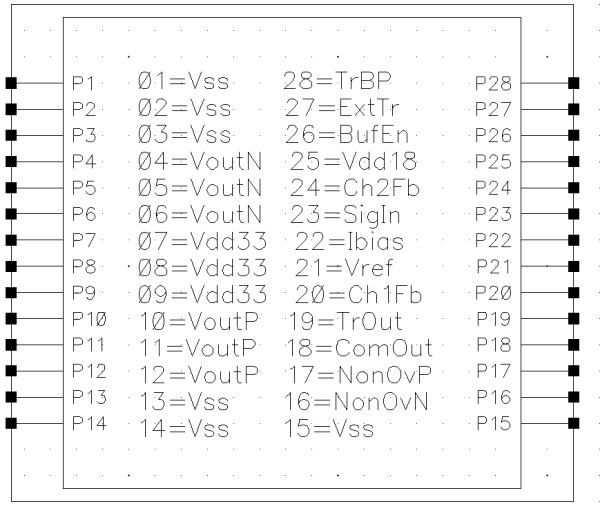


Figure 2: Pin-out of the chip

# 4 Application diagram

Figure 3 shows the application level connection for the Class D Amplifier chip.

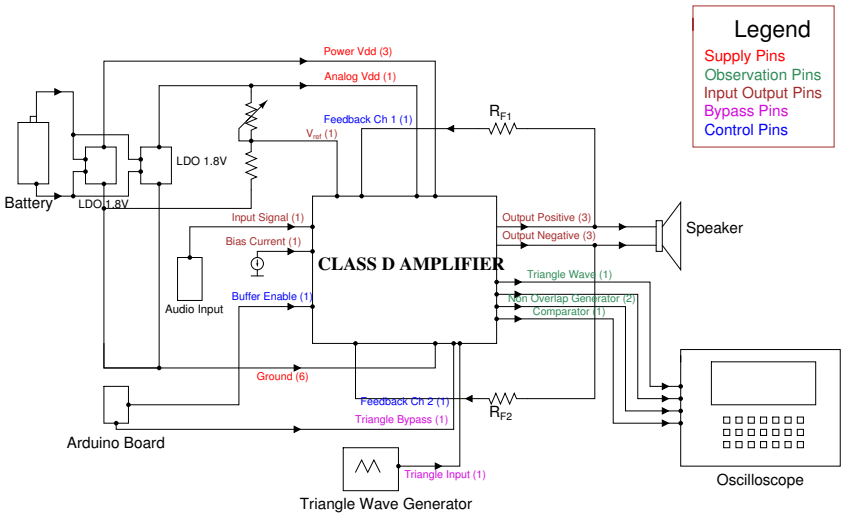


Figure 3: Typical PCB level connections

# 5 Debugging mode

The chip has Buffer enable digital pin, which when switched on, enables probing outputs of different sub-circuits, namely triangle wave, non-overlap generator and comparator. It also has 2 pins for providing external triangle wave (1 digital pin for enabling external triangle wave, and other analog pin for providing the triangle wave).
Other pins that can be used for debugging are the feedback pins, which enable probing the output of single ended to differential converter.

# 6 Performance

Typical performance values are provided in table 2

| S.No. | Parameter | Typ. Value | Units |
|---|---|---|---|
| 1 | Supply Voltage | 1.8 | V |
| 2 | Max input Amplitude | 0.45 | V |
| 3 | Max rms current | 170 | mA |
| 4 | Max output power | 150 | mW |
| 5 | Max THD+N (SNDR) | 36 | dB |
| 6 | Output stage resistance | 0.8 | Ω |
| 7 | Max Input/Output frequency | 20 | KHz |
| 8 | Input triangle wave frequency | 500 | KHz |

Table 2: Performance parameters

# 7 Typical Output Spectrum

Typical Output spectrum for input of 400mV (-7dB approx) is as shown in figure 4. The SNDR in this case is 35dB (about 1.4% THD+N).

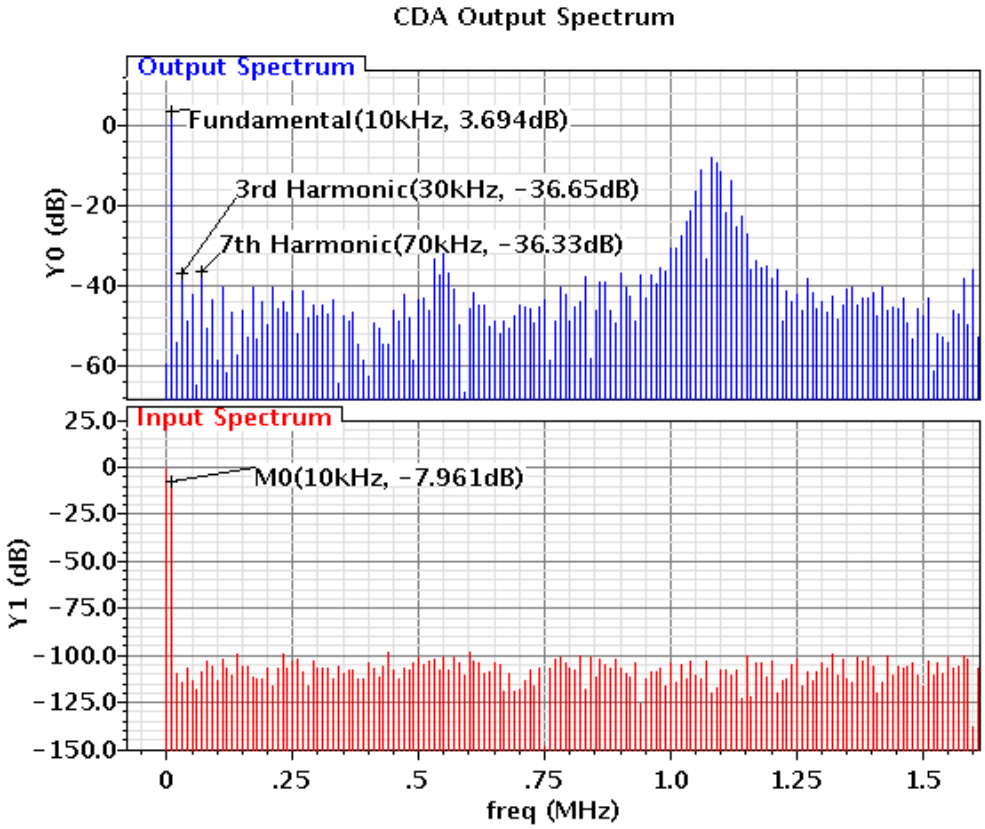


Figure 4: Spectrum at the input and output of the class-D amplifier for a 10kHz 400mV input amplitude