# A Pipelined 5-Msample/s 9-bit Analog-to-Digital Converter 

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#### Abstract

A pipelined, 5-Msample/s, 9-bit analog-to-digital (A/D) converter with digital correction has been designed and fabricated in $3-\mu \mathrm{m}$ CMOS technology. It requires $8500 \mathrm{mil}^{2}$, consumes 180 mW , and has an input capacitance of $\mathbf{3} \mathbf{p F}$. A fully differential architecture is used; only a two-phase nonoverlapping clock is required, and an on-chip sample-and-hold ( $\mathrm{S} / \mathrm{H}$ ) amplifier is included.


## I. Introduction

TRADITIONAL designs of high-speed CMOS analog-to-digital (A/D) converters have used parallel (flash) architectures [1]-[13]. While flash architectures usually yield the highest throughput rate, they tend to require large silicon areas because of the many comparators required. An important objective is the realization of high-speed A/D converters in much less area than that required by flash converters so that the $\mathrm{A} / \mathrm{D}$ interface function can be integrated on the same chip with associated complex, high-speed, image-processing functions. Multistage conversion architectures reduce the required area by reducing the total number of comparators [14]-[19]. Using a pipelined mode of operation in these architectures allows the stages to operate concurrently and makes the maximum throughput rate almost independent of the number of stages. Also, digital correction techniques significantly reduce the sensitivity of the architecture to certain component nonidealities. Pipelined configurations have been previously applied in high-performance board-level converters, but they have not been applied to monolithic CMOS A/D converters because of the difficulty of realizing high-speed interstage sample-and-hold ( $\mathrm{S} / \mathrm{H}$ ) gain functions in CMOS technologies. In this paper, an experimental four-stage pipelined A/D converter with digital correction that has 9 -bit resolution and 5 -Msample/s conversion rate in a $3-\mu \mathrm{m}$ CMOS technology is described. The experimental converter uses high-speed differential switched-capacitor circuitry to carry out the interstage gain functions.

This paper is divided into four additional parts. In Section II, pipelined A/D architectures are described con-

[^0]ceptually, and their advantages over flash and two-step subranging architectures [17] are explained. In Section III, the error sources present in pipelined A/D converters are identified, and the way in which digital correction eliminates the effects of some of these errors is shown. In Section IV, the circuits in an experimental prototype are described. Finally, experimental results from the prototype converters are given in Section V.

## II. Conceptual Description

A block diagram of a general pipelined A/D converter with $k$ stages is shown in Fig. 1. Each stage contains an S/H circuit, a low-resolution A/D subconverter, a lowresolution digital-to-analog (D/A) converter, and a differencing fixed-gain amplifier. In operation, each stage initially samples and holds the output from the previous stage. Each stage then does a low-resolution A/D conversion on the held input, and the code just produced is converted back into an analog signal by a D/A converter. Finally, the D/A converter output is subtracted from the held input, producing a residue that is amplified and sent to the next stage.

The primary potential advantages of the pipelined architecture are high throughput rate and low hardware cost. The high throughput rate of the pipelined architecture stems from concurrent operation of the stages. At any time, the first stage operates on the most recent sample, while the next stage operates on the residue from the previous sample, and so forth. If the A/D subconversions are done with flash converters, a pipelined architecture only needs two clock phases per conversion. Flash architectures also require two clock phases per conversion, one each for sampling and A/D conversion, and use pipelining to do the digital decoding operation. The throughput rate of flash converters is maximized because their pipelined information is entirely digital and can be transferred to 1-bit accuracy in less time than it takes to generate and transfer the analog residue in a pipelined multistage architecture. The area and consequent manufacturing cost of pipelined converters is small compared to those of flash converters, however, because pipelined converters require fewer comparators than flash converters. For example, the 9-bit prototype pipelined converter described in Section IV


Fig. 1. Block diagram of a general pipelined $\mathrm{A} / \mathrm{D}$ converter.
uses 28 comparators and requires a core area of 8500 $\mathrm{mil}^{2}$ in a $3-\mu \mathrm{m}$ CMOS technology. A 9-bit flash converter would use 512 comparators and would be more than ten times larger than the pipelined prototype in the same technology. Not only is the area small for pipelined converters, but also it is linearly related to the resolution because if the necessary accuracy can be achieved through calibration or trimming, the resolution can be increased by adding stages to the end of the pipeline without increasing the number of clock phases required per conversion. In contrast, flash and subranging architectures need exponential, rather than linear, increases in area to increase their resolution and also require trimming or calibration for greater than 8 - or 9 -bit linearity.

Other advantages of the pipelined architecture stem from the use of $\mathrm{S} / \mathrm{H}$ amplifiers to isolate the stages. First, because an $\mathrm{S} / \mathrm{H}$ amplifier can also be used on the input of the A/D converter, pipelined architectures can accurately sample high-frequency input signals. Second, the interstage gains from these amplifiers diminish the effects of nonidealities in all stages after the first stage on the linearity of the entire conversion; furthermore, this allows the converter to use a digital correction technique in which nonlinearity in the $A / D$ subconversions has little effect on the overall linearity. This subject is presented in Section III.

The main disadvantage of pipelined $A / D$ converters is that they require the use of operational amplifiers (op amps) to realize parasitic-insensitive $\mathrm{S} / \mathrm{H}$ amplifiers. Although the $\mathrm{S} / \mathrm{H}$ amplifiers improve many aspects of the converter performance, the op amps within the $\mathrm{S} / \mathrm{H}$ amplifiers limit the speed of the pipelined converters. In contrast, op amps are not required in subranging architectures. Because high-speed op amps are difficult to realize, a common goal in the design of subranging A/D converters is to avoid using op amps. If op amps are not used, however, it is impossible to realize parasitic-insensitive $\mathrm{S} / \mathrm{H}$ amplifiers. The consequent high-frequency input sampling is poor, stage operation is sequential, and tolerance to error sources in stages after the first is unimproved from that of the first stage. Also, flash converters usually do not use an input $\mathrm{S} / \mathrm{H}$ amplifier because of the difficulty in realizing an op amp in CMOS technologies that is fast enough to drive the inherently large input load. Therefore, flash converters often suffer reduced performance at high input signal frequencies.


Fig. 2. Block diagram of a two-stage pipelined A/D converter with offset and gain errors.

## III. Error Sources

The primary error sources present in a pipelined $A / D$ converter are offset errors in the $\mathrm{S} / \mathrm{H}$ circuits and amplifiers, gain errors in the $\mathrm{S} / \mathrm{H}$ circuits and amplifiers, $\mathrm{A} / \mathrm{D}$ subconverter nonlinearity, $\mathrm{D} / \mathrm{A}$ subconverter nonlinearity, and op-amp settling-time errors. With digital correction, as shown below, the effects of offset, gain, and A/D subconverter nonlinearity are reduced or eliminated; therefore, the $\mathrm{D} / \mathrm{A}$ converter nonlinearity and op-amp settling-time errors limit the performance of pipelined $A / D$ converters. To begin the error analysis, the effects of offset and gain errors are considered next.

A block diagram of a two-stage pipelined $A / D$ converter with offset and gain errors in each of the $\mathrm{S} / \mathrm{H}$ circuits and the interstage amplifier is shown as a representative example in Fig. 2. The nonideal $\mathrm{S} / \mathrm{H}$ circuits and interstage amplifier are replaced by ideal elements in series with gain and offset errors, and each of these replacements is surrounded by a dotted line. The gain error in the first-stage $\mathrm{S} / \mathrm{H}$ circuit changes the conversion range of the A/D converter and does not affect linearity. The gain errors in the interstage amplifier and second-stage $\mathrm{S} / \mathrm{H}$ circuit can be combined into one equivalent error that does affect linearity. However, because the interstage gain only has to be accurate enough to preserve the linearity of the stages after the first stage, the effect of this gain error on linearity is small. For example, if both stages in Fig. 2 have 4-bit resolution, and if the only error is in the gain of the interstage amplifier, the interstage amplifier gain should be equal to 16 and must be accurate to within $\pm 3$ percent.

The offset error in the first-stage $\mathrm{S} / \mathrm{H}$ circuit causes an input-referred offset but does not affect linearity. The offset errors in the interstage amplifier and second-stage $\mathrm{S} / \mathrm{H}$ circuit can be combined into one equivalent offset that does not affect linearity if digital correction is used. Because addition is commutative, the equivalent offset can be pushed to the left of the first-stage subtractor. To move the equivalent offset to the input branch, where is causes an input-referred offset; an equal but opposite offset must be inserted in the first-stage A/D subconverter branch. As shown below, the effect of the offset in the first-stage $A / D$ subconverter is eliminated by the digital correction.

Next, the effect of nonlinearity in the first-stage A/D subconversion is considered. A block diagram of one stage in a pipelined A/D converter is shown in Fig. 3(a). A 2-bit stage is used as a representative example. Nonlinearity in

(a)

(b)

(c)

Fig. 3. (a) Block diagram of one 2-bit stage in a pipelined $A / D$ converter. (b) Ideal residue versus input. (c) Residue versus input with A/D subconverter nonlinearity.
the $A / D$ subconverter is modeled as an input-referred linearity error. The effect of this nonlinearity is studied by examining plots of the residue versus the input. Two such plots are shown in Fig. 3(b) and (c).

In Fig. 3(b), both the A/D subconverter and the D/A converter are assumed to be ideal. The plot has a sawtooth shape because when the input is between the decision levels determined by the $A / D$ subconverter, the $A / D$ subconverter and D/A converter outputs are constant; therefore, the residue rises with the input. When the input crosses a decision level, the $A / D$ subconverter and $D / A$ converter outputs increase by one least significant bit (LSB) at a 2-bit level, so the residue decreases by 1 LSB . Here, the residue is always between $\pm 1 / 2 \mathrm{LSB}$ and consists only of the part of the input that is not quantized by the first stage. With the interstage gain equal to 4 , the maximum residue is amplified into a full-scale input to the next stage; therefore, the conversion range of the next stage is equal to the maximum residue out of the first stage.

A similar curve is shown in Fig. 3(c) for a case when the $\mathrm{A} / \mathrm{D}$ subconverter has some nonlinearity, but the $\mathrm{D} / \mathrm{A}$ converter is still ideal. In this example, two of the $A / D$ subconverter decision levels are shifted, one by $-1 / 2$ LSB and the other by $+1 / 2$ LSB. When the input crosses a shifted decision level, the residue decreases by 1 LSB. If the decision levels are shifted by less than $1 / 2 \mathrm{LSB}$, the residue is always between $\pm 1$ LSB. Here, the residue consists of both the unquantized part of the input and the error caused by the A/D subconverter nonlinearity. Be-


Fig. 4. Block diagram of a two-stage pipelined A/D converter with digital correction.
cause the $\mathrm{D} / \mathrm{A}$ converter is assumed to be ideal, these increased residues are accurate for the codes to which they correspond; therefore, at this point, no information is lost. If the interstage gain is still 4 , however, information is lost when the larger residues saturate the next stage and produce missing codes in the conversion. Therefore, if the conversion range of the second stage is increased to handle the larger residues, they can be encoded and the errors corrected. This process is called digital correction [20], [21] and is described next.

A block diagram of a two-stage pipelined A/D converter with digital correction is shown in Fig. 4. The new elements in this diagram are the pipelined latches, the digital correction logic circuit, and the amplifier with a gain of 0.5 . The amplifier with a gain of 0.5 is conceptual only and is drawn to show that the interstage gain is reduced by a factor of 2 so that nonlinearity error in an amount between $\pm 1 / 2$ LSB at a $n 1$-bit level in the firststage $\mathrm{A} / \mathrm{D}$ subconversion does not produce residues that saturate the second stage. If the first stage is perfectly linear, only half the conversion range of the second stage is used. Therefore, 1 bit from the second stage is saved to digitally correct the outputs from the first stage; the other $n 2-1$ bits from the second stage are added to the overall resolution. After the pipelined latches align the outputs in time so that they correspond to one input, the digital correction block detects overrange in the outputs of the second stage and changes the output of the first stage by 1 LSB at a $n 1$-bit level if overrange occurs. Digital correction improves linearity by allowing the converter to postpone decisions on inputs that are near the first-stage A/D subconverter decision levels until the residues from these inputs are amplified to the point where similar nonlinearity in later-stage A/D subconverters is insignificant.

To do the digital correction, a correction logic circuit is required. Also, if flash converters are used in the stages, all stages after the first require twice as many comparators as without digital correction. The logic is simple, however, and none the comparators needs to be offset canceled.

It is shown above that with digital correction, nonlinearity in the A/D subconverters can be corrected if the D/A converter is ideal. Therefore, the D/A converter in the first stage determines the linearity of the entire A/D converter. Such D/A converters can be realized with resistor strings for linearities in the 8-9-bit range. For integral linearity greater than 9 bits, the design of such a D/A converter is not trivial and either requires calibration or
trimming. Also, fast settling op amps are required to do analog subtraction and amplification at the sampling rate of the A/D converter. The $3-\mu \mathrm{m}$ CMOS prototype described in Section IV is able to do these functions at 5 Msample/s. The maximum speed of such processing increases in scaled technologies, and video conversion rates should be achievable in $1.5-2-\mu \mathrm{m}$ CMOS technologies.

## IV. Prototype

Several important design considerations for the prototype converter are now presented. To minimize design time, assume that all stages are identical. Fast op amps and flash subconverters are used to operate at as high a speed as possible. The most basic architectural decision is to choose the resolution per stage; for efficient use of the conversion range of each stage, this choice determines the corresponding value of interstage gain. To attain maximum throughput rate, the resolution per stage should be small so that the interstage gain is small and the corresponding closed-loop bandwidth of the gain block is large. Conversely, large resolution and corresponding gain per stage are desirable to achieve high linearity because the contributions of nonidealities in all stages after the first are reduced by the combined interstage gain preceding the nonideality. Thus the speed and linearity requirements conflict in determining the optimum resolution per stage. It also can be shown under certain simplifying assumptions that to minimize the amount of required hardware, the optimum resolution per stage is about 3 or 4 bits per stage, which is about midway between the high and low end. This compromise in the resolution per stage keeps both the number of op amps and the number of comparators small. Finally, because the goal of this project was to realize an A/D converter small enough that it could be incorporated within a primarily digital chip, the A/D converter must be able to operate in the presence of large power supply noise caused by the digital circuits. To reduce the sensitivity of the converter to this nbise, all analog signal paths in the prototype are fully differential.
To meet these requirements, the prototype is divided into four stages with 3 bits produced per stage. A block diagram of one stage is shown in Fig. 5. The A/D subconversions are done with flash converters, so each stage needs seven comparators. The $\mathrm{S} / \mathrm{H}$ amplifier block replaces both the $\mathrm{S} / \mathrm{H}$ circuit and interstage amplifier shown in earlier figures. Because the interstage gain is 4 instead of 8 , half the range and one bit from each of the last three stages are saved to digitally correct the outputs of the previous stages. Thus, instead of obtaining 3 bits of resolution from each of these stages, only 2 bits of resolution are obtained from each. The digital correction is done off the chip. In total, 9 bits of resolution are produced, using 28 comparator and four op amps.

The $\mathrm{S} / \mathrm{H}$ amplifier block is expanded in Fig. 6(a). Fig. 6(b) shows that the clock is divided into two nonoverlapping phases. On clock phase $\phi_{1}$, the input is sampled onto


Fig. 5. Block diagram of one stage in the prototype.


Fig. 6. (a) Schematic of $\mathrm{S} / \mathrm{H}$ amplifier. (b) Timing diagram of a twophase nonoverlapping clock.
the $4 C_{I}$ capacitors, and the integrating $C_{I}$ and commonmode feedback $C_{C M}$ capacitors are reset. On $\phi_{2}$, the left sides of the sampling capacitors are connected together so the difference between the two sampled inputs is amplified by the ratio of the sampling to integrating capacitors. To the extent that the op amp in a closed-loop configuration drives its differential input to zero, the gain is insensitive to parasitic capacitances on either the top or bottom plates of any of these capacitors. Meanwhile, the common-mode feedback (CMFB) capacitors are connected to the outputs of the op amp to start the CMFB circuit: Switched-capacitor CMFB is useful in pipelined A/D converters because pipelined converters inherently allow a clock phase needed to reset the capacitor bias.
As a result of the use of digital correction, the offsets of all the op amps are simply referred to the input of the A/D converter, each in an amount diminished by the combined interstage amplifier gain preceding the offset. Therefore, the op amps do not have to be offset canceled and do not have to be placed in a unity-gain feedback configuration. Since the op amps do not have to be unitygain stable, their speed can be optimized for a closed loop gain of 4. The op amp, shown in Fig. 7, uses a fully differential, class $A / B$ configuration with dynamic bias. The class $A / B$ structure gives both high slew rate and high gain after slewing. According to simulation, the amplifier dissipates 20 mW and settles in 50 ns to an accuracy of 0.1 percent with a $5-\mathrm{V}$ differential step into a $4-\mathrm{pF}$ load.


Fig. 7. Op-amp schematic.

The op amp is similar to one reported by Castello and Gray [22], and its operation is now described. Transistors $M_{1}-M_{4}$ form the input stage and generate the class $A / B$ action. Source followers $M_{5}-M_{8}$ are used to bias the input stage so that it conducts some current even for zero differential input. For an increase in the voltage on the positive input and a corresponding decrease on the negative input, the gate-to-source voltages of both $M_{1}$ and $M_{4}$ increase while those of $M_{2}$ and $M_{3}$ decrease; therefore, the current in $M_{1}$ and $M_{4}$ increases and that in $M_{2}$ and $M_{3}$ decreases from their standby values. Transistors $M_{9}$ and $M_{13}, M_{10}$ and $M_{14}, M_{11}$ and $M_{15}$, and $M_{12}$ and $M_{16}$ form current mirrors that reflect and amplify current from the input branches to the output branches. Cascode transistors $M_{17}-M_{20}$ increase the gain of the op amp by increasing the output resistance of the output nodes to ground. A high-swing dynamic bias circuit composed of transistors $M_{31}-M_{38}$ adjusts the gate bias on the cascode transistors so that the output branches can conduct large currents during slewing and have high swings during settling. Transistors $M_{41}-M_{44}$ together with the $C_{C M}$ capacitors and associated switches in Fig. 6(a), form the CMFB circuit. Because the gates of $M_{41}$ and $M_{42}$ are tied to a constant bias voltage, these transistors are constant-current sources. The gates of $M_{43}$ and $M_{44}$ are connected to the CMBIAS terminal shown in Fig. 6(a). This point is alternatively switched from a bias voltage on $\phi_{1}$ to a capacitively coupled version of the output on $\phi_{2}$. During $\phi_{2}$, the CMBIAS point rises and falls with changes in the com-mon-mode output voltage. This change adjusts the current drawn through $M_{43}$ and $M_{44}$ so that the common-mode output voltage is held constant near 0 V . Note that if the two halves of the differential circuit match perfectly,
changes in the differential output voltage do not change the CMBIAS point.

Because the speed of this op amp is limited by the speed of its current mirrors, wide-band current mirrors are used to increase the speed. To this end, transistors $M_{9}-M_{12}$ are not simply diode connected, but instead are buffered by source followers $M B_{1}-M B_{4}$. Because of this change, the currents needed to supply the parasitic capacitance between the gates and sources of the current mirrors at high frequencies come from the power supplies instead of from the input branch. The drawback to this approach is that the drain-to-source voltages of transistors $M_{9}-M_{12}$ are increased by the gate-to-source voltages of transistors $M B_{1}-M B_{4}$, respectively. Therefore, input stage transistors $M_{1}-M_{4}$ operate with less drain-to-source voltage than if $M_{9}-M_{12}$ were diode connected. As a result, $M_{1}-M_{4}$ enter the triode region for smaller differential inputs than with diode-connected loads, and the amount of current that the input stage can produce while slewing is limited. Because a high-swing dynamic bias circuit is used, this is not a problem for $\pm 5-\mathrm{V}$ operation; however, for $+5-\mathrm{V}$ operation, these wide-band current mirrors probably would limit the slew rate of the op amp.

A block diagram of an A/D, D/A subsection is shown in Fig. 8. To save area, one resistor string is shared for both the $\mathrm{A} / \mathrm{D}$ and $\mathrm{D} / \mathrm{A}$ functions. The resistor string divides the reference into equal segments and provides the boundaries between these segments as thresholds for a bank of comparators. The comparators are clocked at the end of $\phi_{2}$. On $\phi_{1}$, eight $D / A$ converter outputs are enabled and one is selected based on control signals generated from the comparator outputs ( $y_{1}, \cdots, y_{8}$ ). Although Fig. 8 shows a single-ended representation of both the


Fig. 8. Block diagram of $A / D, D / A$ subsection.


Fig. 9. Connection of comparator with $\mathrm{A} / \mathrm{D}, \mathrm{D} / \mathrm{A}$ subsection.
$\mathrm{A} / \mathrm{D}$ subconverter and $\mathrm{D} / \mathrm{A}$ converter functions, on the prototype, both functions are fully differential. Therefore, instead of just one D/A converter output, equal and opposite D/A converter outputs are used. Also, each comparator compares a differential input to a differential reference instead of a single-ended input to a single-ended reference.

The connection of a comparator within an $A / D, D / A$ subsection is shown in Fig. 9. The points labeled $V R+$ and $V R$ - are connected to taps on the resistor string that depend on which comparator in the bank is under consideration. For example, for the top comparator, $V R+$ is connected to the most positive $A / D$ subconverter tap, and $V R-$ is connected to the most negative $\mathrm{A} / \mathrm{D}$ subconverter tap. On clock $\phi_{1}$, the comparator inputs are grounded, and the capacitors sample the differential reference. On $\phi_{2}$, the left sides of the capacitors are connected to the differential input. Ignoring parasitic capacitance, the input to the comparator is then the difference between the differential input and the differential reference. The parasitic capacitances on the inputs to the comparator attenuate the input slightly, but the decision is not affected if the comparator has enough gain. As mentioned in Section III, because of digital correction, no offset cancellation on the comparator is required. Therefore, the comparator is never placed in a feedback loop and does not have to be stable in a closedloop configuration.

The comparator, shown in Fig. 10, uses a conventional latched-differential-amplifier configuration. Transistors $M_{1}$ and $M_{2}$ are source followers. Transistors $M_{3}-M_{8}$ form a


Fig. 10. Comparator schematic.


Fig. 11. DNL versus code.
differential amplifier, and $M L_{1}$ and $M L_{2}$ form a latch. Transistors $M C S_{1}$ and $M C S_{2}$ form a current switch that allows the bias current from $M B_{2}$ to flow through either the differential amplifier or the latch. With the latch signal low, the inputs are amplified. Because $M_{7}$ and $M_{8}$ are biased in the triode region, the gain of the amplifier is only about 20 dB . When the latch signal is raised, the bias current is switched from the amplifier to the latch. During the transition, the parasitic capacitances on the inputs to the latch hold the amplified input. Finally, the latch switches, and the comparison is completed.

## V. Experimental Results

As mentioned in Section IV, the digital correction is done off chip. This allows tests to be run to evaluate the need for the correction. Unless stated otherwise, all results are obtained using the full correction; that is, digital correction is applied to the first three stages. The prototype has been tested primarily in two ways [23], [24]: first with a code density test, and second with a signal-to-noise ratio (SNR) test. Both tests have used high- and lowfrequency input signals. Results of the code density test are shown in Figs. 11 and 12.

In Fig. 11, differential nonlinearity (DNL) is plotted on the $y$ axis versus code on the $x$ axis for all 512 codes. The conversion rate is $5 \mathrm{Msample} / \mathrm{s}$, and the input frequency is 2 MHz . Because the DNL never goes down to -1 LSB ,


Fig. 12. INL versus code.


Fig. 13. SNR versus input level.
there are no missing codes. The maximum DNL is less than 0.6 LSB.

In Fig. 12, integral nonlinearity (INL) is plotted on the $y$ axis versus code on the $x$ axis. Again, the conversion rate is $5 \mathrm{Msample} / \mathrm{s}$ and the input frequency is 2 MHz . The maximum INL is 1.1 LSB. The nonideality in the curve is caused by both nonlinearity in the first-stage D/A converter and incomplete settling of the first-stage op-amp output.

Under the same conditions as in Figs. 11 and 12 but with the digital correction completely disabled, the maximum DNL and INL are about 10 LSB at a 9-bit level, owing to comparator offsets. If the correction is applied only on the first stage, the maximum DNL and INL drop to about 3 LSB. When digital correction is applied on the first two stages, the maximum DNL is about 0.9 LSB and the maximum INL is about 1.5 LSB; therefore, there are no missing codes in this case. Also, the uncorrected histogram data from the code density test show that there are no codes for which any residue is greater than the reference level for comparator $C_{1}$ or less than the reference level for comparator $C_{7}$ as labeled in Fig. 8. This means that the maximum absolute value of nonlinearity in an A/D subconversion is less than or equal to $1 / 4 \mathrm{LSB}$ at a 3-bit level, and the full digital correction range ( $\pm 1 / 2$ LSB) is not used. Therefore, comparators $C_{1}$ and $C_{7}$ are not needed in the last three stages.

SNR measurements were made by taking fast Fourier transforms on 1024 samples from the A/D converter at the downsampled rate of 20 kHz while the converter was running at 5 Msample/s. In Fig. 13, SNR is plotted on the $y$ axis versus input level on the $x$ axis for five input

TABLE I
Data Summary over Input Frequency Variation 9-bit Resolution; 5-Msample/s Conversion

Rate; $\pm 5-\mathrm{V}$ Power Supplies

| Input Frequency | 2 kHz | 2 MHz | 5.002 MHz |
| :---: | :---: | :---: | :---: |
| Peak DNL (LSB) | 0.5 | 0.6 | 0.5 |
| Peak INL (LSB) | 1.0 | 1.1 | 1.2 |
| Peak SNR (dB) | 50 | 50 | 49 |

frequencies: $2 \mathrm{kHz}, 22 \mathrm{kHz}, 202 \mathrm{kHz}, 2.002 \mathrm{MHz}$, and 5.002 MHz . The curve for 5.002 MHz represents a beat frequency test on the converter when compared to the curve for 2 kHz because the converter is running at the difference between these two frequencies or $5 \mathrm{Msample} / \mathrm{s}$. An ideal 9-bit curve is also shown. The peak SNR is around 50 dB instead of 56 dB , as would be expected with a 9 -bit converter; this difference is accounted for by distortion generated from the INL for large input signals. When the input signal is reduced in amplitude, the distortion is reduced and the real curves approach the ideal 9 -bit curve. Note that there is little difference in the curves for different input frequencies, showing that the first-stage S/H amplifier is able to accurately sample high-frequency input signals.

The results of the code density and SNR tests for variations in the input frequency are summarized in Table I. Peak DNL, INL, and SNR are shown for three input frequencies, and the performance is almost constant. This is important because it shows that the first-stage $\mathrm{S} / \mathrm{H}$ amplifier is able to accurately sample high-frequency input signals.
A photograph of the core of a prototype chip is shown in Fig. 14. The core is about 50 mil high by 150 mil wide. The stages follow one after another and are identical except that the fourth stage does not have a D/A converter or a subtractor and the two-phase nonoverlapping clock alternates from stage to stage. A test op amp and a test comparator are at the end. The prototype was made by MOSIS in a $3-\mu \mathrm{m}$, double-polysilicon, p -well, CMOS process.

## VI. Summary

This paper reports on a prototype pipelined A/D converter with typical characteristics summarized in Table II. In summary, the prototype demonstrates that pipelined architectures and digital correction techniques are of potential interest for high-speed CMOS A/D conversion applications.

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Fig. 14. Photograph of the core of the prototype.

TABLE II
Typical Performance: $25^{\circ} \mathrm{C}$

| Technology | 3-u CMOS |
| :--- | :--- |
| Resolution | 9 bits |
| Conversion Rate | $5 \mathrm{Ms} / \mathrm{s}$ |
| Area $^{*}$ | 8500 mils $^{2}$ |
| Power Supplies | $\pm 5 \mathrm{~V}$ |
| Power Dissipation | 180 mW |
| Input Capacitance | 3 pF |
| Input Offset | $<1 \mathrm{LSB}$ |
| CM Input Range | $\pm 5 \mathrm{~V}$ |
| DC PSRR | 50 dB |

*Does not include clock generator, bias generator, reference generator, digital error correction logic, and pads.

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