DESIGN PROJECT EE4303
Spring 2002

I. Project Description

You are to design a single-ended operational amplifier to be used in a switched capacitor gain stage. The schematic of the switched capacitor circuit is shown in figure 1.

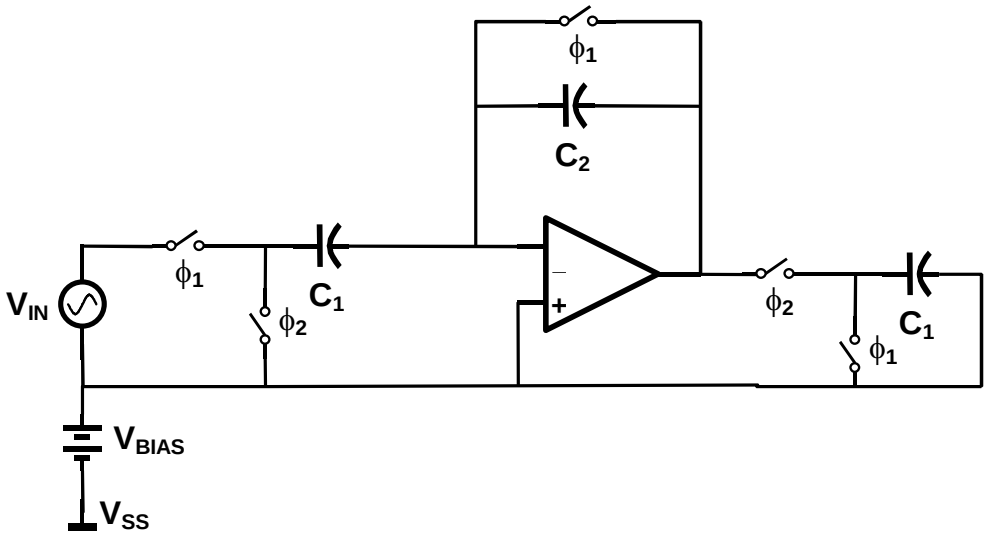

Figure 1: A switched capacitor gain stage. ϕ_1 and ϕ_2 are non overlapping clocks.

The key goal in the design is to minimize the power consumption while maintaining the necessary performance. The following table summarizes the necessary performance:

C_1	1	pF
$C_2 = C_1/2$	0.5	pF
V_{DD}	2.5	V
V_{SS}	0	V
V_{BIAS}	**Your choice**	
Input Voltage Range	$-0.3 < V_{IN} < 0.3$	V
DC Gain Opamp	> 60	dB
Systematic offset voltage (optional)	< 0.5	mV
Settling accuracy	Better than 0.1%	
Settling time	< 20	nsec

Table 1: Requirements

You need to design an operational amplifier that meets these specifications, including its bias circuit. You can assume that you have one ideal reference current of your choice available.

Operation of the circuit:

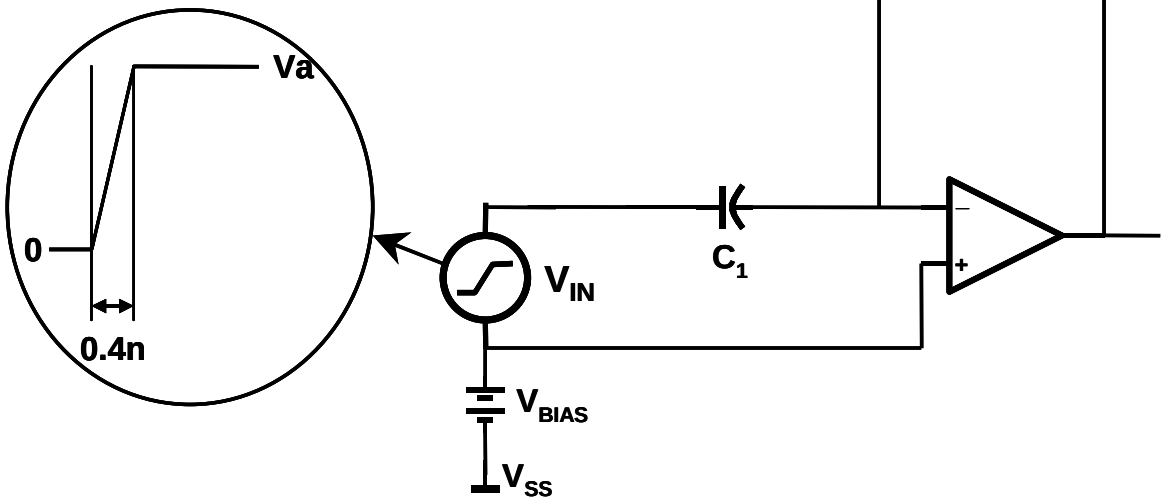

Figure 2: Equivalent schematic during clock phase 1. The initial charge on C_1 needs to be 0.

Figure 2 shows the equivalent circuit configuration during clock phase ϕ_1 for a dc input voltage of Va. For simplification the operation of the clock switches is mimicked by using a step input voltage source with a rise time of 0.4nSec. After settling capacitor C_1 will be charge to a voltage Va.
Figure 3 shows the equivalent circuit that can be used to simulate the operation during phase ϕ_2 . The charge on C_1 from ϕ_1 is conserved by setting the initial condition of the capacitor to Va. The other capacitors have an initial charge of zero.

IMPORTANT: You need to make sure that in both clock phases the specifications of table 1 are met. You need to verify the settling time for small inputs (+10mV & -10mV) **and** large inputs (+300mV & –300mV).

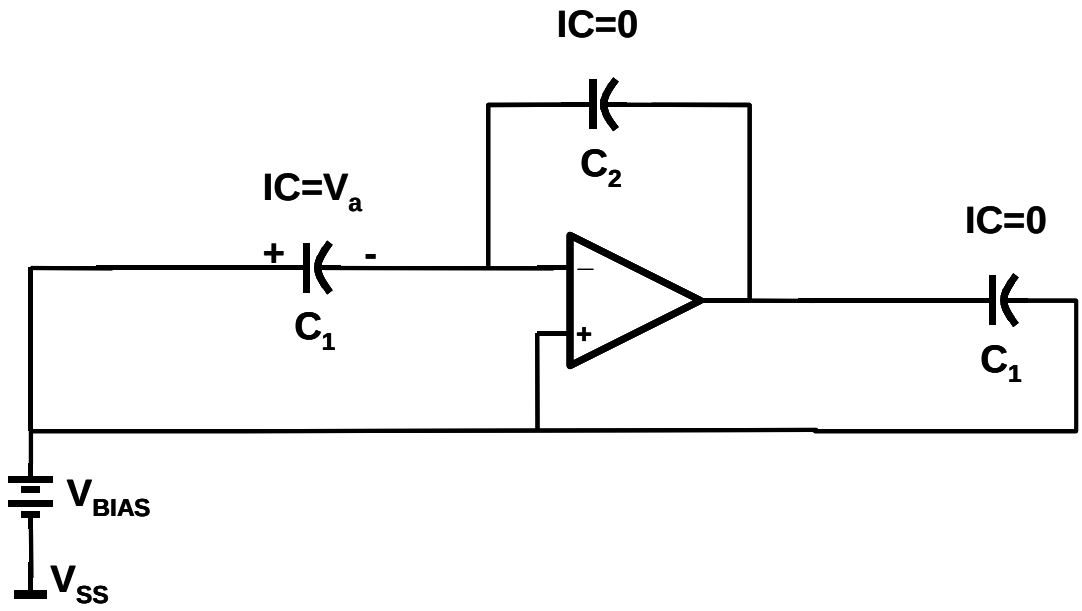

Figure 3: Equivalent schematic to simulate operation during clock phase 2. The initial conditions for the different capacitors are indicated.

II. What do you submit in your report

You need to write a clear but concise report describing your design. The report needs to be typed and should not be longer than 7 pages using a 12pt font (appendices not included). The report needs to contain the following sections:

1. *Schematic of the final amplifier + motivation for the choice of topology*

Draw a clean schematic of your final amplifier. Clearly indicate the nominal current through each branch and the width and length of each device. Uniquely name each device and node and refer to these names in the remainder of this report.

Briefly motivate your choice of topology and convince the reader that this is the best topology for the given application and requirements. Discuss possible alternatives and their advantages or disadvantages.

2. *Sizing of the devices*

Describe the flow of decisions and calculations to size the transistors to meet the performance requirements. Make your description such that the reader can resize the circuit for different performance requirements. Explain how you minimized the power consumption of your circuit. Document your hand calculations of the transistor size

estimates and indicate how you further optimized them using the circuit simulator. If you change your hand-calculated transistor sizes using the simulator, motivate why you need to make these changes.

3. Simulation Results illustrating each of the requirements

For each requirement submit a schematic of the simulation you did to verify the performance. If your simulator input is text-based, submit the input file but also draw a schematic with the same naming conventions.

Submit a graph showing the simulation results. Annotate the graph clearly and include zoom-ins to illustrate important details.

Include a summary table in your report with the important specifications of your design and the attained simulation results.

4. Appendices

Keep the main report concise, but feel free to add additional relevant information or results in appendices.

III. Simulation Tools

Use the cadence CAD environment that is available in the computer lab.

IV. Process Parameters

You have to design your amplifier in TSMC 0.25um CMOS technology that is set up in the cadence CAD environment in the lab.

V. Group Work

You can complete this assignment individually or work in groups of maximum two students and submit a joint report.

VI. Grading

Your grade will depend on the following criteria:

- Report: deliver a clear, concise but complete report. If you wish to submit supplemental data, schematics or calculations add appendices to your report. Consider your report as a flyer that goes out to a customer and try to convince her or him that your design will be the best for the job.
- Design: is the choice of topology and the sizing well motivated and suited for the requirements. Has a careful design been done? Will the design work in a practical simulation?
- Simulations: have all the performance requirements been carefully and correctly simulated and have the results been clearly reported.
- Performance: have all the performance requirements been met. If not, has been investigated why not and how the design can be improved. A ranking according to power

consumption will be made of all the submitted designs that meet specifications. This ranking will influence the final grade.

VII. Questions, Updates and Guidance

Questions regarding the interpretation of specifications will probably arise. This is a very typical situation for any circuit design task. You can always consult the staff with your questions. Or, try to use your own judgment to come up with a resolution and explain your choices in your report. Also check the class webpage for updates.

Advice: a circuit design is a pretty involved task. It will most probably require you a couple of iterations on the topology and sizing to get to the solution. It will also take you some time to get used to the specific CMOS technology and circuit simulator. You probably want to experiment with a few simple transistor configurations before tackling the more complicated circuits. Do not postpone starting on the project till just before the deadline !!!!
Good Luck.

-- Peter Kinget (April 2002)