MO2B-2

A Simplified CMOS FET Model using Surface Potential Equations For Inter-modulation Simulations of Passive-Mixer-Like Circuits

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Outline

- Motivation and Prior Art
- Simplified Surface Potential Model
- Short-Channel Effects
- Simulation and Measurement Results
- Conclusion

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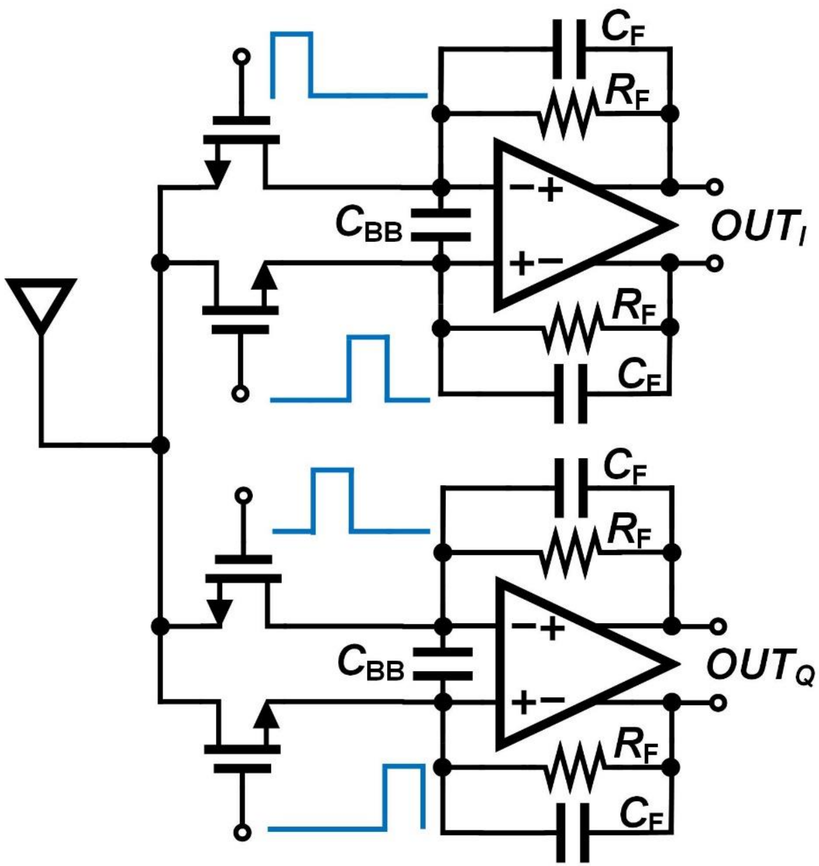
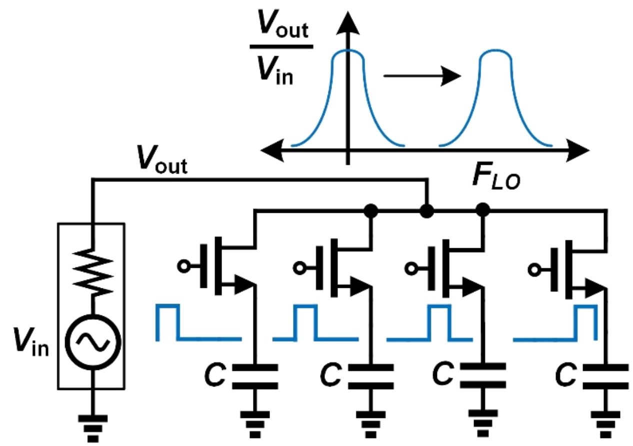
Circuits That Use FETs As Switches

Passive-Mixers and
Mixer-First Receivers



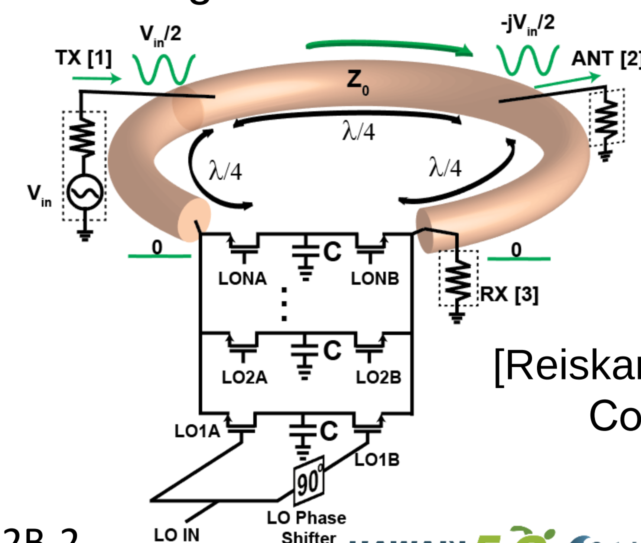
[Andrews JSSC'10]

N-Path Filters



[Ghaffari JSSC'13]

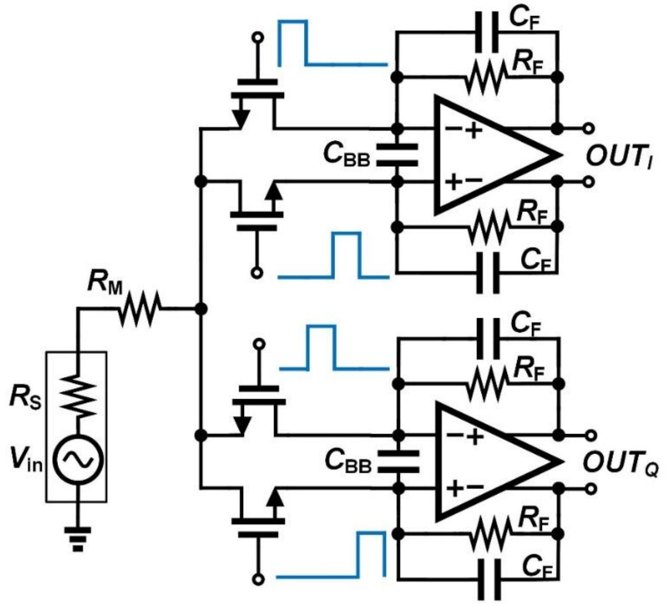
Integrated Circulators

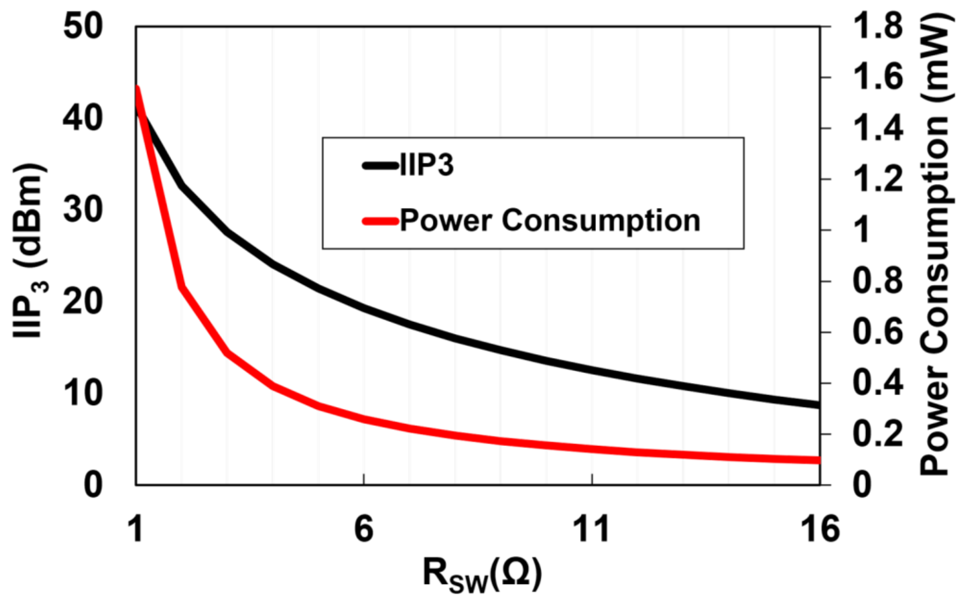


[Reiskarimian Nature Comm.'16]

Mixer-First Receiver Design Challenges

- Increasing switch FETs size improves linearity at the cost of power consumption.
- Increasing series resistance R_M improves linearity at the cost of NF.

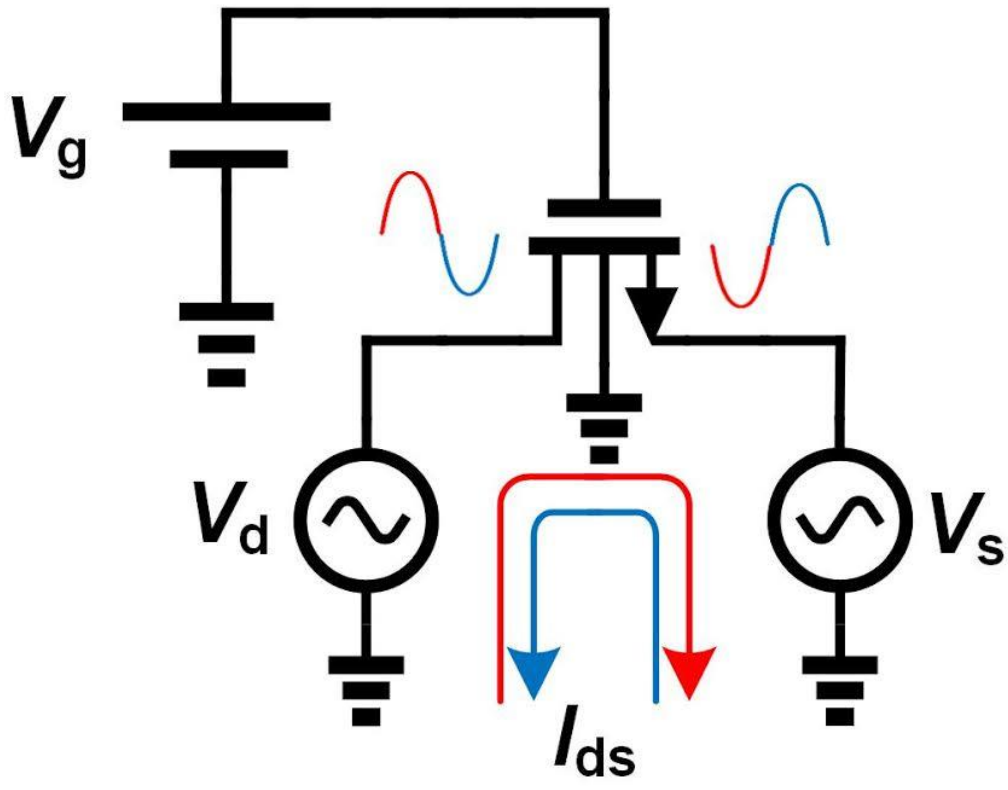




Out-of-band IIP_3 is calculated using [Yang TCASI'15]. Power consumption is calculated for an operating frequency of 1GHz.

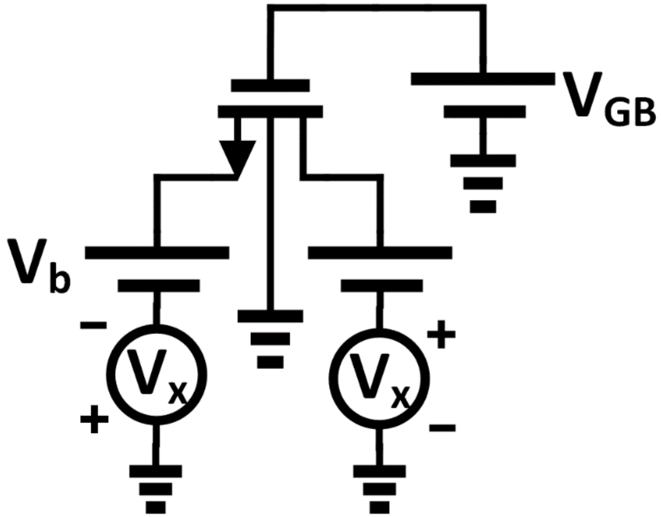
Linearity simulations are critical during the design phase for the optimization of passive mixer-like circuits.

FET Operation As a Switch

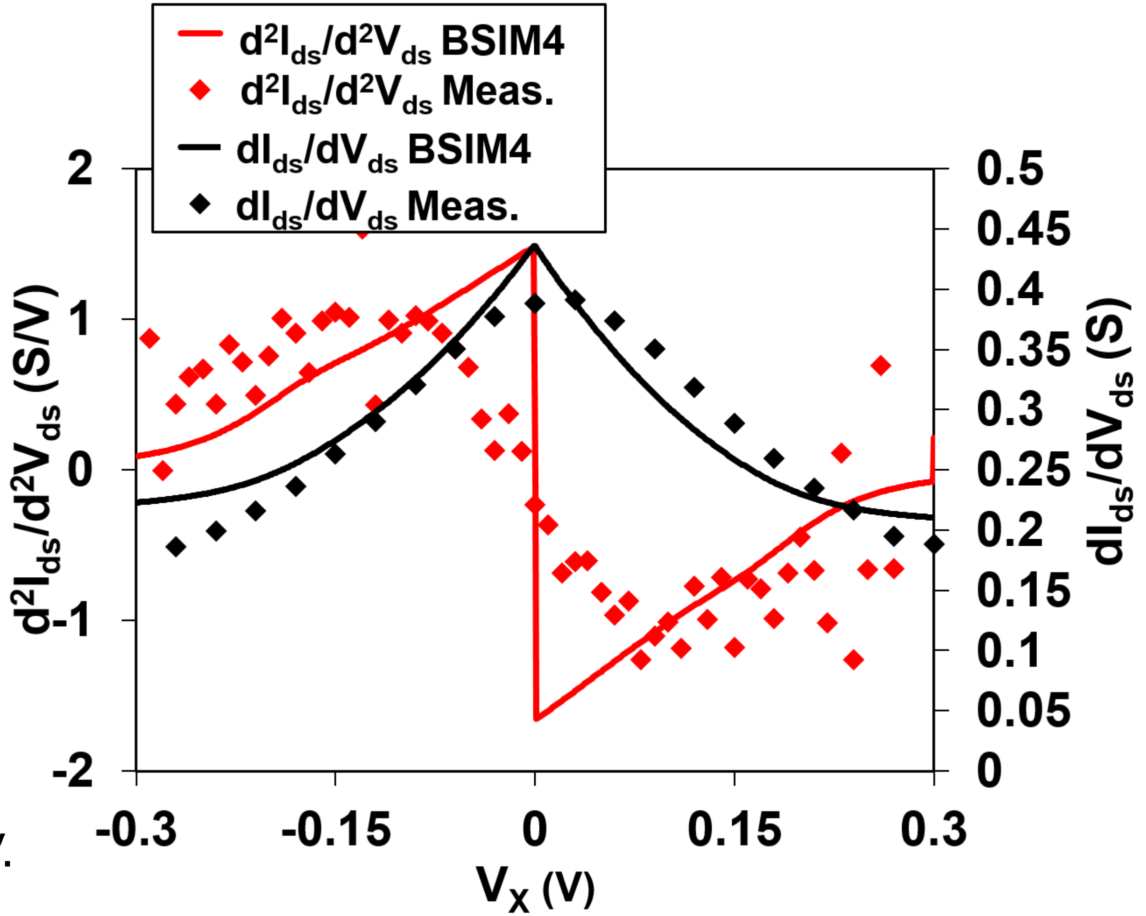


MOSFET switches are symmetric devices and typically experience source-drain reversal during AC operation.

Gummel Symmetry Test In BSIM4

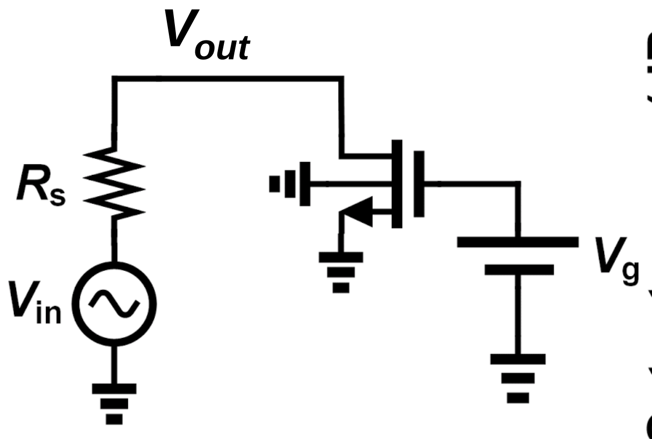


- 65nm CMOS;
- FET size: $\frac{96\mu m}{65nm}$;
- V_{GB} = 1.2V and V_b=0.3V.



In BSIM4 models, the 2nd derivative of I_{DS} shows discontinuity around V_{DS}=0.

Two-Tone Test Using BSIM4 Model



- 65nm CMOS;
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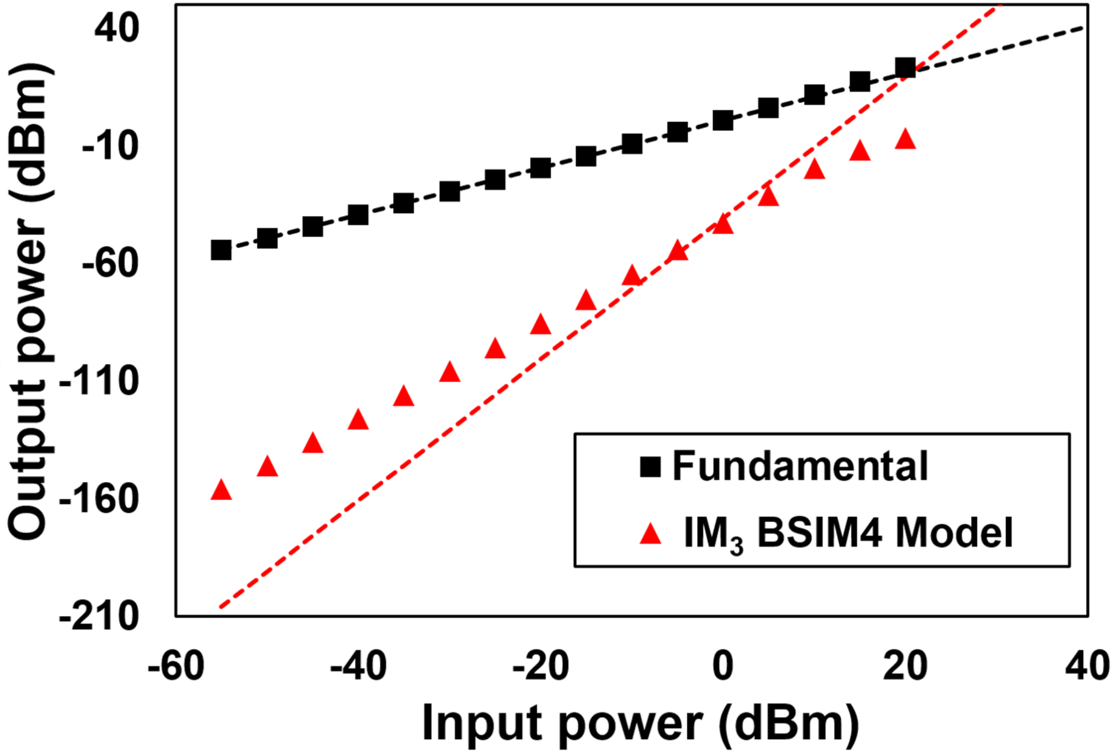


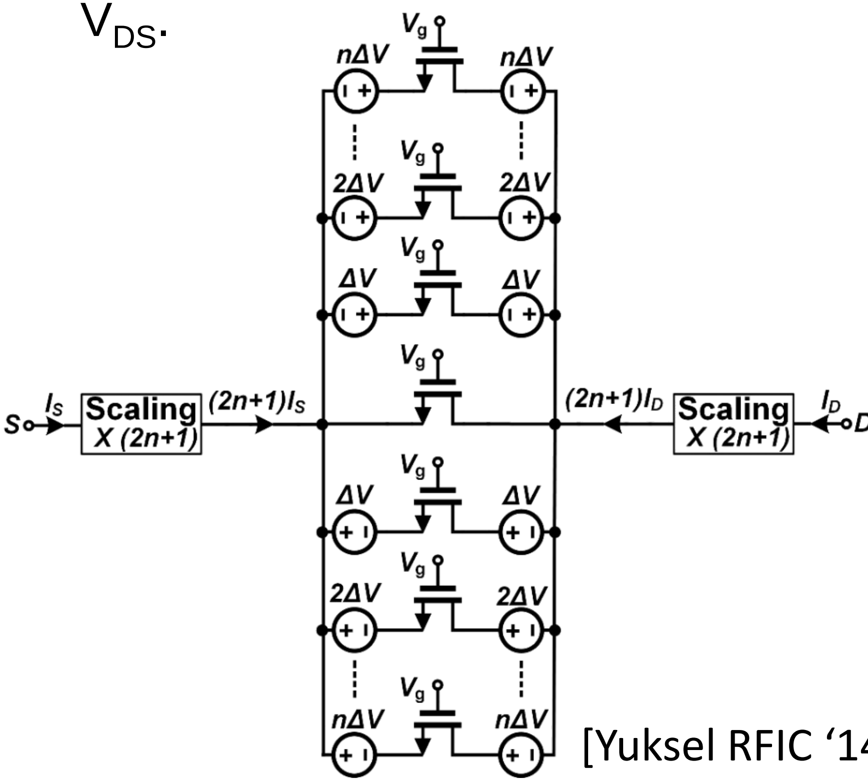
The IM_3 predicted by BSIM4 models shows unphysical characteristics (slope of 2dB/dB).

Transistor Models Comparison

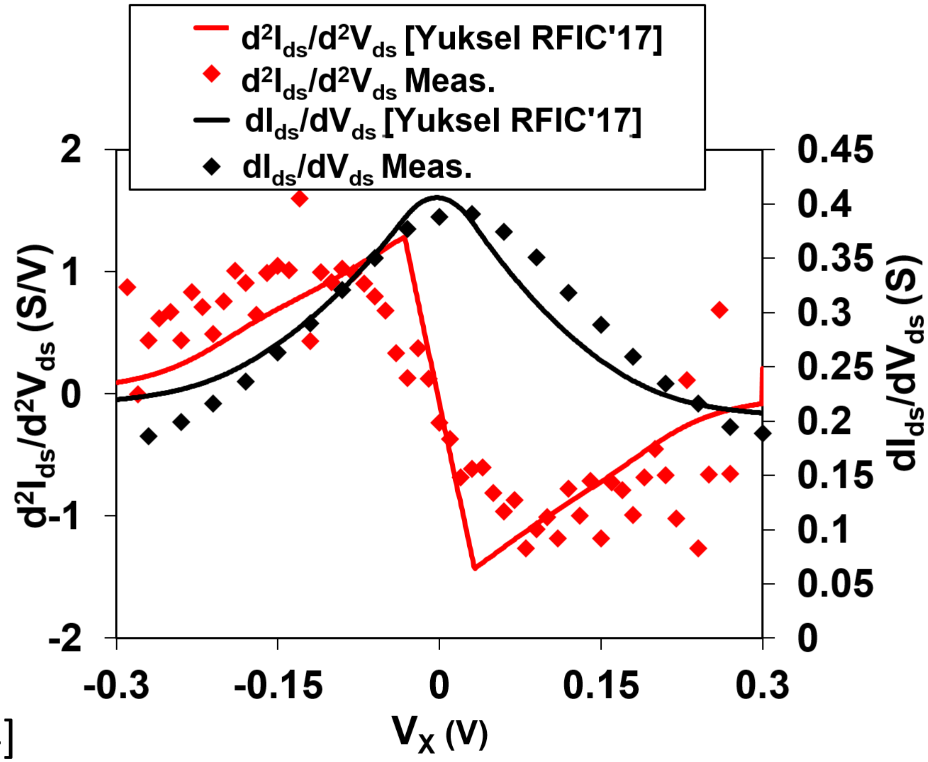
Source-referenced models E.g. BSIM	Body-referenced models E.g. PSP
✓ Physical driving forces are V_{GS} and V_{DS} . ✓ V_T appears in the equations. ✓ Velocity saturation is easy to handle. × Asymmetric around the source-drain reversal point.	✓ Symmetry is appealing. ✓ Effective mobility is well handled. ✓ It is easy to make the drain current continuous at V_{DS}=0. × Not provided by most digitally-driven foundries.

Prior Work

- Break the transistor into 2n+1 transistors in parallel with small offset voltages in V_{DS}.



[Yuksel RFIC '14]



- ✗ **High processing load (if n=32, 1 FET is replaced by 65 FET).**
- ✗ **Predicts 3dB/dB for IM_3 only for $\Delta V < V_{DS} < n\Delta V$.**
- ✗ **Need measurements to extract value of ΔV.**

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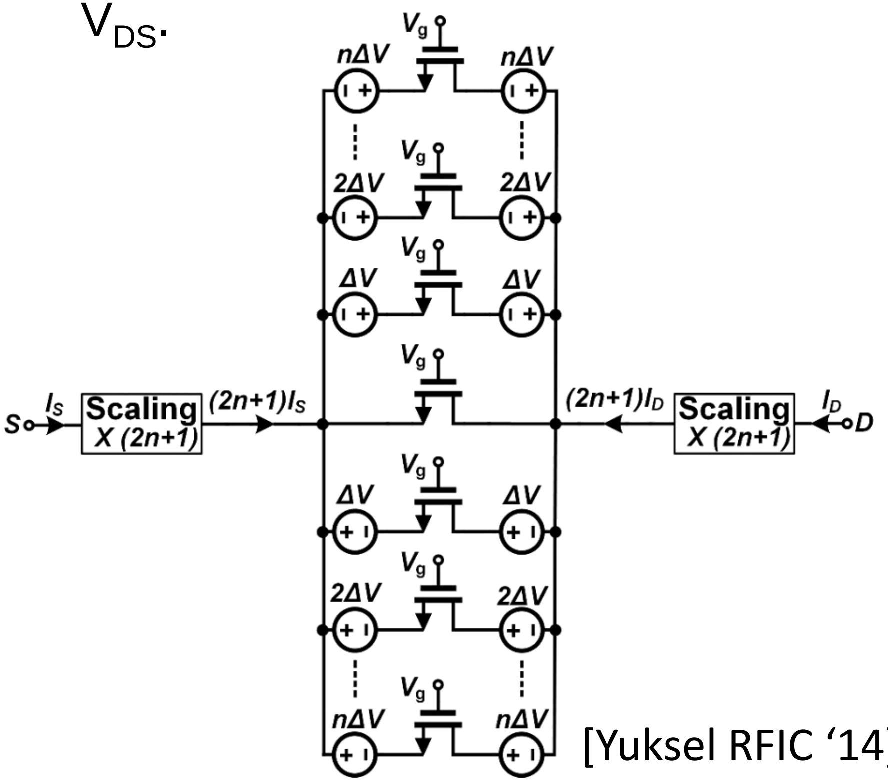

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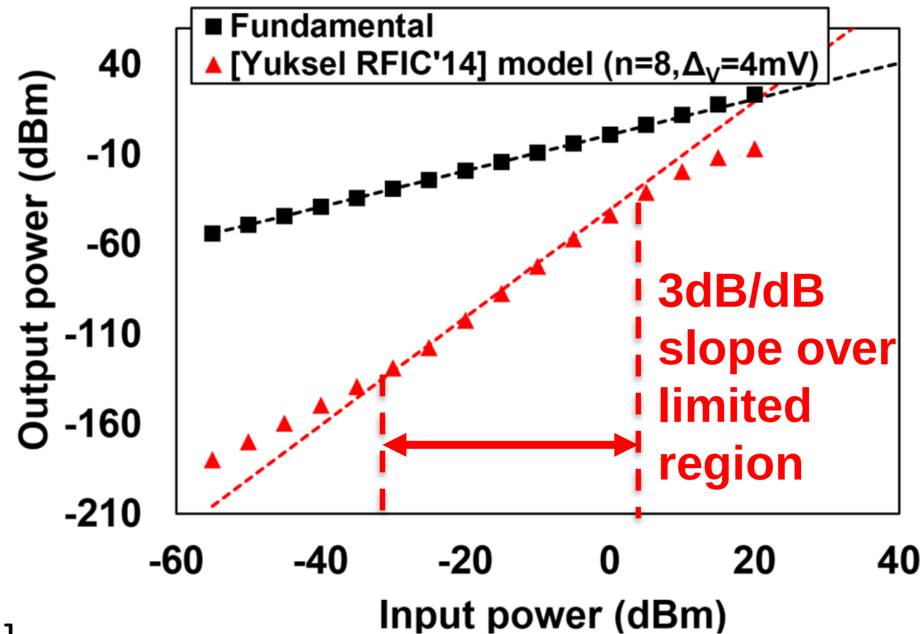

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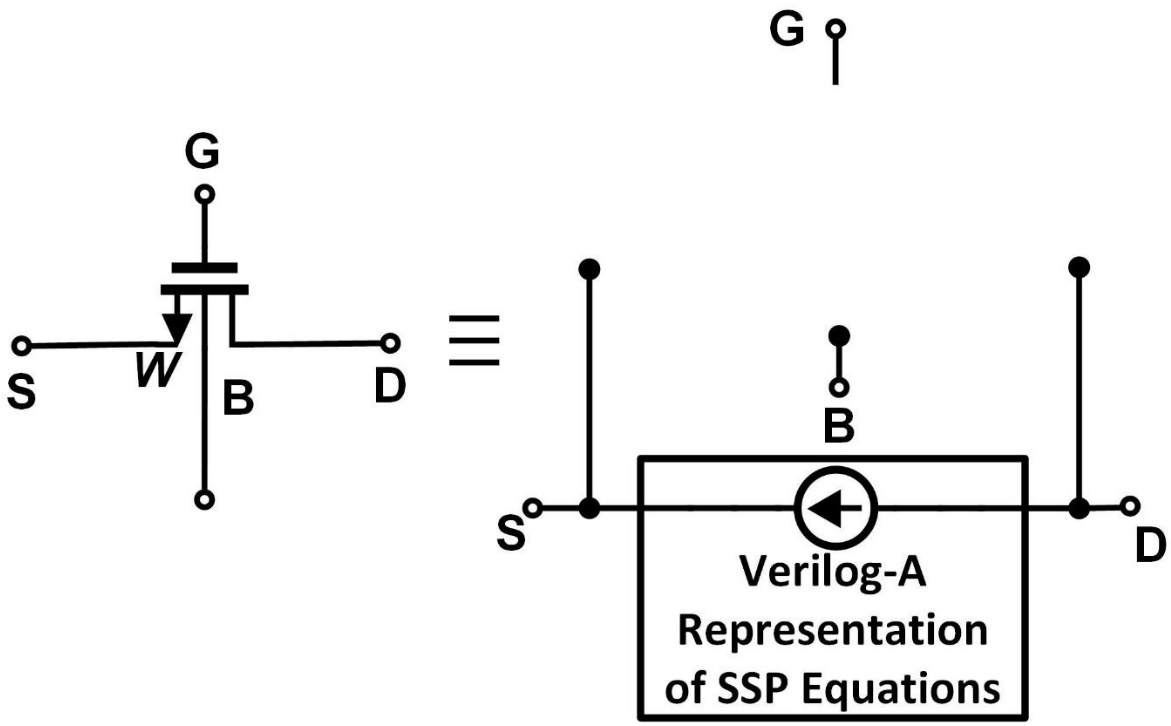
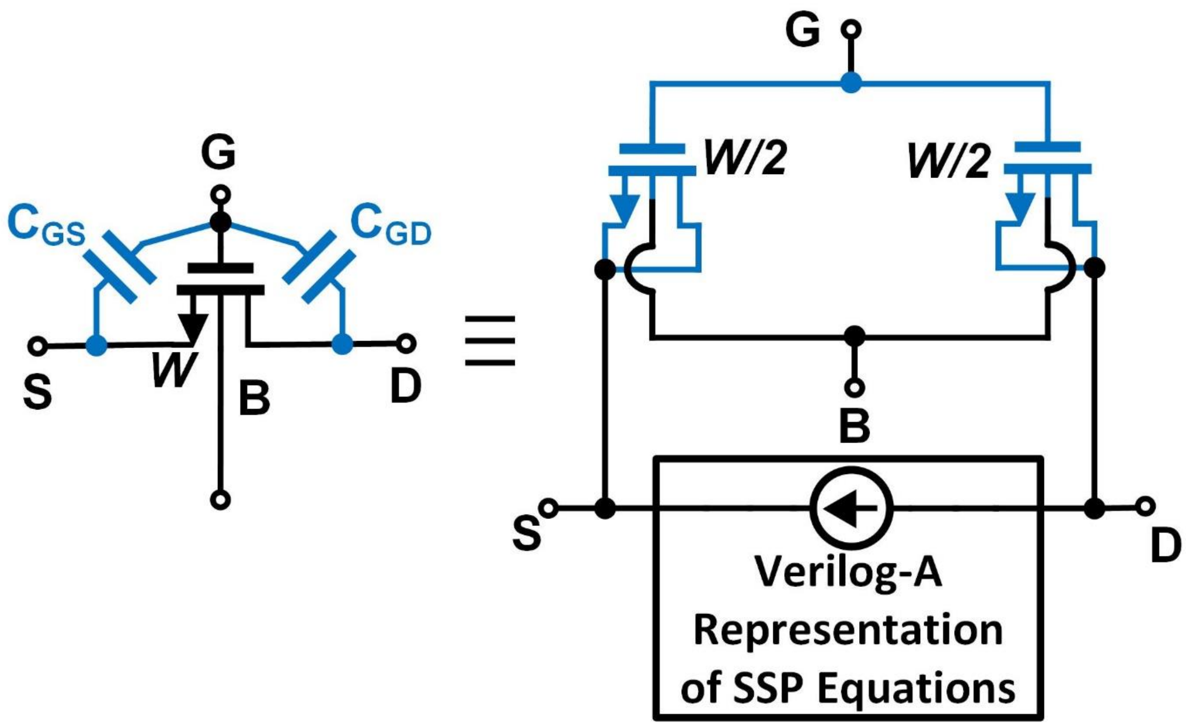
Simplified Surface Potential Model

- Simple Verilog-A code is employed to define the I_{DS} based on FET terminal voltages using simplified surface potential (SSP) equations.



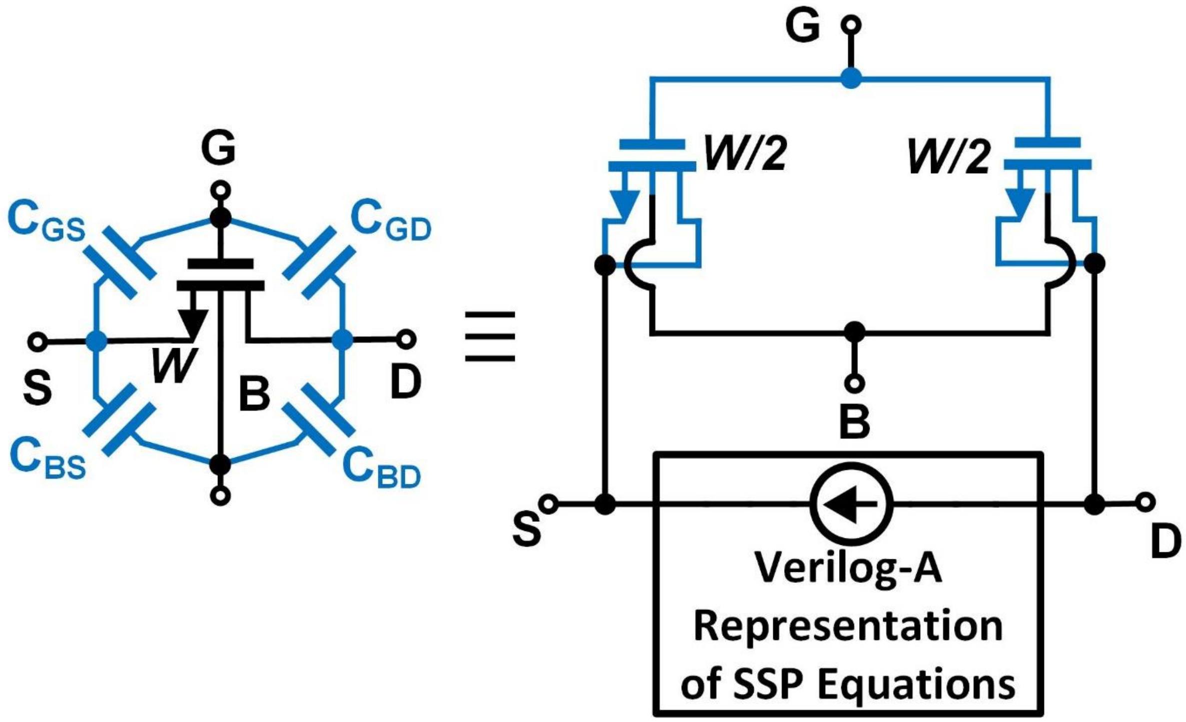
Simplified Surface Potential Model

- Foundry provided model is used to take into account the 2nd order parasitics
  - Gate-source and gate-drain capacitance.



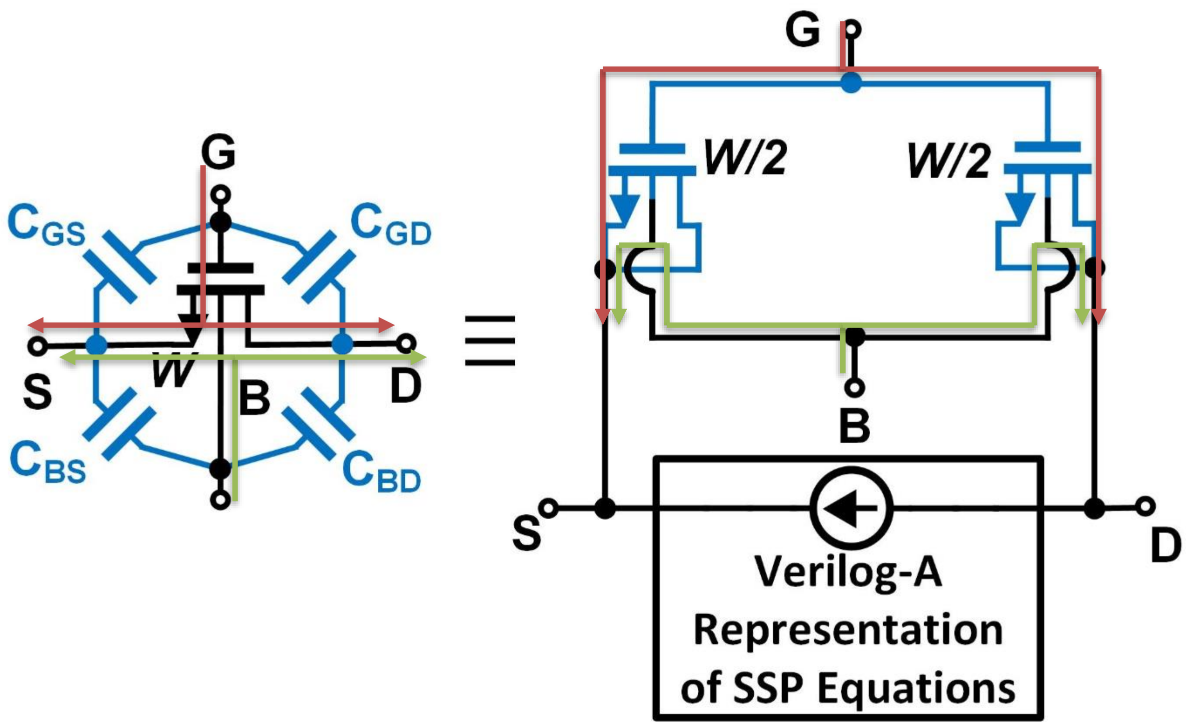
Simplified Surface Potential Model

- Foundry provided model is used to take into account the 2nd order parasitics
  - Body-source and body-drain capacitance.



Simplified Surface Potential Model

- Foundry provided model is used to take into account the 2nd order parasitics
  - Gate and body leakage currents.

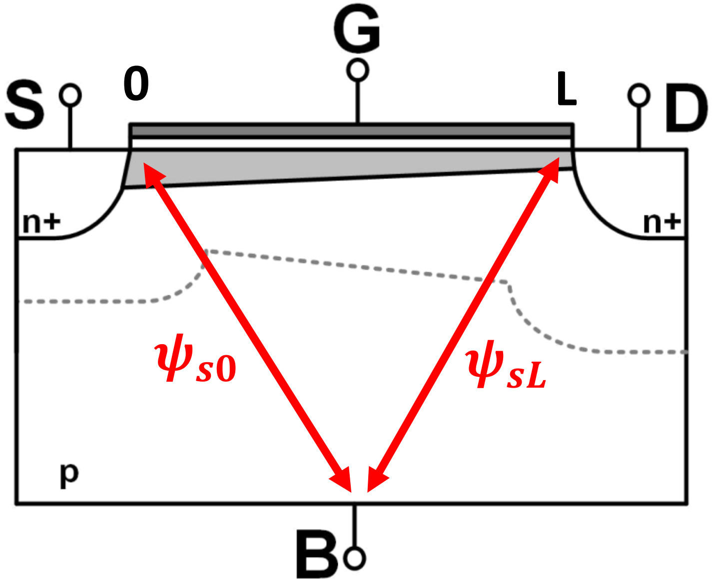


Surface Potential Equations

- Surface potential at source and drain ends can be described by*:

$$\psi_{s0} = V_{GB} - V_{FB} - \gamma\sqrt{\psi_{s0} + \phi_t e^{(\psi_{s0} - 2\phi_F - V_{SB})/\phi_t}}$$

$$\psi_{sL} = V_{GB} - V_{FB} - \gamma\sqrt{\psi_{sL} + \phi_t e^{(\psi_{sL} - 2\phi_F - V_{DB})/\phi_t}}$$

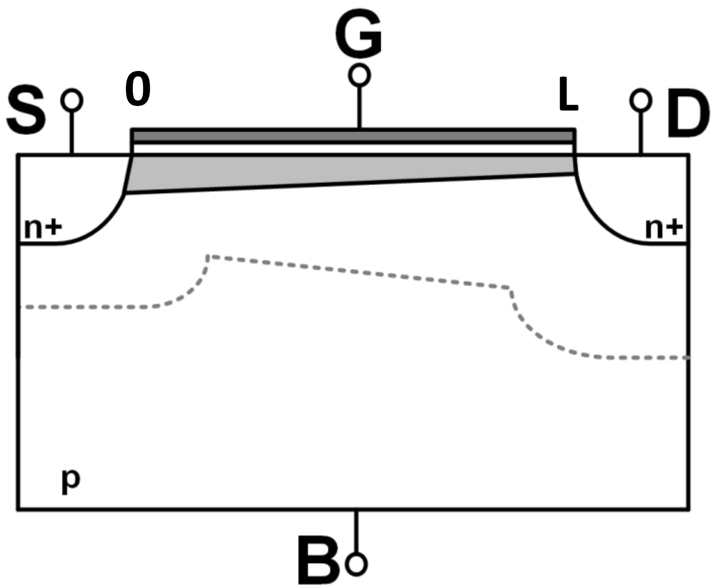


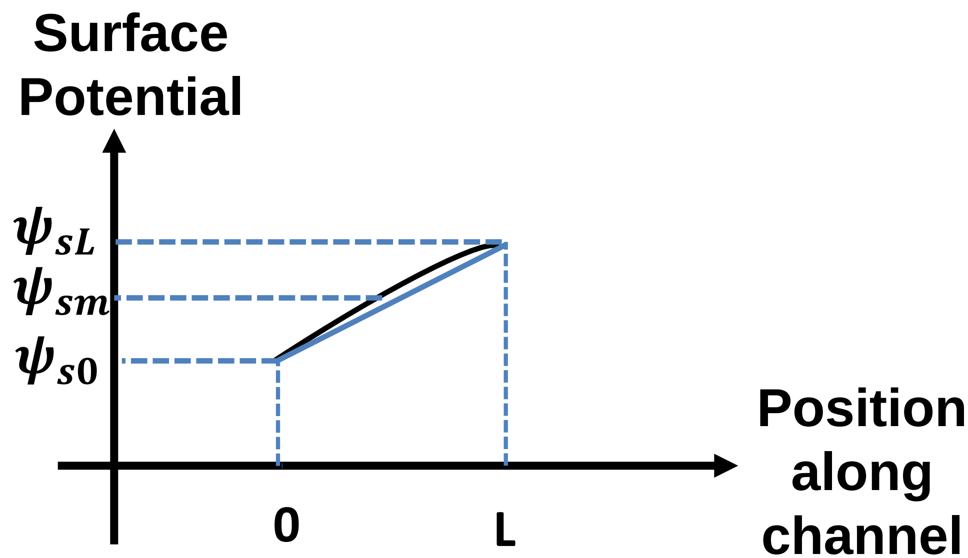
V_{FB}: Flat-band voltage
γ: Body coefficient
ϕ_F: Fermi voltage
ϕ_t: Thermal voltage

* Y. Tsividis and C. McAndrew, Operation and Modeling of the MOS Transistor. Oxford Univ. Press, 2011.

Surface Potential Along The Channel

- Surface Potential along the channel can be approximated linearly.





$$\psi_{sm} = \frac{\psi_{s0} + \psi_{sL}}{2}$$

Drain-Source Current Equation

- The drain-source current is a combination of drift and diffusion currents and can be approximated by*:

$$I_{DS,total} = I_{DS,drift} + I_{DS,diff.}$$

$$-I_{DS,drift} = \frac{W}{L}\mu C_{ox}(V_{GB} - V_{FB} - \psi_{sm} - \gamma\sqrt{\psi_{sm}})(\psi_{sL} - \psi_{s0})$$

$$-I_{DS,diff.} = \frac{W}{L}\mu C_{ox}\alpha_m\phi_t\,(\psi_{sL} - \psi_{s0})$$

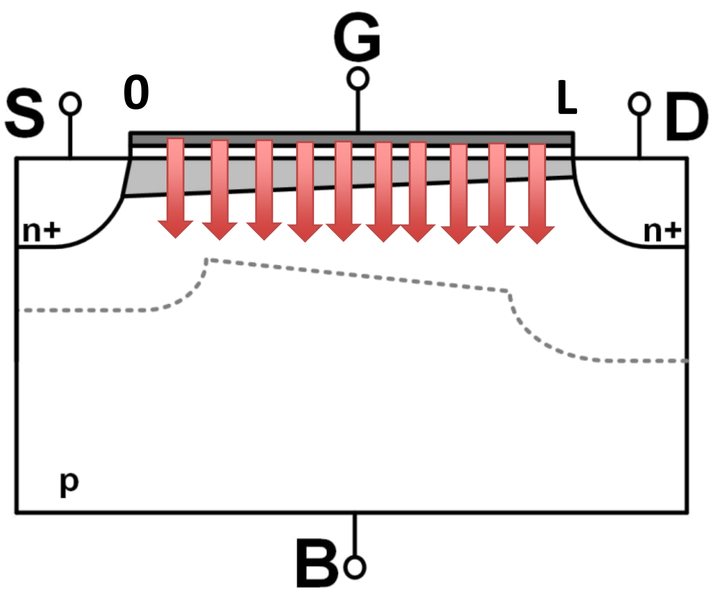
$$\alpha_m = 1 + \frac{\gamma}{2\sqrt{\psi_{sm}}}$$

W: Width
L: Length
μ: Mobility of electron
V_{FB}: Flat-band voltage
γ: Body coefficient
φ_F: Fermi voltage

Completely symmetric at V_{DS}=0.

Effective Mobility

- The mobility of electrons is reduced by the transverse field in the channel*.



$$\mu_{eff} = \frac{\mu_0}{1 - \frac{a_0}{\epsilon_s}\left(\overline{Q'_B} + \eta_E \overline{Q'_I}\right)}$$

$$\overline{Q'_B} = -C_{ox}\gamma\sqrt{\psi_{sm}}$$

$$\overline{Q'_I} = -C_{ox}(V_{GB} - V_{FB} - \psi_{sm}) - \overline{Q'_B}$$

μ_0, a_0 and η_E can be treated as curve fitting parameters.

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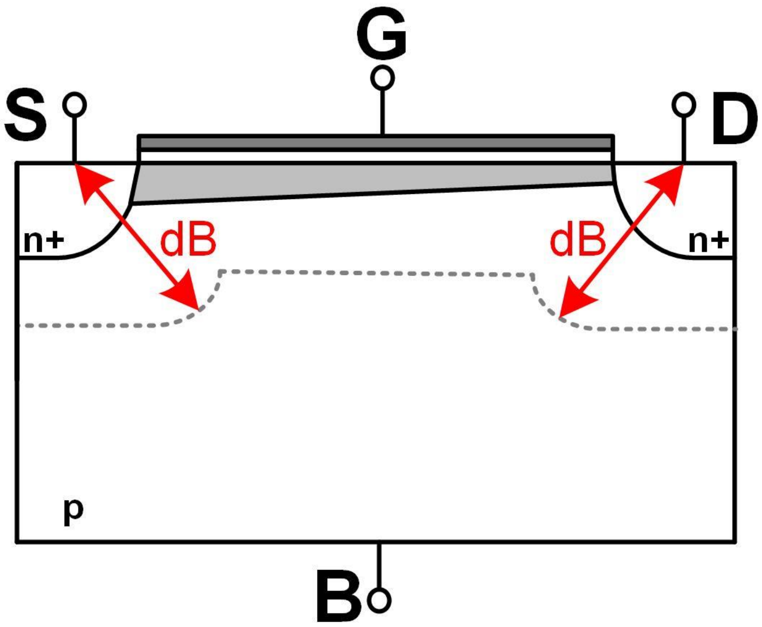
Charge Sharing

- The extension of the drain and source depletion charge into the channel reduces the gate control over the channel charge.



$$\gamma_1 = \gamma \frac{\widehat{Q_B}}{Q_B}$$

$$\frac{\widehat{Q_B}}{Q_B} = 1 - \frac{d_j}{L}\left(-1 + \sqrt{1 + 2\frac{dB}{d_j}}\right)$$

Depletion region is not necessarily same around the source and drain.

Charge Sharing

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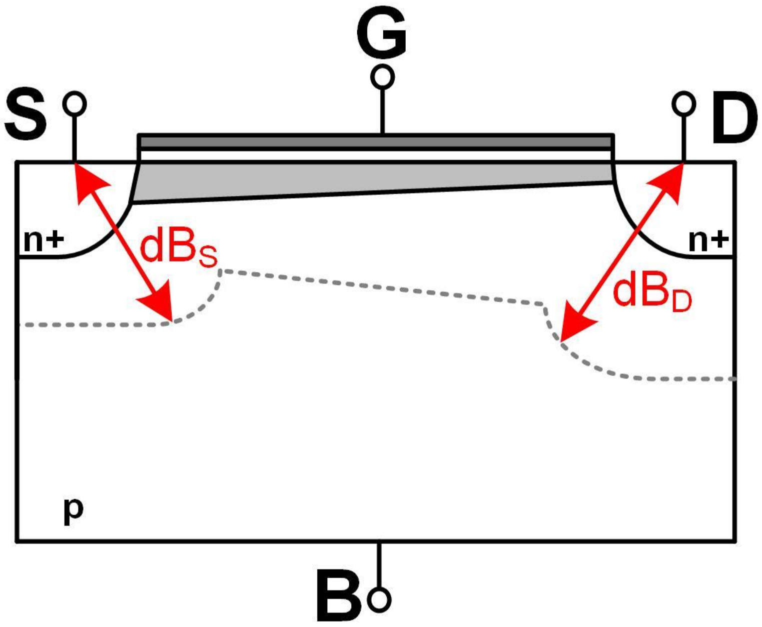


$$\gamma_1 = \gamma \frac{\widehat{Q_B}}{Q_B}$$

$$\frac{\widehat{Q_B}}{Q_B} = 1 - \frac{\Delta_S}{L}\left(1 - \frac{dB_S}{2dB}\right) - \frac{\Delta_D}{L}\left(1 - \frac{dB_D}{2dB}\right)$$

$$\Delta_{S/D} = d_j\left(-1 + \sqrt{1 + 2\frac{dB_{S/D}}{d_j}}\right)$$

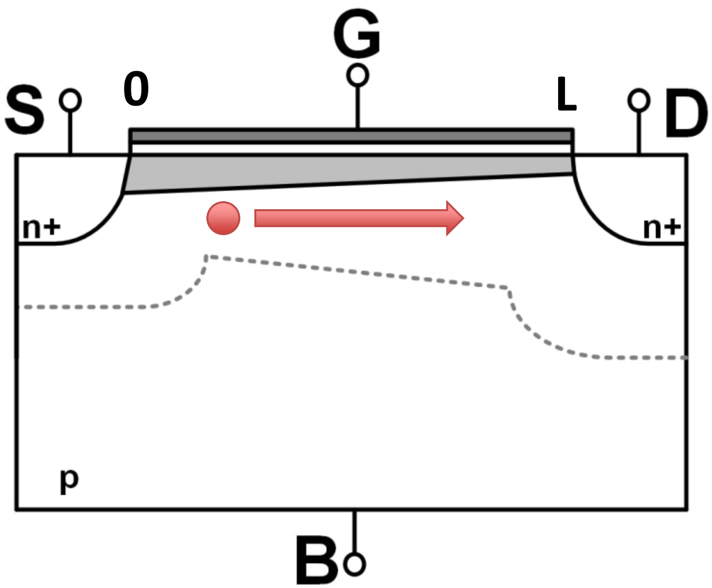
$$dB = \frac{dB_S + dB_D}{2}$$

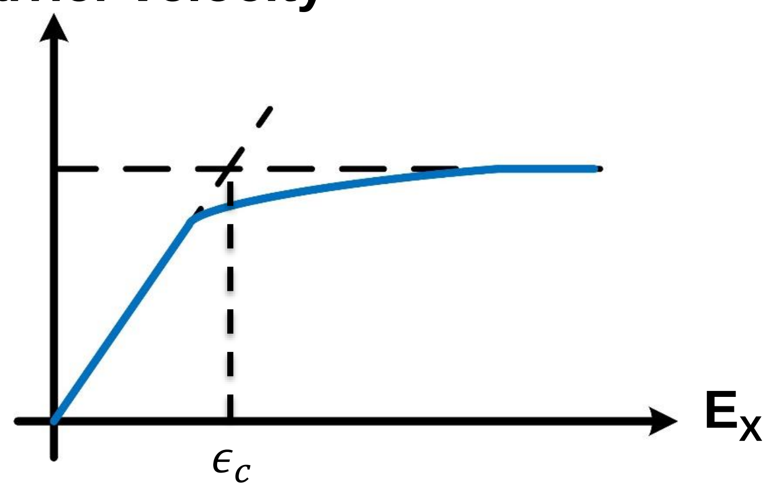
d_j: Junction depth

Completely symmetric at V_{DS}=0.

Velocity Saturation

- Velocity of carriers can saturate even with device operating in triode.





$$-I_{DS,w\ Velocity\ Saturation} \neq \frac{-I_{DS,w/o\ Velocity\ Saturation}}{1 + \frac{-V_{DS}}{L\epsilon_c}}$$

Second order derivatives are discontinuous.

Velocity Saturation

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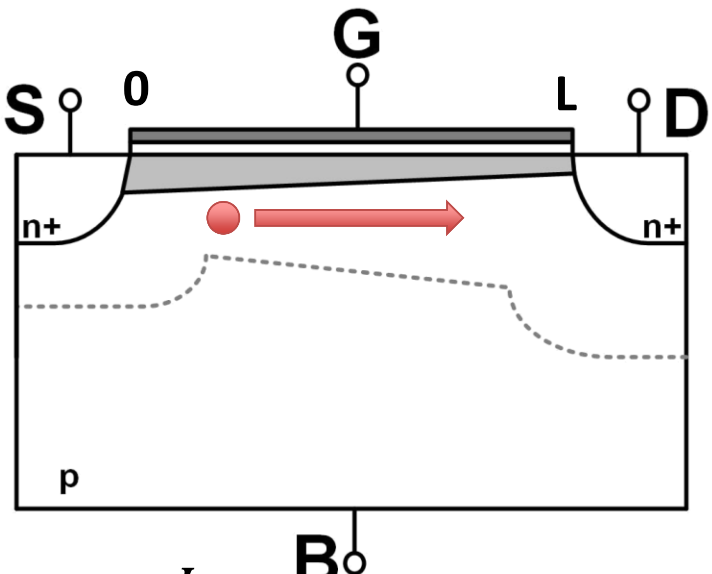
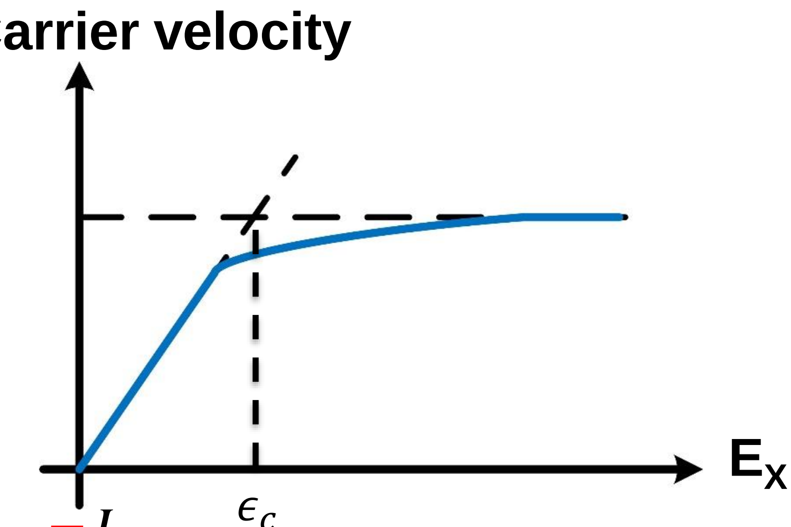




$$-I_{DS,w\ Velocity\ Saturation} = \frac{-I_{DS,w/o\ Velocity\ Saturation}}{0.5\left(1+\sqrt{1+2\left(\frac{V_{DS}}{L\epsilon_c}\right)^2}\right)}$$

Accurately models the current and its derivatives.

Channel Length Modulation

- Channel length modulation can be described as:

$$L_{eff} = L - l_p$$

$$l_p = l_a \times \ln\left(1 + \frac{V_{DSX} - V_{DS,eff}}{V_e}\right), l_a = \sqrt{3t_{ox}d_j}$$

t_{ox}: gate oxide thickness
d_j: source and drain junction depth
V_e: Early voltage

- Smoothing functions are employed to ensure about the continuity of the current around V_{DS}=0*:

$$V_{DS,eff} = \frac{V_{DS}}{(1+(\frac{V_{DS}}{V'_{DS}})^{10})^{0.1}}, V_{DSX} = \sqrt{V_{DS}^2 + 0.01} - 0.1$$

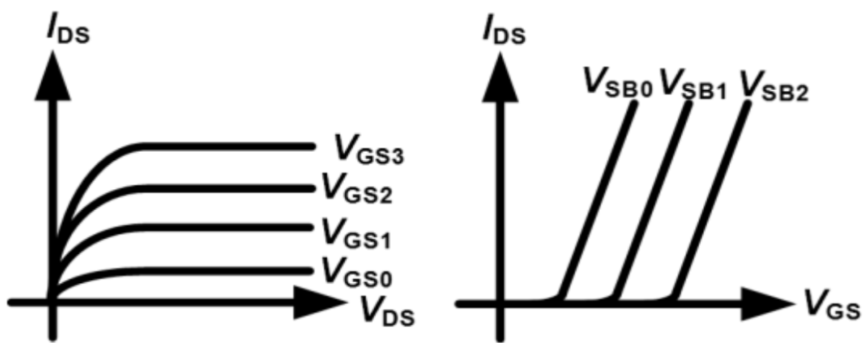
V'_{DS}: Smoothing function constant

*X. Li et al., “PSP 102.3,” NXP Semiconductors, Tech. Rep. 2008.

Model Parameter Extraction

Foundry provided model

Simulator



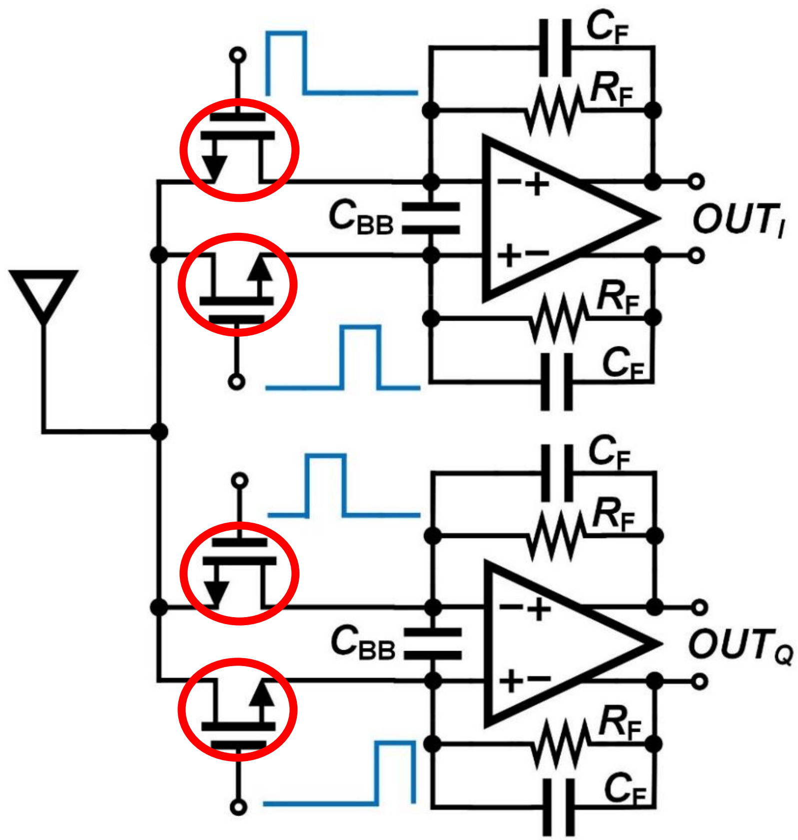
Curve-fitting using MATLAB

SSP model parameters

PSP Model Versus SSP Model

SSP Model	PSP
✓ Less than 20 parameters	× Hundreds of parameters
× Ignores temperature variation and process corners	✓ Includes temperature variations and process corners
× Only used for transistors operating as a switch	✓ All regions of operation

PSP Model Versus SSP Model



Only transistors operating as a switch are replaced with the SSP model.

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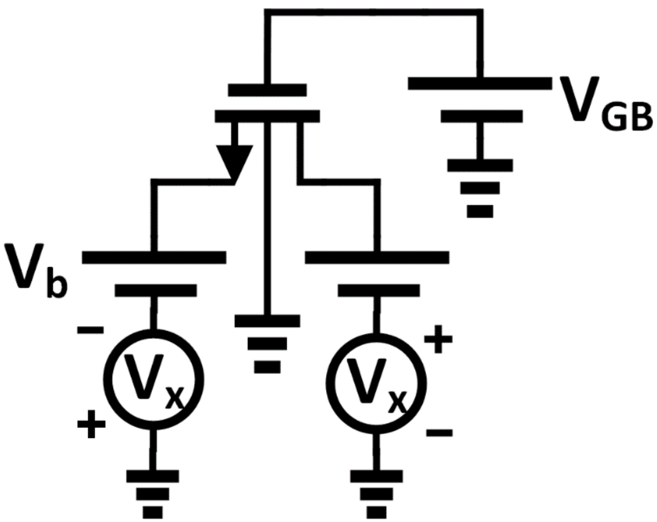
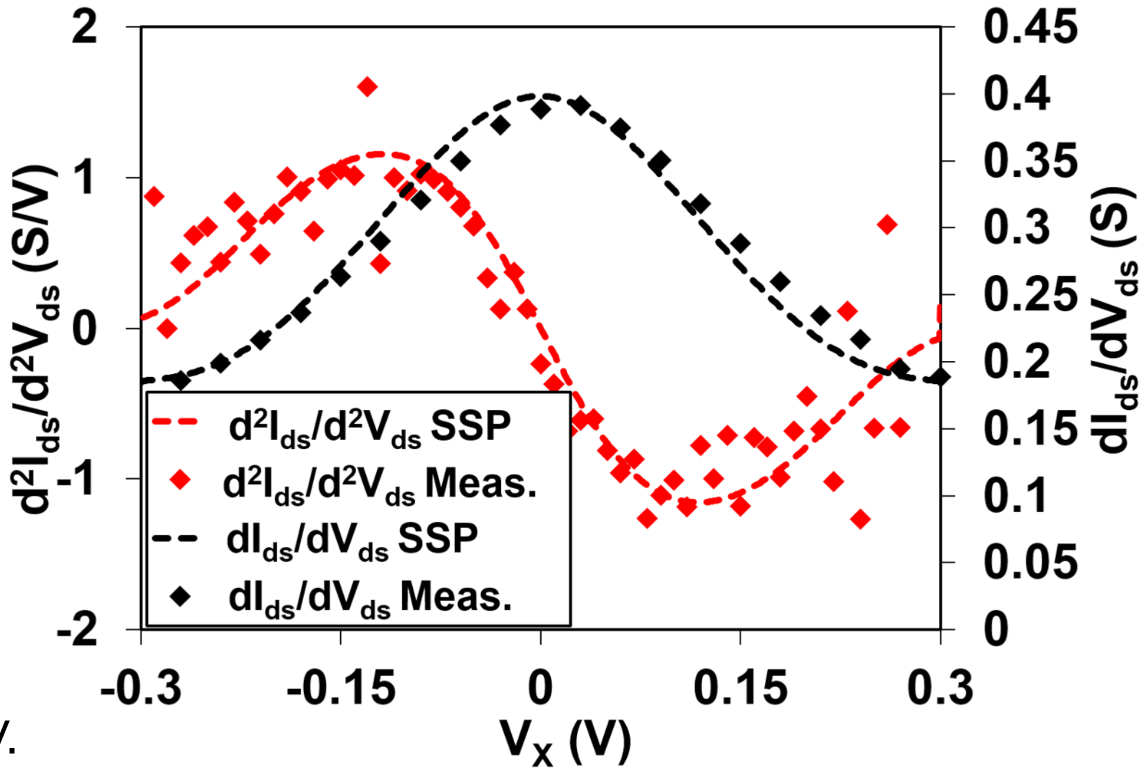
Measured Gummel Symmetry Test

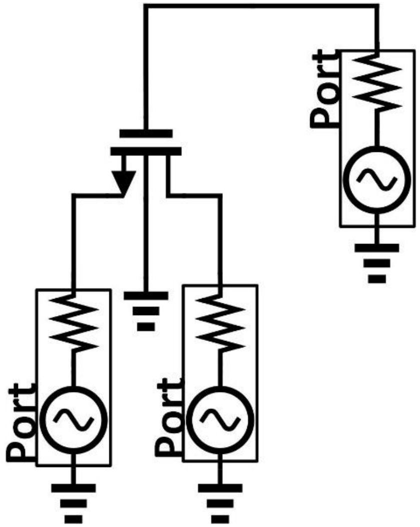


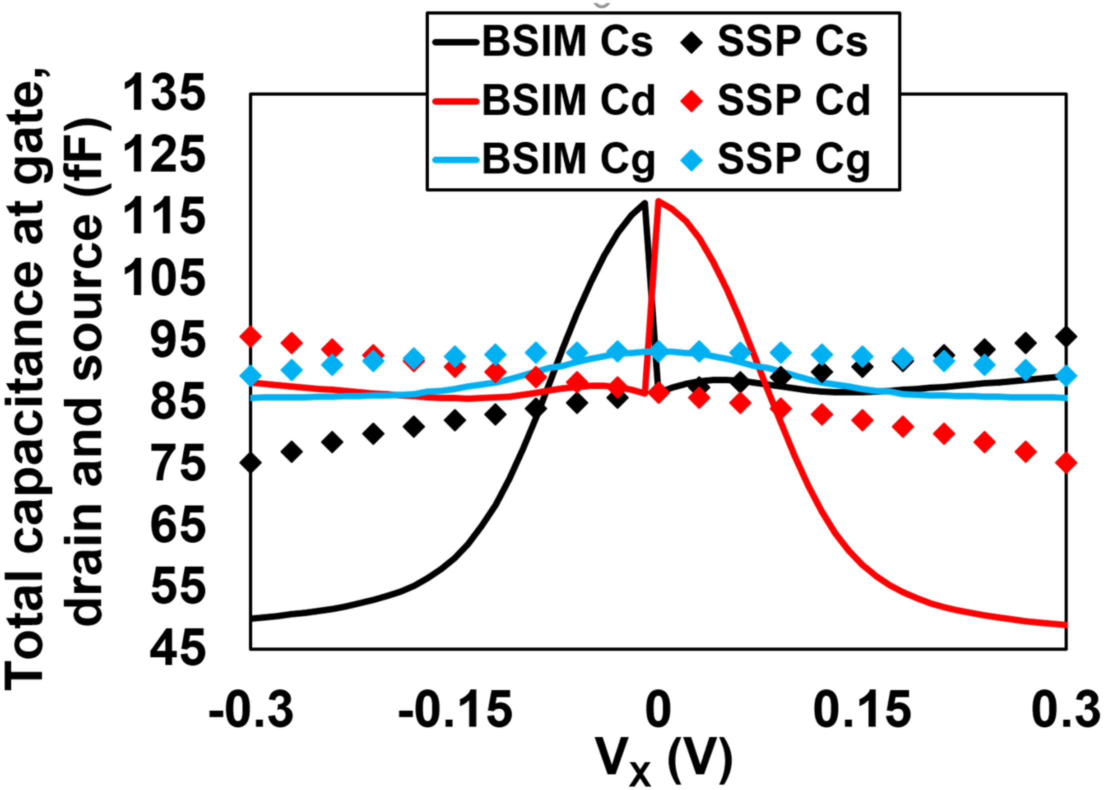
- 65nm CMOS;
- FET size: $\frac{96\mu m}{65nm}$;
- V_{GB} = 1.2V and V_b=0.3V.



The SSP model accurately predicts I_{DS} and its derivatives.

Terminal Capacitance Simulation

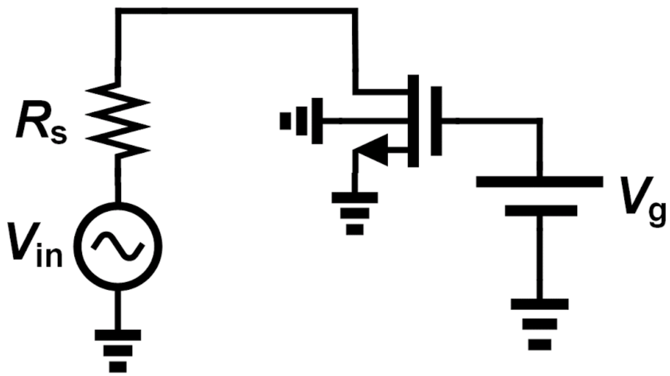




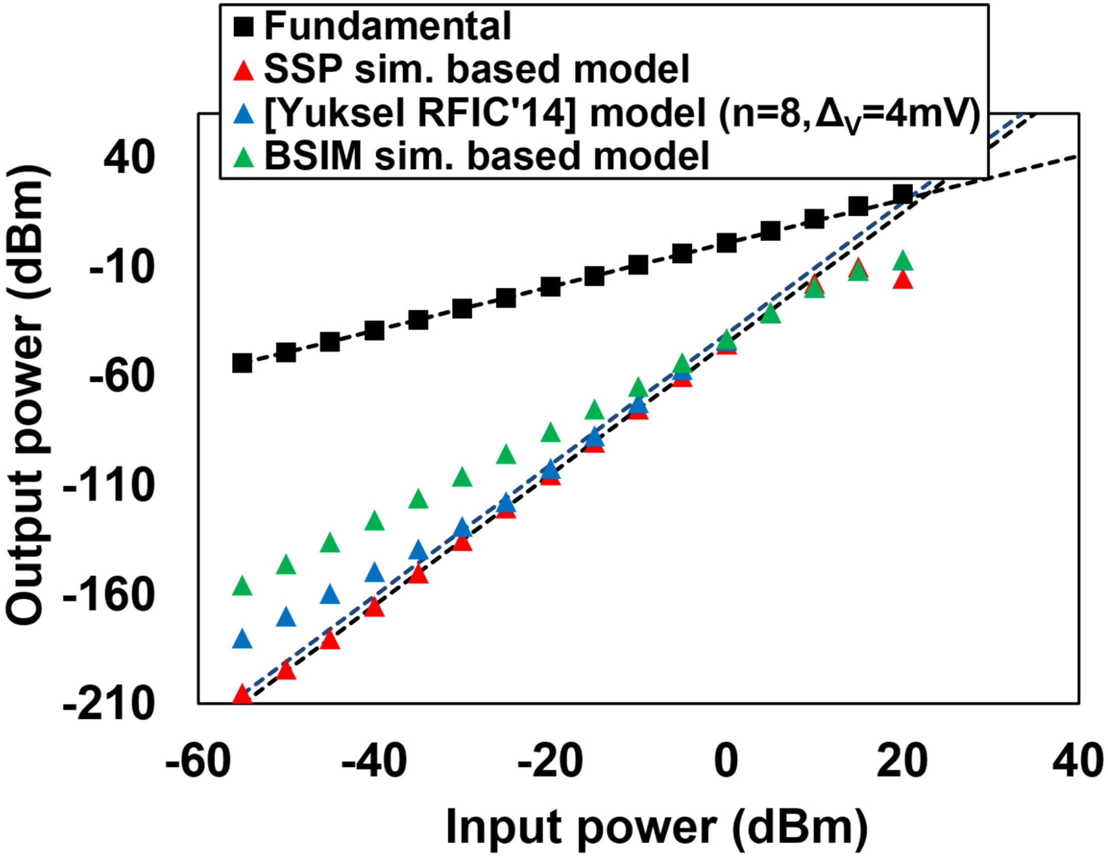
- All capacitors: 1F
- All Inductors: 1H
- 65nm CMOS;
- FET size: $\frac{96\mu m}{65nm}$;
- V_{GB} = 1.2V and V_b=0.3V.

The SSP model fixes the discontinuity in the terminal capacitances.

FET IIP$_3$ Simulation

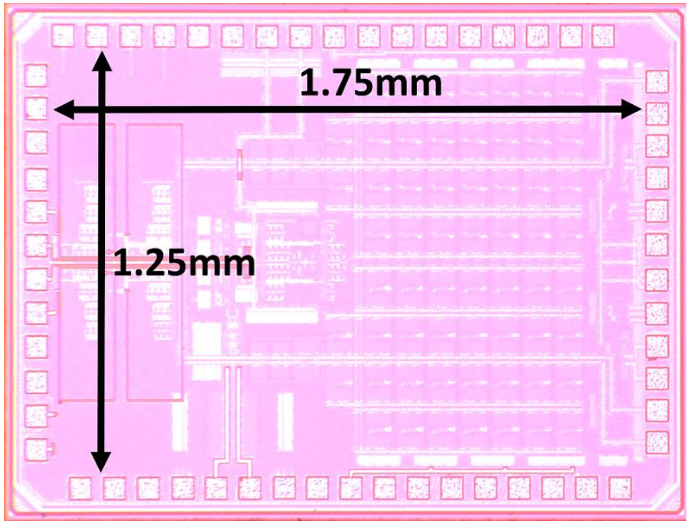


- 65nm CMOS;
- FET size: $\frac{96\mu m}{65nm}$;
- V_g = 1.2V.

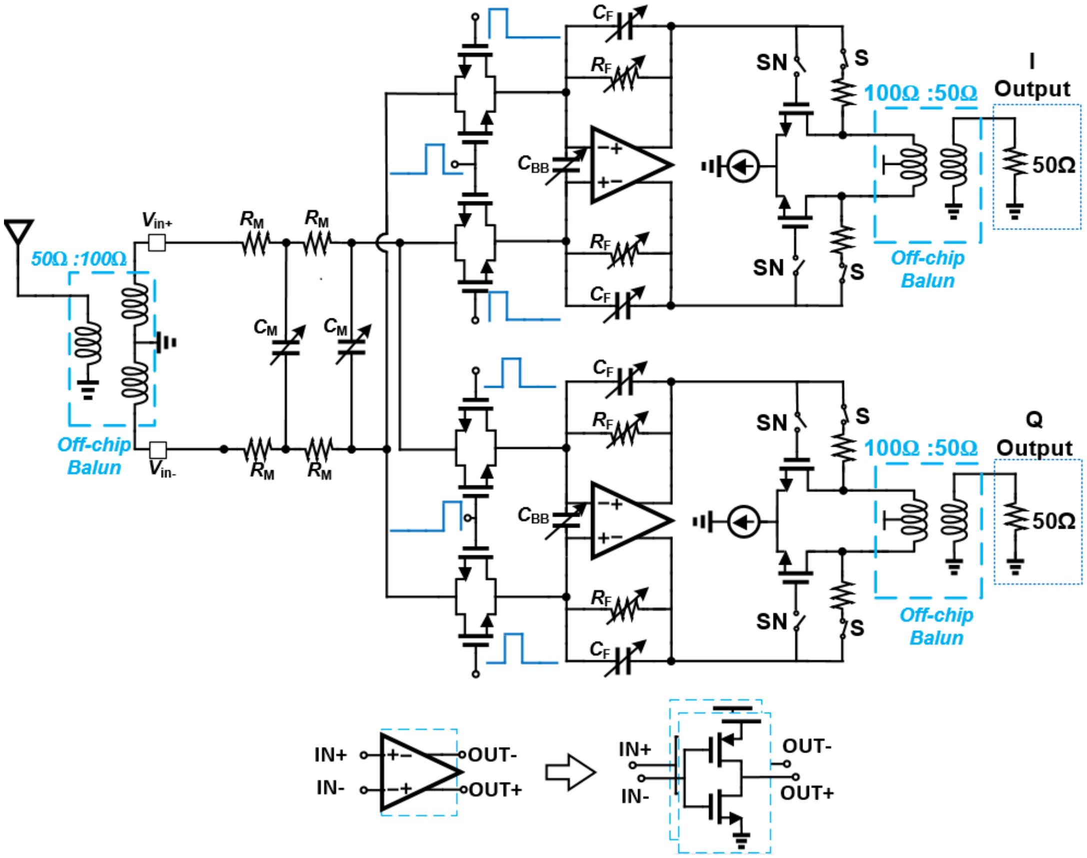


The model predicts 3dB/dB slope for IM$_3$ for a wide range of drain-source voltage across the FET.

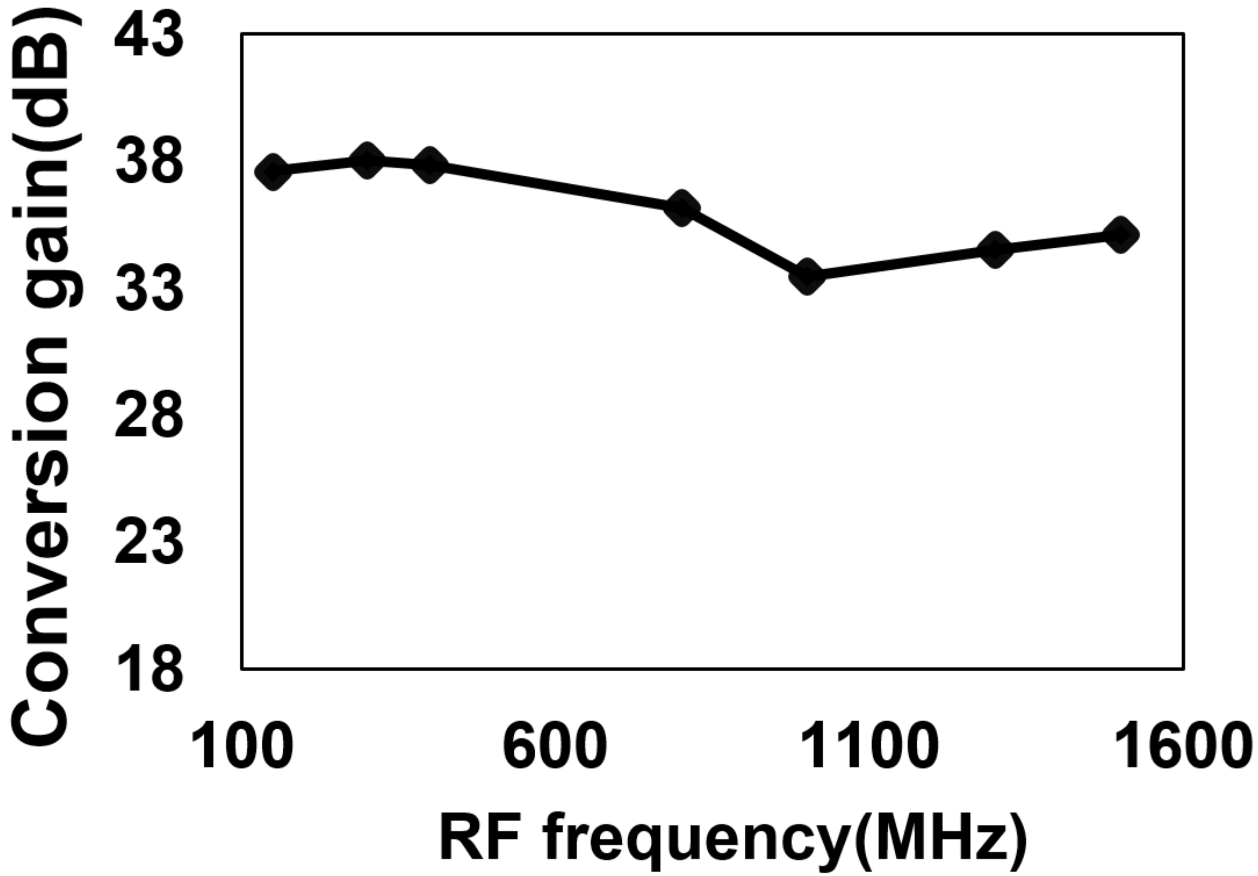
65nm CMOS Mixer-First Receiver



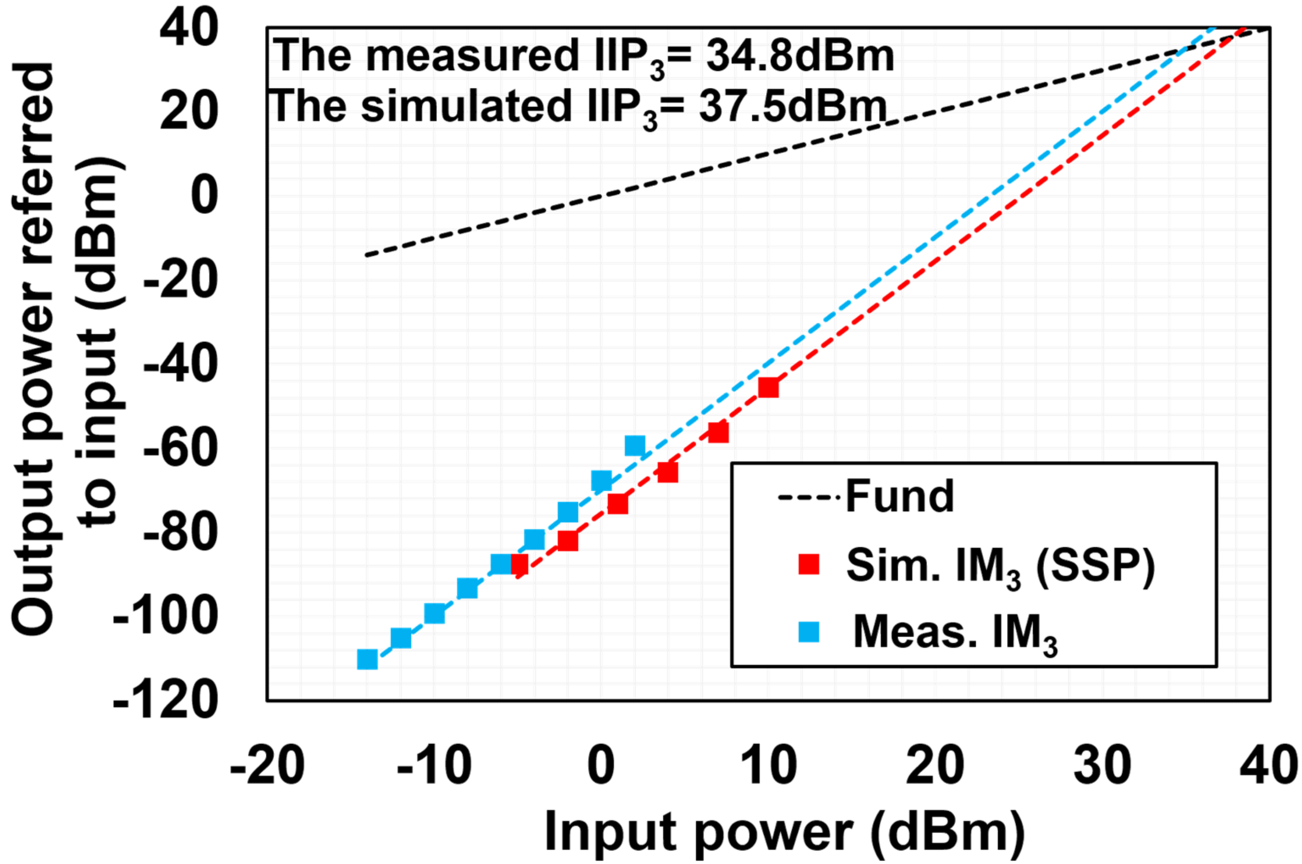
4-Path 0.15-2.5GHz passive-mixer-first receiver in 65nm CMOS.



Mixer-First Receiver Gain



Mixer-First Receiver Out-of-Band IIP_3



The LO frequency is 300MHz and input tones are applied at 500MHz and 699MHz.

The SSP model predicts IIP_3 with better than 3dB precision.

Comparison Table

	This work	[Yuksel 14]
Mixer-first receiver OOB-IIP$_3$ simulation accuracy	3dB (4-phase)	4dB* (8-phase)
Single switch simulation time(s)**	0.298	1.2
Mixer first receiver simulation time(min)	56***	Not feasible

*This is an 8-phase mixer-first receiver reported in [Andrews JSSC'10].
**The computer is equipped with quad-core i7 CPU and 32GB physical memory, and simulations are performed on schematic level.
***Simulation is performed with the PSS-shooting method with number of harmonics equal to 175, the LO frequency is 300MHz and tones are applied at 500MHz and 680MHz and simulation is done for 3 power level point.

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Conclusion

- Digitally-driven foundries typically provide BSIM4 models that yield unphysical results when simulating passive mixer-like circuits.
- A simplified surface potential model is introduced that does not require measurements for model fitting, and leverages the foundry-provided models for capturing second-order parasitics.
- The SSP model is more computationally relaxed than prior art, and shows greater accuracy in simulating linearity of passive-mixer-like circuits.
- The model is available at cosmic.ee.columbia.edu for download.