A 134 GHz +4 dBm Frequency Doubler at $f_{\max}$ in 130 nm CMOS

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***Abstract*—A +4 dBm 134 GHz frequency doubler operating at the maximum oscillation frequency ($f_{\max}$) of the technology is shown in an IBM 130 nm CMOS process. The doubler is implemented in a balanced topology, driven by a chain of stacked Class-AB amplifiers, and generates the highest reported power in 130 nm CMOS beyond 100 GHz. A theoretical study of frequency doublers is presented including scaling trends across frequency and CMOS technology nodes.**

***Index Terms*—CMOS, frequency doubler, mm-Wave.**

I. Introduction

MODERN CMOS nodes have an $f_{\max}$ from 130–300 GHz (Fig. 1). So, current CMOS high mm-Wave sources use device nonlinearity, in oscillators [1], [2] or frequency multipliers [3]–[5], [8], [9] to generate harmonics in this range.

We present a frequency doubler in 130 nm CMOS with +4 dBm output power at 134 GHz. We also present a theoretical analysis of a balanced doubler to identify fundamental performance limits across frequency and technology. In frequency multipliers output power is determined by device harmonic current and optimal load. Existing analyses in [3], [4] and [6] discuss increasing harmonic content through duty-cycle optimizations. To our knowledge, this is the first attempt at identifying the optimal load impedance of mm-Wave frequency multipliers. We also obtain a closed form expression for the output power purely in terms of technology metrics.

II. Scaling Trends in CMOS Multipliers

The conventional balanced frequency doubler in Fig. 2 has two transistors biased for nonlinear (low duty-cycle) operation and driven by anti-phase signals at the fundamental frequency. The second harmonic is extracted and the fundamental and odd harmonics are suppressed by connecting the drains before driving the load. A second harmonic trap (quarter-wavelength open stub) at the inputs forces the gate voltages at the second harmonic to zero, as the second harmonic current generated by a second harmonic voltage at the gate (fed back through C_{gd}) is detrimental to output power [3]. For the theoretical study, the devices are sized to drive 50 Ω optimally without impedance transformation to minimize output side loss.

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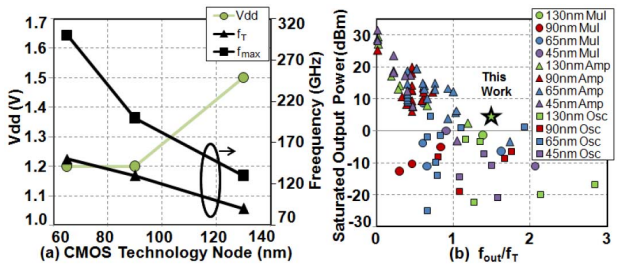

Fig. 1. (a) Scaling of supply voltage and cutoff frequency (f_T) across CMOS nodes. (b) Comparison of this work with state-of-the-art CMOS sources across output frequency normalized to technology f_T.

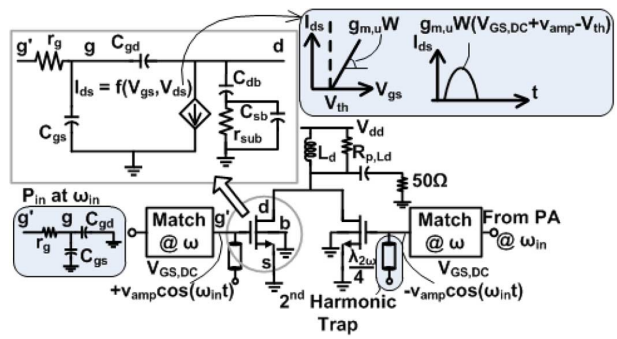

Fig. 2. Circuit diagram of a simple balanced CMOS frequency doubler.

In the device model in Fig. 2, aside from the nonlinear drain-source current I_{ds}, all capacitances and resistances are linear. Then, if $\omega_{\rm in}(C_{gs}+C_{gd})r_g \ll 1$, the input power is

$$P_{{\rm in},\omega_{\rm in}} \approx 2 \times \frac{v_{\rm amp}^2}{2}\omega_{\rm in}^2 r_g (C_{gs}+C_{gd})^2 \qquad (1)$$

where $\omega_{\rm in}$, r_g, C_{gs}, C_{gd} and $v_{\rm amp}$ are input frequency, gate resistance, gate-source and gate-drain capacitances and fundamental amplitude, respectively.

The output power is determined by the second harmonic current from the devices and the optimal load impedance. Assuming a piecewise-linear model for device current in Fig. 2, based on the gate bias $V_{GS,DC}$, the device transconductance generates a clipped sine-wave current. Authors in [3] and [4] show that the optimal duty-cycle to maximize second harmonic current is 35% if the peak positive gate voltage swing is set by the gate-source voltage limit for long-term reliability ($2 \times V_{dd} = 3$ V between any two device terminals). Given a threshold voltage of 0.45 V, this dictates negative gate bias voltages. The doubler in [3] uses 0 V gate bias. Additionally, gate-drain voltage swing limits must be considered. Simulated conversion gain at peak output power across bias, when both gate-drain and gate-source swing limits are considered, is relatively constant. For simplicity, a 0 V bias is used here.

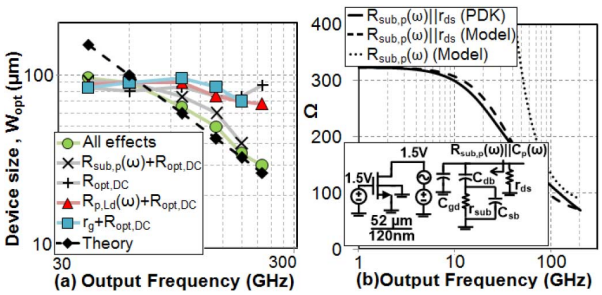

Fig. 3. (a) Device size needed to deliver maximum power to a 50 Ω load in a 130 nm CMOS balanced doubler. (b) Frequency dependence of $R_{\mathrm{sub},p}$.

Several mechanisms potentially limit the optimal load resistance R_{opt} (or alternately, the optimal device size that delivers maximum power to 50 Ω). The dependence of the device current on the drain voltage through channel length modulation or triode operation yields an optimal load resistance that we term $R_{\mathrm{opt,DC}}$. As it arises from device DC I-V characteristics, $R_{\mathrm{opt,DC}}$ is largely frequency independent. Other mechanisms include losses in drain inductance $(R_{p,Ld})$, substrate resistance and the gate resistance (seen from the drain through C_{gd}).

Fig. 3(a) depicts load-pull simulations of a balanced doubler in 130 nm CMOS across frequency. The optimal device size to drive 50 Ω is shown with the various effects sequentially enabled. $R_{\mathrm{opt,DC}}$ arises from I–V characteristics and cannot be turned off but substrate and gate resistance can be disabled in design kit models. $R_{\mathrm{opt,DC}}$ is indeed frequency independent, while gate resistance and losses in L_d produce negligible effect. Interestingly, *beyond an output frequency of 60 GHz and unlike fundamental-frequency small-signal/power amplifiers, the optimal load is dominated by substrate resistance*.

The substrate model is shown in Fig. 3(b), where $R_{\mathrm{sub},p}$ and C_p are the net parallel resistance and capacitance respectively. r_{ds} arises from channel-length modulation in saturation. The simulated output resistance of a 130 nm device in saturation is compared to the model where $R_{\mathrm{sub},p}$ is given by $R_{\mathrm{sub},p} = 1/(\omega^2 C_{db}^2 r_{\mathrm{sub}}) + (1 + C_{sb}/C_{db})^2 r_{\mathrm{sub}}$. When substrate resistance alone dominates, the optimal device size to drive 50 Ω would be $W_{\mathrm{opt}}(\omega) = 1/(\omega_{\mathrm{out}}^2 C_{db,u}^2 r_{\mathrm{sub},u} \times 2 \times 50\ \Omega) + (1 + C_{sb}/C_{db})^2 r_{\mathrm{sub},u}/(2 \times 50\ \Omega)$ as the 50 Ω load should be conjugate-matched to $R_{\mathrm{sub},p}/2$ (due to the presence of two devices). Here $C_{db,u}$ and $r_{\mathrm{sub},u}$ are per unit length. This $W_{\mathrm{opt}}(\omega)$ value moves from $1/\omega_{\mathrm{out}}^2$ dependence to a constant value. The range of interest, 60 to 200 GHz in 130 nm CMOS, lies in the transition between the two regions. For this range, preserving the value at the transition corner, optimal device size can be modeled with a $1/\omega_{\mathrm{out}}$ dependence

$$W_{\mathrm{opt}}(\omega) \approx \frac{(1 + \frac{C_{sb}}{C_{db}})}{\omega_{\mathrm{out}} C_{db,u} \times 50\ \Omega}. \tag{2}$$

The accuracy of (2) is verified in Fig. 3(a). $W_{\mathrm{opt}}(\omega)$ closely follows the optimal device size to drive 50 Ω as predicted by large signal simulations in the high mm-Wave range.

The simulated input power versus frequency for 130 nm and 65 nm CMOS designs is in Fig. 4(a). In (1), to maximize output power within breakdown limits v_{amp} is set to V_{dd}. As $r_g = r_{g,u}/W_{\mathrm{opt}}$, $C_{gs} = C_{gs,u} \times W_{\mathrm{opt}}$ and $C_{gd} = C_{gd,u} \times W_{\mathrm{opt}}$, where $C_{gs,u}$, $C_{gd,u}$ and $r_{g,u}$ are per unit length, the $1/\omega_{\mathrm{out}}$ dependence of W_{opt} means the input power is expected to linearly increase with frequency, as seen in Fig. 4(a).

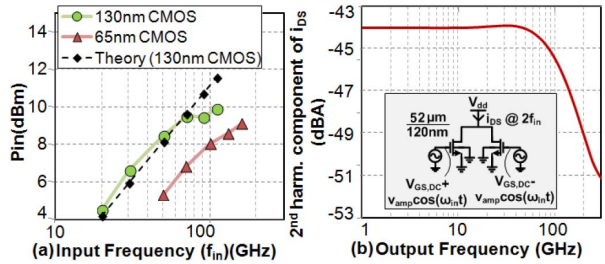

Fig. 4. (a) P_{in} of optimal doubler driving 50 Ω across frequency. (b) Frequency dependence of 2nd harmonic current due to NQS effect in 130 nm.

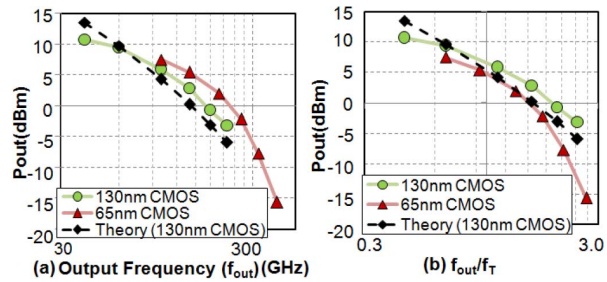

Fig. 5. Simulated output power for optimal doublers driving 50 Ω in 130 nm and 65 nm CMOS across (a) absolute f_{out}, (b) f_{out} normalized to f_T.

The second harmonic current for a clipped-sine-wave model can be written as $F_2 \times g_{m,u} \times W_{\mathrm{opt}} \times (V_{dd} - V_{\mathrm{th}})$. $g_{m,u}$ is the per unit width transconductance when $V_{gs} > V_{\mathrm{th}}$ and F_2 is the ratio of second harmonic component to peak. Half the current of both devices flows into the load due to conjugate match. *The optimality of conjugate match results from the dominance of the substrate network at mm-Wave and enables a closed form expression for output power*. At high frequencies, the Non-Quasi Static (NQS) effect, or the finite time of channel charge build-up, produces a roll-off in the output harmonic current. This is modeled as a pole at $f_{\mathrm{NQS}} = 150$ GHz in 130 nm CMOS [Fig. 4(b)]. The output power then is $P_{\mathrm{out}} = (1/2)(F_2 \times g_{m,u} \times W_{\mathrm{opt}} \times (V_{dd} - V_{\mathrm{th}}))^2/(1 + f_{\mathrm{out}}^2/f_{\mathrm{NQS}}^2) \times 50\ \Omega$, which becomes

$$P_{\mathrm{out}} = \frac{F_2^2}{100\ \Omega} \left(\frac{C_{\mathrm{in}}}{C_{\mathrm{out}}} \times \frac{C_{sb}}{C_{db}} \right)^2 (V_{dd} - V_{\mathrm{th}})^2 \frac{\left(\frac{f_T}{f_{\mathrm{out}}}\right)^2}{1 + \frac{f_{\mathrm{out}}^2}{f_{\mathrm{NQS}}^2}}. \tag{3}$$

$C_{\mathrm{in}} = C_{gs} + C_{gd}$ and $C_{\mathrm{out}} = C_{db}C_{sb}/(C_{db} + C_{sb})$. Equation (3) indicates that the output power falls first at 20 dB and then 40 dB per decade. Fig. 5 depicts the simulated output power for optimal doublers driving 50 Ω in 130 nm and 65 nm CMOS. It also plots the theoretical trend from (3) for 130 nm CMOS. Fig. 1 implies that $f_T \times (V_{dd} - V_{\mathrm{th}})^2$ is constant (≈90 GHz-V^2) across CMOS scaling. Ignoring NQS, (3) indicates that at a fixed f_{out}, a 65 nm doubler surpasses a 130 nm CMOS doubler in output power by the ratio of f_T, namely 2.2 dB. This is indeed seen in Fig. 5(a). If f_{out} is normalized to f_T, a 130 nm doubler surpasses its 65 nm counterpart by the ratio of $(V_{dd} - V_{\mathrm{th}})^2$, which is ≈3 dB [Fig. 5(b)].

III. A 134 GHz Doubler in 130 nm CMOS

A +4 dBm doubler at 134 GHz (originally designed for 120 GHz) is shown in 130 nm CMOS ($f_{\max} \approx 135$ GHz [2]).

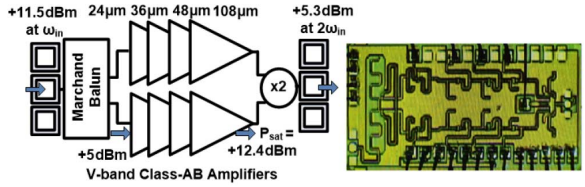

Fig. 6. Block diagram and chip photo of the 130 nm CMOS F-band doubler. The annotated values are at 67 GHz after post-layout simulations.

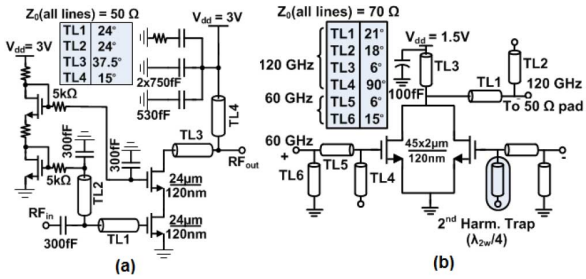

Fig. 7. (a) First V-band amplifier stage and, (b) the F-band balanced doubler.

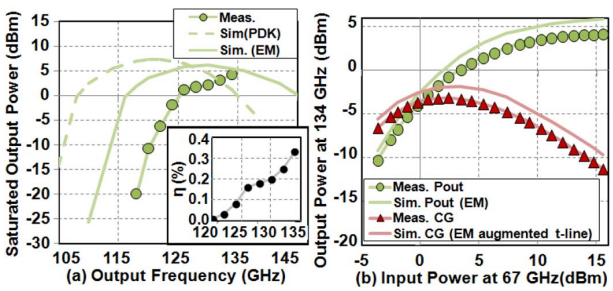

Fig. 8. (a) Measured and simulated saturated output power and efficiency. (b) Output power and conversion gain at 134 GHz.

A Marchand balun splits the input to drive two Class-AB V-band amplifier chains (Fig. 6). To mitigate the fundamental power generation challenge, two-way device stacking is used in the amplifiers to enable operation from 3 V and increase output power [7]. In 130 nm CMOS, the Maximum Available Gain (MAG) for a device is only 5 dB at 60 GHz. A cascode with identical devices has 7.5 dB MAG. MAG improvement through interstage matching or broadband neutralization shows ≈ 1.5 dB improvement before layout. We therefore use a simple cascode [Fig. 7(a)] laid out as in [7] with stepped gate and drain vias [3]. Device sizes of each stage are shown in Fig. 6. They are sized up by $1.33\times$ to $2.25\times$ to ensure saturation of the stages with compressed gains of 1.25 to 3.5 dB. Three stages are conjugate matched for gain. The last stage is designed for output power and efficiency. Each amplifier chain has a post-layout simulated small-signal gain of 14 dB at 67 GHz, 12.4 dBm saturated power and 8% drain efficiency.

The amplifier chain drives a doubler designed as in the previous section (Fig. 7(b)). The anti-phase devices are laid out as in [3] but with a shared drain. In the doubler layout, the pad capacitance along with the routing line to the shared drain transforms the probe 50 Ω to 30 Ω. This inevitable transformation in layout is steepened to 24 Ω as this block is used in a larger system where it drives 24 Ω and its performance can be directly verified. The reduction in load also proportionally increases output power. Based on Fig. 3(a), the optimal device size is around 100 μm, and the post-layout optimized size of 90 μm is very close indicating the strength of our analysis.

TABLE I
RECENT CMOS MULTIPLIERS BEYOND 100 GHZ

Ref.	Tech. (nm)	f_{in} (GHz)	f_{out} (GHz)	$\frac{f_{out}}{f_T}$	P_{sat} (dBm)	Pk. CG (dB)	P_{DC} (mW)	$\frac{P_{out}}{P_{DC}+P_{in}}$ (%)
This Work	130	67	134	1.4	4.2	-3.1	790	0.33
[8]	130	62.5	125	0.18†	-1.5	-10	N/A	10*
[4]	65	10.2	91.8	0.6	8.5	-5.7	438	1.54
[5]	65	122	244	1.62	-6.6	-11.4	40	0.51*
[9]	65	240	480	3.2	-6.3	-14.3	N/A	3.7*

†Diode Doubler, Diode $f_T = 680$ GHz
*Drivers not implemented, and will reduce efficiency.

The measured saturated output power and efficiency, defined as $\eta = P_{\text{out}}/(P_{DC} + P_{\text{in}})$, across frequency is in Fig. 8(a). Post-layout EM simulations of entire matching networks to capture the effects of bends and T-junctions improve correlation between simulations and measurements. A 7% upward frequency shift is still seen and can be from uncertainties in the device models and metal stack. The measured output power across input power at 67 GHz in Fig. 8(b) shows a peak conversion gain of -3.1 dB. Equation (3) predicts a power of 8.5 dBm which falls to 5.3 dBm after post-layout simulations and a peak power of $+4.2$ dBm is measured at an output frequency of 134 GHz with a total power consumption of 708 mW in the amplifiers and 81 mW in the doubler during peak operation. The simulated -3 dB saturated output power BW is 17%.

IV. CONCLUSION

Through analysis of fundamental limits and scaling trends of doublers across frequency and CMOS nodes, a 134 GHz doubler in 130 nm CMOS is implemented. It achieves $4\times$ higher output power than other 130 nm CMOS sources in the same frequency range (Table I) and state-of-the-art output power for the same normalized output frequency (f_{out}/f_T) across all CMOS technologies as seen in Fig. 1.

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