Calibrations for Millimeter-Wave Silicon Transistor Characterization

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***Abstract*—This paper compares on-wafer thru-reflect-line (TRL) and off-wafer short-open-load-thru (SOLT) and line-reflect-reflect-match (LRRM) vector-network-analyzer probe-tip calibrations for amplifier characterization and parasitic-extraction calibrations for transistor characterization on silicon integrated circuits at millimeter-wave frequencies. We show that on-wafer calibrations generally outperform off-wafer and LRRM probe-tip calibrations at millimeter-wave frequencies. However, certain parasitic-extraction algorithms designed specifically to remove contact pads, transmission-lines, and access vias correct for much of the error in off-wafer calibrations.**

***Index Terms*—Calibration, measurement, millimeter wave, scattering parameters, silicon, transistor, vector network analyzer (VNA).**

I. Introduction

SCATTERING-PARAMETER measurements of transistors fabricated on silicon die are usually calibrated with commercially available impedance-standard substrates. However, as these commercial calibration solutions measure scattering parameters "at the probe tips," and not at the transistor terminals, they are often augmented with additional measurements to try to remove the electrical parasitics associated with the probe pads and move the calibration reference plane closer to the transistor terminals. Assessing the accuracy of these approaches for augmenting commercial calibrations is one of the greatest measurement challenges of the high-frequency silicon community, and is the subject of this paper.

The vector-network-analyzer (VNA) calibrations used to characterize silicon transistors are usually performed in two steps [1]. These steps are often referred to as "tiers" of the calibration.

The first-tier calibration is usually an off-wafer probe-tip calibration. That is, it is performed on a commercial impedance-standard substrate using lumped-element standards and short-open-load-thru (SOLT) [2], line-reflect-match (LRM) [3], or line-reflect-reflect-match (LRRM) [4] calibration algorithms. These commercial calibration artifacts are usually fabricated by plating gold contacts and conductors on an alumina substrate, which ensures robust calibration standards and good contact repeatability.

This first-tier off-wafer calibration moves the calibration reference plane to the probe tips, and is often used to calibrate measurements of microwave amplifiers and other complex microwave circuits. As there is no single well-defined reference plane at this point, the probe-tip calibration is somewhat approximate.

Nevertheless, these probe-tip calibrations are more widely used in the industry than any other calibration type, and we study them for this reason. This is in part because probe manufacturers sell a variety of impedance-standard substrates and provide easy-to-use software packages to simplify the implementation of the calibrations. Users of commercial probe-tip calibrations do not have to fabricate or characterize the calibration standards themselves and can take advantage of calibration software that automates the calibration procedure.

For transistor characterization, the first-tier probe-tip calibration is often augmented by a second-tier calibration intended to extract the parasitics associated with the transistor-access vias and other access structures from the transistor measurements [1], [5]–[8]. These two-tier parasitic-extraction calibrations are intended to move the calibration reference plane from the probe tips to the transistor terminals, and yield measurements of the intrinsic elements of the transistor [1], [9]–[11]. These parasitic-extraction calibrations must subtract out the electrical parasitics associated with contact pads, transmission lines in the interconnect stack separating the contact pads from the transistors, and access vias connecting those transmission lines to transistors fabricated in the silicon substrate.

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Unlike probe-tip calibrations, first-tier on-wafer TRL calibrations lump the parasitics associated with contact pads and transmission lines in the interconnect stack into the error model for the VNA and probes, and place the calibration reference plane in a transmission line next to the transistor. On-wafer TRL calibrations have very few systematic errors [12]–[14], simplifying error analyses and making the thru-reflect-line (TRL) the calibration of choice for metrological applications.

Recently [15] demonstrated that on-wafer TRL calibrations appeared to perform well in small transmission lines built in an IBM 65-nm technology. Previous comparisons have shown that SOLT calibrations performed on an impedance-standard substrate do not perform as well as on-wafer TRL calibrations [9], [10]. This is because the TRL calibrations are designed to directly measure the scattering parameters in transmission lines fabricated on the wafer at a well-defined single-mode reference plane near the device-under-test.

However, one of the problems with on-wafer TRL calibrations on silicon is the difficulty of obtaining good contact repeatability to aluminum contact pads. In [16], we developed a gold-plating process that improves the quality of contact repeatability on aluminum contact pads to a level comparable to that obtained on commercial impedance-standard substrates. This has, in turn, greatly improved the quality of our on-wafer TRL calibrations in silicon interconnect stacks, effectively solving this problem and making TRL a viable choice for transistor characterization on silicon [16].

The more commonly used probe-tip calibrations, on the other hand, are easy to perform and do not require that custom calibration artifacts be fabricated in the silicon interconnect stack. Furthermore, engineers usually expect that the second-tier parasitic-extraction calibrations typically employed on silicon will repair errors in the first-tier calibration as the calibration reference plane is moved down to the transistor terminals. The ability of a second-tier parasitic-extraction calibration to repair errors in a first-tier off-wafer calibration was observed in experiments reported in [1] and [17], but the study was limited and no conclusions were drawn as to the approach with the greatest accuracy.

In this paper, we compare an on-wafer millimeter-wave TRL VNA calibration kit [16] fabricated in the IBM 45-nm complementary metal–oxide-semiconductor (CMOS) silicon-on-insulator SOI12S0 integrated-circuit process to commercial off-wafer SOLT and LRRM probe-tip calibrations performed on an impedance-standard substrate.[1] We also examine the performance of these calibrations after they are augmented by open-short, pad-short-open, and pad-line-short-open parasitic-extraction calibrations used for extracting intrinsic transistor models. This provides a firm basis for further investigating the hypothesis that second-tier parasitic-extraction calibrations on silicon repair errors in first-tier probe-tip calibrations advanced in [1], [2], and [17].

However, rather than simply showing good agreement between on-wafer and probe-tip calibrations, we try to determine which approaches are most accurate. We begin with a comparison of different first-tier calibrations to each other for purposes of amplifier characterization, as has been done in [18]–[22]. We then follow up with comparisons of combinations of first-tier and second-tier parasitic-extraction calibrations to better understand the hypothesis that these second-tier calibrations are able to repair errors in first-tier calibrations. Finally, we show that first-tier on-wafer TRL calibrations generally outperform first-tier probe-tip calibrations, even when these calibrations are augmented with second-tier parasitic-extraction calibrations designed to bring the calibration reference plane down to the transistor terminals. We also identify a second-tier calibration developed by Mangan *et al.* [23] that seems to be able to repair much, although not all, of the error in a first-tier SOLT calibration.

The conclusions regarding the improved accuracy of first-tier on-wafer TRL calibrations are important because they establish a baseline calibration with few systematic errors to which other calibrations can be compared by use of methods such as the calibration-comparison method [18]. This should facilitate the development of more accurate probe-tip and more compact on-wafer calibrations in the future by providing a well-understood calibration with which they can be verified (e.g., [3], [22], and [24]–[28]).

II. First-Tier TRL and SOLT Calibrations

Fig. 1(a) shows a photograph of the transistor test structure. The transistor was separated from the contact pads by 150-μm-long microstrip access lines to limit coupling between the probes. Fig. 1(b) shows a sketch of the cross section of the microstrip transmission lines.

A. On-Wafer TRL Calibration

The on-wafer TRL calibration kit, which was studied in detail in [16], consisted of a 300-μm-long thru line, a pair of symmetric shorts (reflects) offset by 150 μm from the contact pads, and four transmission lines with an additional length of 200, 300, 800, and 2000 μm. This design sets the nominal reference plane of the TRL calibration 150 μm from the contact pads in the center of the thru line. This position corresponds to the input at the left of the transistor shown in the figure. To minimize calibration and measurement errors, the contact pads and access lines are of the same design as the TRL calibration artifacts structures and the transistor test structures. See [16] for additional information on this calibration kit.

We fabricated the access lines and transmission lines used in the TRL calibration kit in the interconnect stack of the IBM 45-nm CMOS silicon-on-insulator SOI12S0 integrated-circuit process (see Fig. 1). That technology supports three thick metal and dielectric layers at the top of the interconnect stack. The transmission-line center conductor is fabricated in the topmost LB layer, and we were able to completely suppress metal fill in the two UA and UB layers below this topmost LB layer over a 24-μm width while adhering to IBM design rules. The center conductor is 6-μm wide and supported by approximately 6.275 μm of dielectric with a relative dielectric constant of about 4.0. This put the nominal characteristic impedance of the transmission lines at about 75 Ω, a reasonable match to the nominally 50-Ω probes.

[1]We use brand names only to better specify the experimental conditions. The National Institute of Standards and Technology (NIST) does not endorse commercial products. Other products may work as well or better.

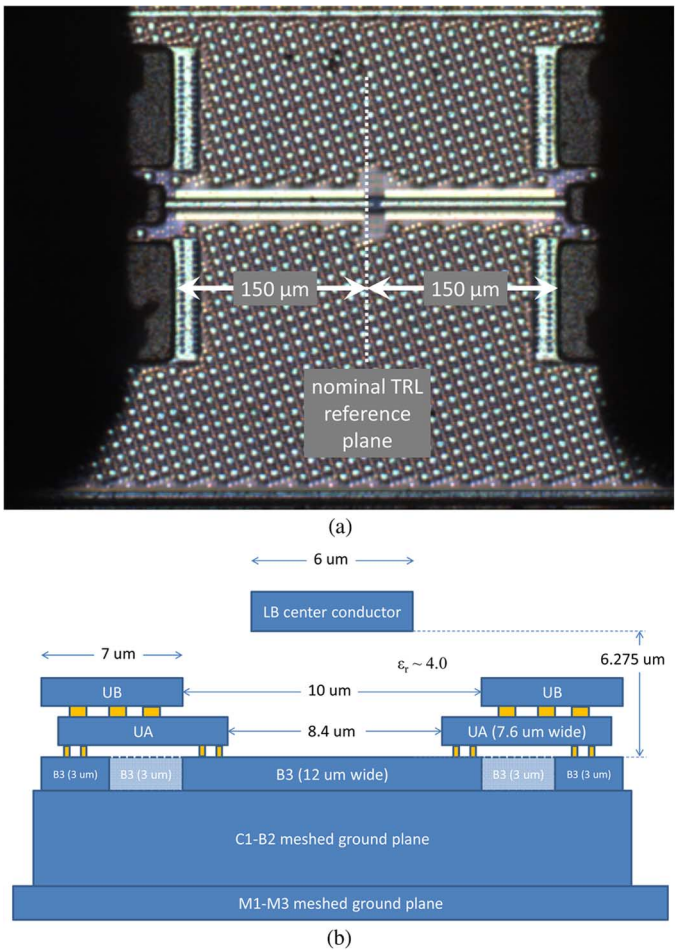

Fig. 1. Transmission-line calibration artifacts and test structures we employed. The interconnect stack supports 11 levels of metal: LB, UB, UA, B3, B2, B1, C2, C1, M3, M2, and M1 (from [1]). (a) Photograph of a test structure showing the contact pads, access lines, and device-under-test. The signal contact pads are 40-μm long and 30-μm wide, and are separated from the ground contact pads by 15 μm. Some of the automated fill on the top metal layers can be seen in the photograph. (b) Cross section of the transmission line.

The ground plane is fabricated in the fourth level of metal (B3) from the top of the interconnect stack. This solid level of metal is 12-μm wide and approximately 255-nm thick. To meet the design rules for the IBM process, we added 3-μm-wide strips of B3 metal spaced 3 μm from these 12-μm-wide ground lines and tied the ground plane together with 7.6- and 7.0-μm-wide strips in the next two higher levels of metal UB and UA, as shown in Fig. 1. We also meshed together all of the lower levels of metal below the B3 ground plane.

To set the reference impedance of the TRL calibration to 50 Ω, we first determined the capacitance per unit length of the line at low frequencies with the load method of [14]. We first moved the reference plane of the TRL calibration back to the contact pads using the propagation constant measured with the TRL algorithm to reduce the differences between the on- and off-wafer reference planes. We also verified the assumption of constant capacitance required by [14] in [16] through the application of the calibration-comparison method and numerical studies. However, since there were no on-wafer loads available on the wafer, we used an off-wafer load instead, potentially adding some error into the overall reference impedance of the calibration. We believe that this was a reasonable approximation as we were able to perform the required fits in [14] at only a few gigahertz, where the difference between the probe-tip and on-wafer reference planes (after translation back to the contact pads) were small. We also note that an error in the capacitance determined with an off-wafer load will uniformly shift the impedance level of the calibration, and have minimal overall impact on the results.

We then determined the actual characteristic impedance of the lines from the measured propagation constant with the method of [13], which works well in low-loss dielectrics. This provides the information needed to account for the complex characteristic impedance of these transmission lines and to transform the reference impedance of the TRL calibration to 50 Ω.

This correction is important even when nominally 50-Ω transmission lines are used in the calibration because the actual characteristic impedance of printed lines becomes large at low frequencies as the resistance per unit length of the lines becomes comparable to the inductive reactance per unit length of the lines. However, we note that an error made in determining the capacitance only results in a shift of the overall reference impedance, and does not have a large effect on the measurements.

B. Probe-Tip SOLT Calibration

We performed first-tier SOLT probe-tip calibrations on a commercial impedance-standard substrate with gold contact pads fabricated on alumina. The 50-μm-pitch probes and impedance-standard substrate were fabricated by the same manufacturer; we also used the standard definitions recommended by the manufacturer in the SOLT calibration algorithm. Finally, we measured the switch terms of our VNA, and corrected for them before applying the SOLT calibration algorithm. We did this to avoid errors in some SOLT calibration algorithms related to imperfect switch-term measurements caused by systematic errors in the definitions of the SOLT calibration artifacts themselves.

III. Amplifier Measurements

We started by comparing the first-tier on-wafer TRL calibration to a first-tier SOLT probe-tip calibration performed on a commercial impedance-standard substrate. Fig. 2 shows a measurement of the gain of an amplifier corrected with the two calibrations. The probe-tip calibration measures a slightly lower gain because its reference planes at the probe tips include, at least in an approximate way, the parasitics of the probe pad and access lines. In this case, the probe-tip calibration clearly does a good job of characterizing the amplifier's gain despite the approximations inherent in setting the reference plane at the probe tips.

Fig. 3 shows the maximum difference between scattering parameters S_{ij} corrected by the on-wafer TRL calibration and S'_{ij} corrected by the SOLT probe-tip calibration of a passive device, as determined by the calibration comparison method of [18]. These differences are surprisingly large, given the good performance of the SOLT calibration seen in Fig. 2.

It is not difficult to find devices whose measurements corrected by the SOLT calibration do not look nearly as good as those of Fig. 2. For example, Fig. 4 shows the magnitude of

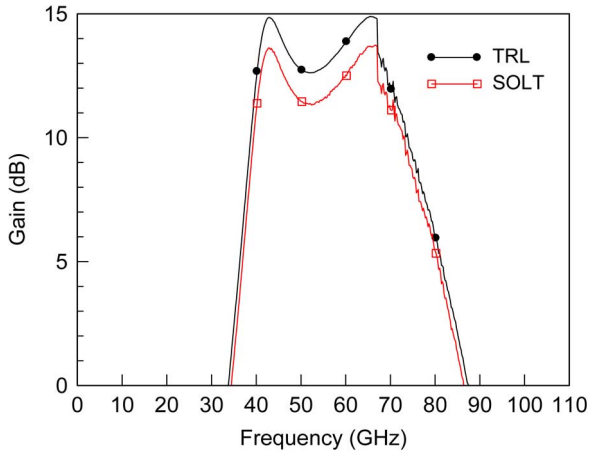

Fig. 2. Comparison of amplifier gain corrected with TRL and SOLT. We used the maximum power available from our VNA to try to maximize the power generated by the amplifier. An increase in power level in the VNA at 67 GHz caused the drop in gain seen above.

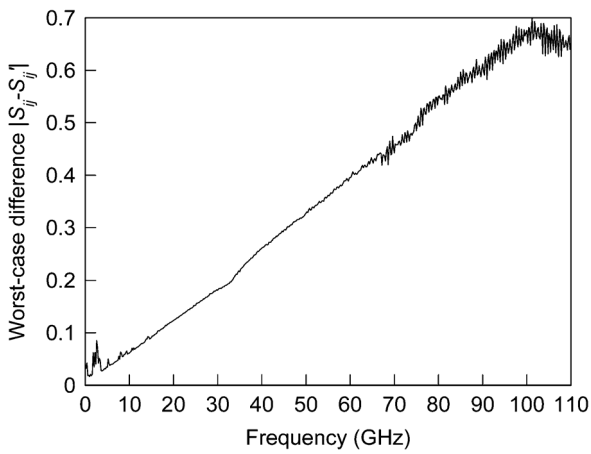

Fig. 3. Worst case differences between measurements corrected by the TRL and SOLT calibrations.

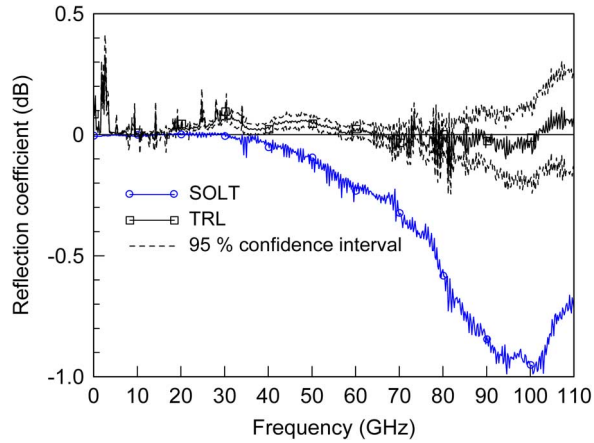

Fig. 4. Open pad corrected by the SOLT and TRL calibrations.

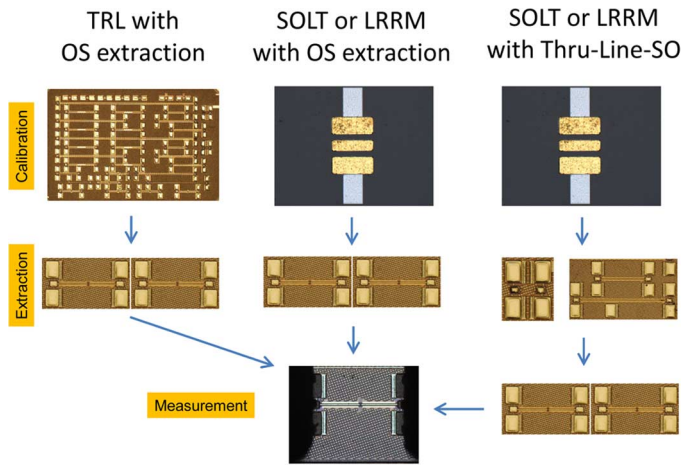

Fig. 5. Illustration of some of the first-, second-, and third-tier calibrations examined in this paper.

the reflection coefficient of an open circuit in the access line next to the contact pad corrected by the two calibrations. We also estimated the uncertainty in the TRL measurements with the method of [29] and [30] in the figure. While neither measurement is perfect, and our estimates of the uncertainties in the TRL-corrected results appear to be smaller than the actual measurement errors, it is clear that the TRL calibration outperformed the SOLT probe-tip calibration in this case. Thus, the first-tier TRL calibrations are preferred over first-tier SOLT probe-tip calibrations in cases like this, where the goal is to characterize amplifiers or other complex microwave circuits on the wafer without augmenting the first-tier calibration with second-tier parasitic-extraction calibrations.

IV. Transistor Measurements

Moving the measurement reference plane close to the device being tested is extremely important for transistor characterization [10], and motivates the use of the parasitic-extraction calibration algorithms discussed in the introduction. We used a set of metrics to compare probe-tip SOLT, probe-tip LRRM, and on-wafer TRL calibrations augmented with second-tier parasitic-extraction calibrations such as [5]–[11] to each other. Fig. 5 illustrates some of the algorithms that we examined.

A. Metrics for Transistor Measurements

The gate–source capacitance $C_{\rm gs}$, input resistance $R_{\rm in}$, drain–source conductance $g_{\rm ds}$, drain–gate capacitance $C_{\rm dg}$, drain–source capacitance $C_{\rm ds}$, and transconductance g_m of small lumped transistors depend only weakly on frequency. This provides a convenient set of metrics for comparing the ability of calibration algorithms to measure the intrinsic scattering parameters of a transistor.

To apply this idea, we can approximate $C_{\rm gs}$, $R_{\rm in}$, $g_{\rm ds}$, $C_{\rm dg}$, $C_{\rm ds}$, and g_m from the transistors admittance and hybrid parameters with the expressions [31]–[33]

$$\begin{aligned} C_{\rm gs} &\approx \frac{\mathrm{Im}(Y_{12}+Y_{11})}{\omega} \\ R_{\rm in} &\approx \mathrm{Re}(h_{11}) \equiv \mathrm{Re}\left(\frac{1}{Y_{11}}\right) \\ g_{\rm ds} &\approx \mathrm{Re}(Y_{22}) \\ C_{\rm dg} &\approx -\mathrm{Im}(Y_{12})/\omega \\ C_{\rm ds} &\approx \frac{\mathrm{Im}(Y_{22}+Y_{21})}{\omega} \\ g_m &\approx \mathrm{Re}(Y_{21}) \end{aligned} \tag{1}$$

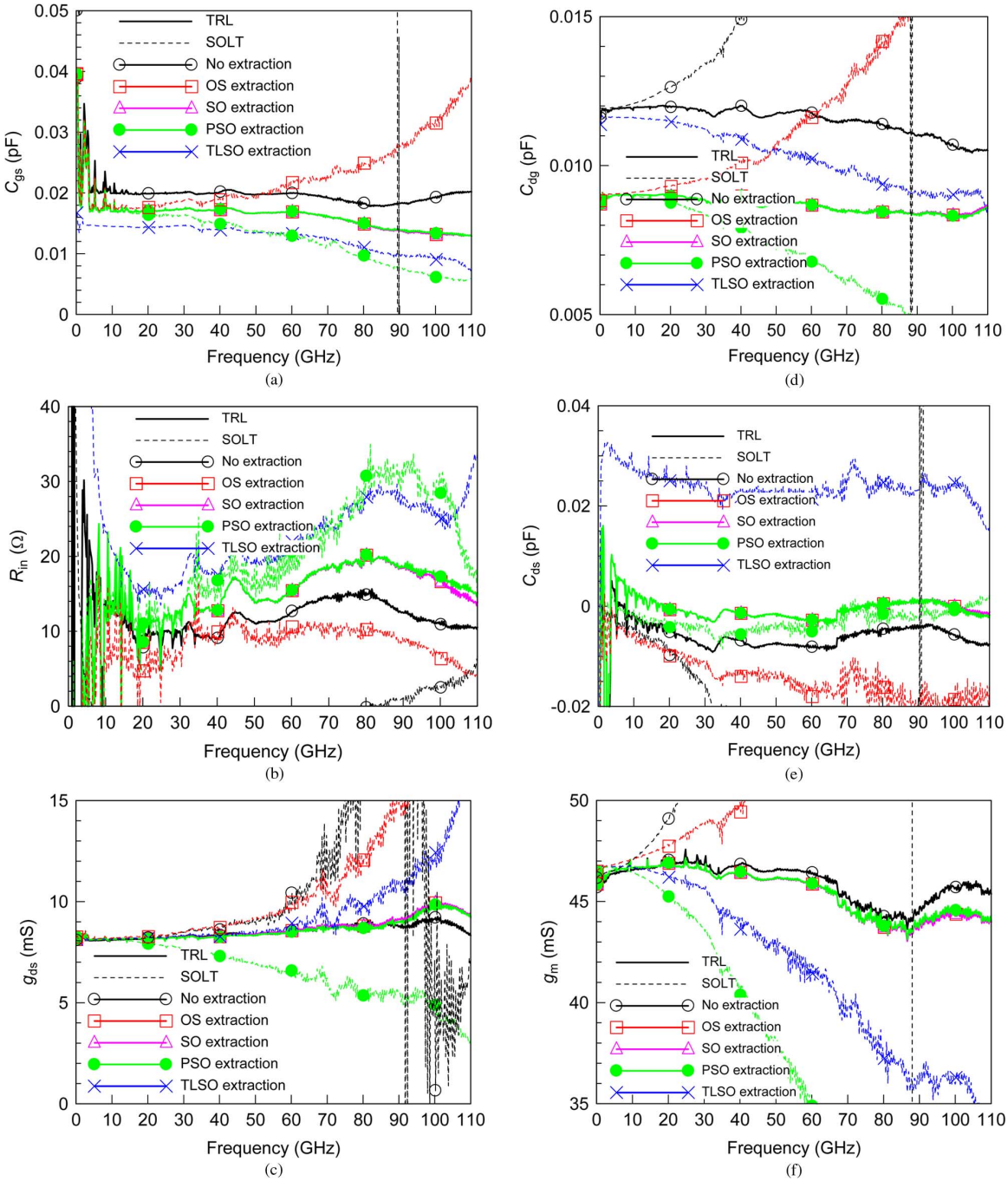

Fig. 6. Approximations from (1) for transistor measurements corrected with first-tier on-wafer TRL and SOLT probe-tip calibrations augmented by second-tier open-short (OS), short-open (SO), pad-short-open (PSO), and thru-line-short-open (TLSO) parasitic-extraction calibrations. (a) Approximation from (1) for gate–source capacitance $C_{\rm gs}$. (b) Approximation from (1) for input resistance $R_{\rm in}$. (c) Approximation from (1) for drain–source conductance $g_{\rm ds}$. (d) Approximation from (1) for drain–gate capacitance $C_{\rm dg}$. (e) Approximation from (1) for drain–source capacitance $C_{\rm ds}$; (f) Approximation from (1) for transconductance g_m.

where Ω is the frequency in radians, Y_{ij} are the admittance parameters of the transistor, and h_{ij} are the hybrid parameters of the transistor. We would expect $C_{\rm gs}$, $R_{\rm in}$, $g_{\rm ds}$, $C_{\rm dg}$, $C_{\rm ds}$, and g_m approximated from (1) and the intrinsic transistor admittance and hybrid parameters of the transistor to be frequency independent. If the calibration has errors or if the parasitic-extraction algorithms do not successfully remove the extrinsic transistor elements, the approximations of $C_{\rm gs}$, $R_{\rm in}$, $g_{\rm ds}$, $C_{\rm dg}$, $C_{\rm ds}$, and g_m determined from (1) will become frequency dependent. Similar approaches were used in [2] and [9]–[11] to assess the ability of a calibration to measure the intrinsic scattering parameters of a transistor.

B. Comparison of Calibration Approaches

Fig. 6 compares approximations of $C_{\rm gs}$, $R_{\rm in}$, $g_{\rm ds}$, $C_{\rm dg}$, $C_{\rm ds}$, and g_m from (1) derived from measurements of a silicon nFET power transistor with 40 fingers of width 770 nm and a minimum length of 40 nm designed for use at millimeter-wave frequencies. Table I lists the calibrations that we compared. We presented gain measurements of this transistor in [16]. The gate

TABLE I
CALIBRATIONS COMPARED IN FIGS. 6–9

Calibration/extraction type	No extraction	OS	SO	PSO	TLSO
On-wafer TRL	X	X			
Probe-tip SOLT	X	X	X	X	X
Probe-tip LRRM	X	X	X	X	X

was contacted on a single side, while the source and drain both exit on the opposite side of the gate in order to reduce parasitic capacitance. The sources connect directly to the ground plane. The drains are tapered while moving up through the metal stack to make contact with the signal line of the microstrip feeds.

All the data shown in the Fig. 6 are determined from the same raw measurements corrected with different first-tier calibrations and second-tier parasitic-extraction calibrations. The curves plotted in solid lines correspond to data corrected with our first-tier on-wafer TRL calibration, while curves plotted in dashed lines correspond to data corrected with the first-tier SOLT probe-tip calibration.

The on-wafer TRL and SOLT probe-tip calibrations with no parasitic extraction algorithms applied are marked with hollow circles in Fig. 6, and labeled "No extraction." The on-wafer TRL calibration with no extraction clearly outperforms the SOLT probe-tip calibration with no extraction, except at low frequencies, where the TRL calibration accuracy is limited by the length of the lines available on the die. This is certainly to be expected based on the amplifier measurements discussed in the last section of this paper, and the fact that the on-wafer TRL calibration places the measurement reference plane close to the transistor, while the SOLT calibration places the calibration reference plane at the probe tips and measures the combination of the contact pad, connecting microstrip line, via holes, and transistor.

The more important question is which calibration is more accurate after we try to extract the parasitic elements around the transistor with a second-tier parasitic-extraction calibration. The curves labeled "OS" and marked with hollow squares represent measurements that have been corrected with a second-tier parasitic-extraction calibration based on measurement of an open and a short [8]. This is a common approach for extracting the parasitic capacitances and inductances from the transistor measurements. We see from Fig. 6 that open-short extraction improves the flatness of the SOLT probe-tip results. Nevertheless, the SOLT probe-tip results with open-short extraction are still not as flat as the on-wafer TRL results with or without open-short extraction applied, except at low frequencies, where the TRL calibration accuracy was limited.

The results are similar for the second-tier short-open (labeled "SO" and marked with triangles in Fig. 6) and pad-short-open (labeled "PSO" and marked with solid dots in Fig. 6) calibrations [8]. While the extraction procedures improve the flatness of the SOLT probe-tip measurements, in most cases, the results are not nearly as flat as the corresponding on-wafer TRL results.

Fig. 6 also shows that augmenting the first-tier on-wafer TRL calibration with second-tier open-short, short-open, and pad-short-open parasitic-extraction algorithms does not greatly change the measurements. In fact, these results are most often so close to each other that their differences are difficult to distinguish in the figure. This shows that the additional corrections to the first-tier on-wafer TRL calibrations provided by the second-tier parasitic-extraction algorithms are small and relatively unimportant, and suggests that these second-tier corrections are not likely to introduce large errors into the measurements. This is important in metrological applications, as it is usually not possible to develop a rigorous basis for the analysis of calibrations based on lumped elements.

However, the same is not true of the SOLT probe-tip calibrations. Here we see that applying different second-tier parasitic-extraction calibrations yields significantly different results. This suggests that the second-tier parasitic-extraction calibrations are not entirely effective in eliminating the electrical behavior of the pads, microstrip access lines, and vias from the transistor measurements. Similar conclusions were reached in [2].

C. Pad-Line-Short-Open Extraction

The second-tier thru-line calibration algorithm developed by Mangan *et al.* [23] is designed to remove the impact of the contact pads, short access lines, and vias from transistor measurements. This calibration requires fabricating two transmission lines of different lengths. The calibration then removes the pad capacitance, estimates the characteristic impedance of the lines from the probe-tip calibration, and places the calibration reference plane at any desired point in the transmission line.

A third-tier parasitic-extraction calibration based on a pair of opens and shorts in the silicon interconnect stack can then be cascaded to the calibration to extract the transistor-access vias from the measurements. We called this the pad-line-short-open parasitic-extraction calibration. While this calibration requires more space on the wafer than traditional parasitic-extraction calibrations, it requires significantly less space on the wafer than a full multiline TRL calibration kit.

The dashed curves in Fig. 6 labeled "TLSO" and marked with X's correspond to first-tier SOLT probe-tip measurements augmented by a second-tier pad-line calibration followed by a third-tier short-open parasitic-extraction calibration. While there are some unexplained systematic and relatively constant offsets in $C_{\rm ds}$ and $R_{\rm in}$, the figure shows that this three-tier thru-line-short-open parasitic-extraction calibration algorithm generally does more to repair the approximations of the first-tier SOLT probe-tip calibration than the other second-tier calibration algorithms we tested. This is not surprising because the open-short, short-open, and pad-short-open extraction algorithms were not designed to account for the 150-μm microstrip access lines.

D. First-Tier LRRM Probe-Tip Calibration

Fig. 7 presents the same data as Fig. 6, except that a first-tier LRRM probe-tip calibration was used instead of a first-tier SOLT probe-tip calibration. The on-wafer TRL calibrations generally outperform the LRRM probe-tip calibrations, except at low frequencies, where the TRL calibration accuracy is limited by the length of the lines was limited by die size. Again, the LRRM calibration augmented by a second-tier

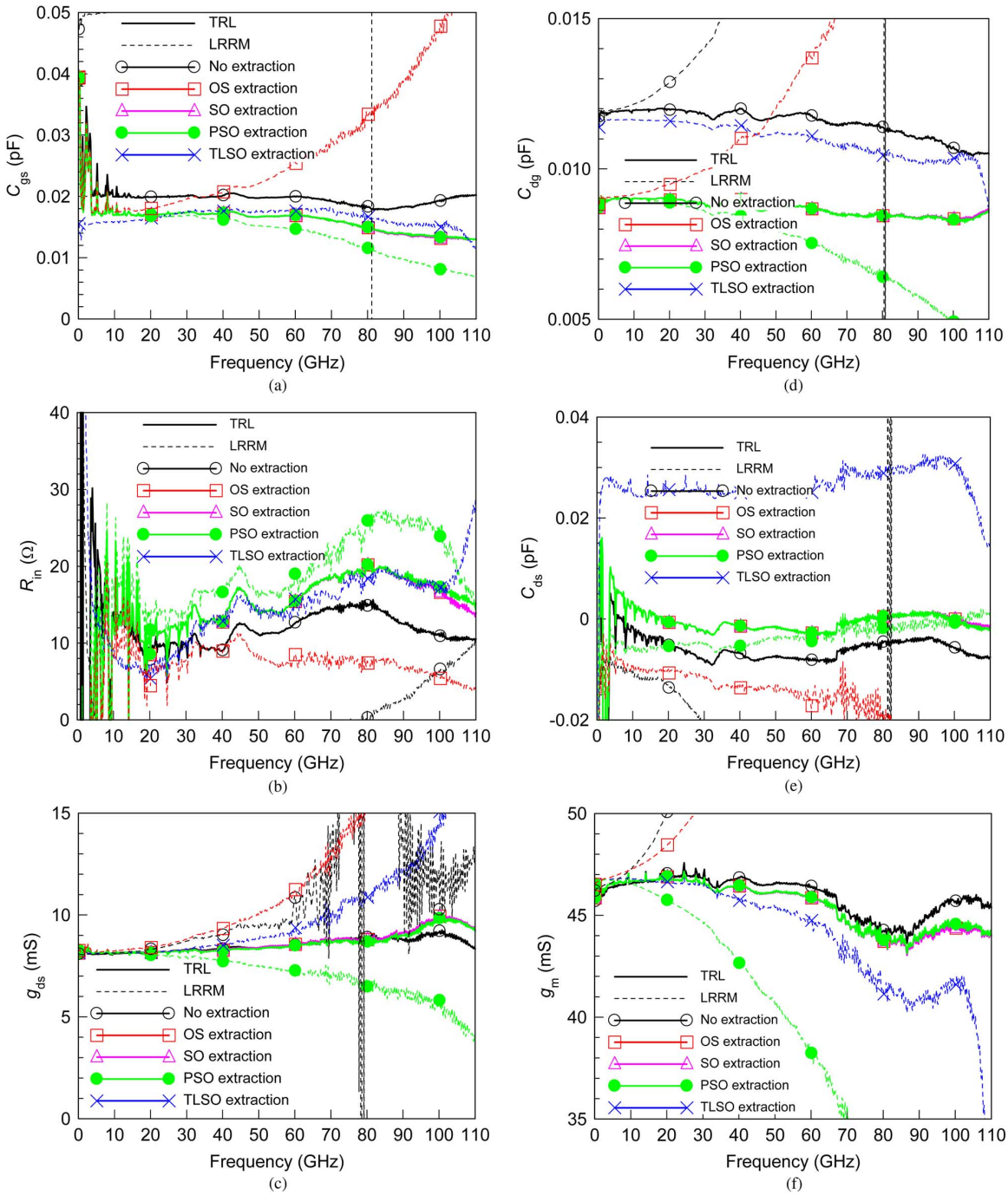

Fig. 7. Approximations from (1) for transistor measurements corrected with first-tier on-wafer TRL and LRRM probe-tip calibrations augmented by second-tier open-short (OS), short-open (SO), pad-short-open (PSO), and thru-line-short-open (TLSO) parasitic-extraction calibrations. (a) Approximation from (1) for gate–source capacitance $C_{\rm gs}$. (b) Approximation from (1) for input resistance $R_{\rm in}$. (c) Approximation from (1) for drain–source conductance $g_{\rm ds}$. (d) Approximation from (1) for drain–gate capacitance $C_{\rm dg}$. (e) Approximation from (1) for drain–source capacitance $C_{\rm ds}$. (f) Approximation from (1) for transconductance g_m.

on-wafer thru-line-short-open parasitic extraction calibration outperformed the other LRRM-based calibrations.

E. Comparison With Uncertainty Estimates

Due to the difficulty of assessing the error mechanisms in probe-tip calibrations, we were not able to estimate the uncertainties in the SOLT and LRRM calibrations. However, the error mechanisms in the TRL calibration are better understood. As a result, we were able to develop rudimentary uncertainty estimates for our TRL calibration. To do that, we took advantage of the use of overdetermined standards in the TRL calibrations and the relatively small systematic errors of the TRL calibration to simplify the analysis with the application of the orthogonal distance regression algorithm of [29] and [30]. This algorithm allowed us to estimate the uncertainty in the first-tier TRL calibration from the lack of fit of the measurements to the VNA calibration model.

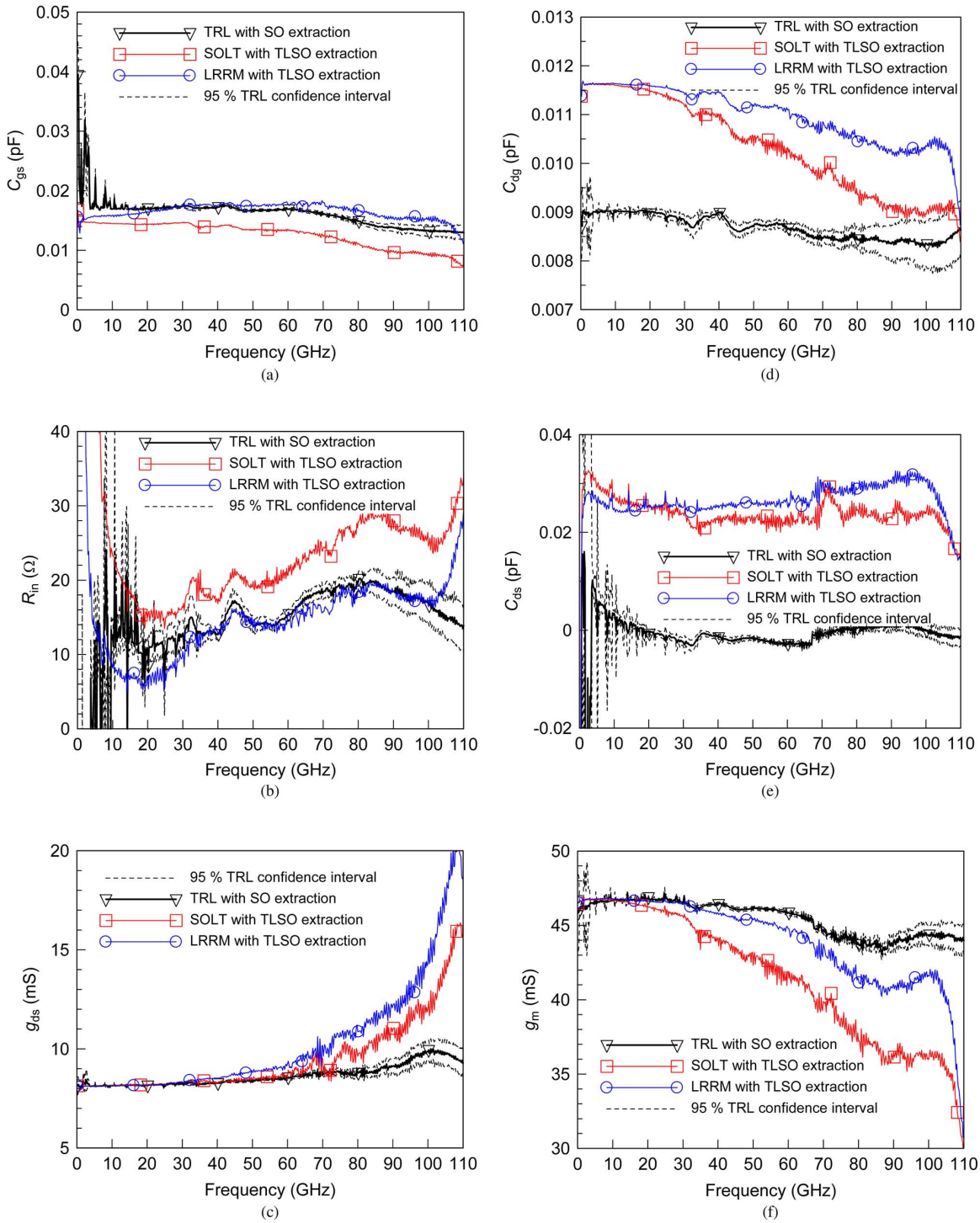

Fig. 8. Approximations from (1) for transistor measurements corrected with first-tier on-wafer TRL augmented by second-tier short-open (SO) parasitic-extraction calibrations and with first-tier probe-tip SOLT and LRRM augmented by second-tier on-wafer thru-line-short-open (TLSO) parasitic-extraction calibrations. (a) Approximation from (1) for gate–source capacitance $C_{\rm gs}$. (b) Approximation from (1) for input resistance $R_{\rm in}$. (c) Approximation from (1) for drain–source conductance $g_{\rm ds}$. (d) Approximation from (1) for drain–gate capacitance $C_{\rm dg}$. (e) Approximation from (1) for drain–source capacitance $C_{\rm ds}$; (f) Approximation from (1) for transconductance g_m.

Since we did not have redundant measurements of the shorts and opens used to de-embed the transistor access vias, and because that de-embedding step is still not well understood, we were not able to include estimates of the error in our transistor parameters due to error incurred in the transistor-access-via de-embedding step. Thus, while we expect our uncertainty estimates to underestimate the total measurement error, we still expect differences in results measured with different base calibrations to be bounded by the uncertainty estimates.

Fig. 8 compares $C_{\rm gs}$, $R_{\rm in}$, $g_{\rm ds}$, $C_{\rm dg}$, $C_{\rm ds}$, and g_m determined by TRL, SOLT, and LRRM calibrations with short-open extraction. Fig. 8 simplifies the comparison of the LRRM and

SOLT probe-tip calibrations, and makes it clear that the LRRM probe-tip calibration performs nearly as well as, and in some cases, clearly outperforms the SOLT probe-tip calibration.

Fig. 8 plots the 95% confidence intervals due to the uncertainty in the base TRL calibration via dashed lines. Except at the low frequencies, where the first-tier TRL calibrations fail, the estimated uncertainty is quite small. In fact, in most cases, the 95% confidence intervals are smaller than the overall ripples in $C_{\rm gs}$, $R_{\rm in}$, $g_{\rm ds}$, $C_{\rm dg}$, $C_{\rm ds}$, and g_m determined by the first-tier TRL calibration with short-open extraction. We attribute these discrepancies to unaccounted-for errors in the short-open extraction algorithm and the use of the approximations in (1), neither of which were included in the error analysis.

Nevertheless, if the base LRRM and SOLT calibrations were just as accurate as the base TRL calibration, we would anticipate that the *differences* of the TRL, LRRM, and SOLT results would be bounded by the 95% confidence intervals shown, after expansion by a factor of $\sqrt{2}$ to account for the equal uncertainties in the base LRRM and SOLT calibrations. As the differences in the plot clearly exceed this amount, it appears that the LRRM and SOLT calibrations must contain errors that are greater than the errors of the TRL calibration we estimated with the method of [29] and [30].

V. Conclusions

We first demonstrated the superiority of on-wafer TRL calibrations performed directly in a silicon interconnect stack over SOLT and LRRM probe-tip calibrations performed on an impedance-standard substrate for microwave amplifier and circuit characterization, except at low frequencies, where the TRL calibration accuracy was limited by the length of the lines that were available to us on our die. We also showed that the second-tier parasitic-extraction calibrations we used to augment SOLT and LRRM calibrations were not able to repair all of the error in the first-tier probe-tip calibrations based on an impedance-standard substrate.

The second-tier method of [23] proved to be an exception. While this calibration requires fabricating on-wafer transmission-line calibration artifacts in the silicon interconnect stack, and applies some of the same principles of the on-wafer TRL approach, it uses significantly less space on the silicon wafer than a full multiline TRL calibration kit and repaired much of the error in our SOLT and LRRM probe-tip calibrations. Furthermore, this calibration may be more practical when it is not possible to apply gold plating to the aluminum contact pads in the silicon interconnect stack.

Nevertheless, we found that overall the on-wafer TRL calibrations outperformed the SOLT and LRRM probe-tip calibrations based on lumped standards fabricated on an off-wafer impedance-standard substrate. In particular, changes due to augmenting the first-tier TRL calibrations with second-tier parasitic-extraction calibrations were small, and all of these second-tier calibrations yielded similar results. This leads to greater confidence in the approach.

We also note that first-tier TRL calibrations are not only more accurate, but rigorously founded in microwave circuit theory [12]. This allows the development of error analyses for TRL calibrations similar to that demonstrated in [34]. An error analysis for off-wafer SOLT and LRRM calibrations would likely have to be based on a comparison to TRL results. As such, it would be difficult to achieve the same low levels of uncertainty in the SOLT or LRRM analysis, as we would have to add differences between the SOLT and LRRM calibrations and the TRL calibrations to the uncertainty in the base TRL calibration.

We were not able to investigate all of the calibrations in current use. For example, we were not able to investigate off-wafer TRL and on-wafer SOLT, LRM, and LRRM calibrations. However, the demonstration of an accurate on-wafer calibration gives us a powerful tool for assessing the accuracy of these and other calibrations, both on-wafer and off-wafer.

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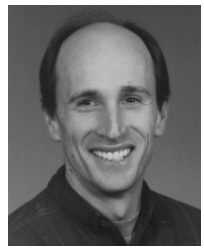

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