216- and 316-GHz 45-nm SOI CMOS Signal Sources Based on a Maximum-Gain Ring Oscillator Topology

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***Abstract*—This paper introduces a maximum-gain ring oscillator (MGRO) topology that maximizes the power gain (PG) achieved by the active devices in a ring oscillator using appropriately designed passive matching networks to maximize the frequency of oscillation. A design methodology is provided along with expressions for the passive matching elements. In the absence of passive losses, the topology can oscillate at the $f_{\max}$ of the active devices. In the presence of passive loss, for the first time, the losses can be taken into account in a closed-form fashion to maximize device PG, and consequently, oscillation frequency. Based on this topology, two different oscillators operating at approximately 108 and 158 GHz are implemented using the 56-nm body-contacted devices ($f_{\max} \approx 200$ GHz) of IBM's 45-nm silicon-on-insulator CMOS technology. The fact that these two oscillators function well with marginal startup gains of 2.62 and 0.62 dB, respectively, demonstrates the robustness of the techniques described here. The second harmonic of the oscillation is extracted using a load–pull-optimized extraction network. This topology can be generalized for the extraction of any harmonic from MGROs with a different number of stages. The oscillators generate −14.4 dBm at 216.2 GHz and −21 dBm at 316.5 GHz while drawing 57.5 and 46.4 mW of dc power, respectively. This paper also describes the modeling of CMOS active and passive devices for high millimeter-wave and sub-millimeter-wave integrated-circuit design.**

***Index Terms*—CMOS integrated circuits (ICs), CMOS process, CMOS technology, monolithic microwave integrated circuits (MMICs), oscillators, *Q* factor, ring oscillators, sub-millimeter-wave integrated circuits, submillimeter-wave measurements, submillimeter-wave technology, submillimeter-wave transistors.**

I. Introduction

THE HIGH millimeter-wave (100–300 GHz) and the sub-millimeter-wave (300 GHz–3 THz) regions of the electromagnetic (EM) spectrum lie between the usual frequencies of operation of electronic and photonic systems and have remained unexplored until quite recently. Applications include active and passive imaging, short-range high data rate communication links, sensing, and spectroscopy.

Sub-millimeter-wave signals have been dominantly generated using III–V compound semiconductors, [1]–[8]. In [1], using a 250-nm InP HBT technology with a maximum frequency of oscillation $f_{\max} > 800$ GHz, the authors have demonstrated fundamental oscillators at 573 and 412.9 GHz with −19 and −5.6 dBm of output power, respectively. Signal generation in the high-millimeter-wave/sub-millimeter-wave range has also been successfully demonstrated using heterostructure barrier varactor (HBV) multipliers [9]–[13]. Most recently, the authors of [12] have demonstrated an HBV quintupler generating 60 mW of power at 175 GHz. Signal sources based on GaAs Schottky diode multipliers have also been constructed [14]–[16]. The authors in [14] generate more than 0 dBm of power in the 840–900-GHz range using a frequency multiplier chain. The authors in [15] have shown −17.5 dBm of output power at 2.58 THz.

SiGe technologies have also become an active avenue for signal generation in the millimeter-wave and sub-millimeter-wave regimes, [17]–[22]. The authors in [19] construct a push–push oscillator generating −4.5 dBm at 190 GHz in an SiGe:C bipolar technology with an $f_{\max}$ of 275 GHz. A 278-GHz push–push oscillator in the same technology has been shown in [22]. Recently, in a 250-nm SiGe BiCMOS process ($f_{\max} = 435$ GHz), the authors in [17] have shown a spatially power-combined array of four frequency multipliers generating an effective isotropic radiated power (EIRP) of −17 dBm at 820 GHz.

Modern CMOS technology nodes have an $f_{\max}$ of about 150–300 GHz (130–65-nm CMOS). Loss in passive components is also quite high at these frequencies, and consequently these technologies cannot provide amplification in the sub-millimeter-wave/terahertz region. Current research focuses on building oscillators close to and below $f_{\max}$ (typically below 200 GHz), and extracting harmonics to extend the output frequency (f_{out}) beyond $f_{\max}$. The authors in [23] use the push–push technique with a cross-coupled oscillator (XCO) in 45-nm CMOS to generate a second harmonic at 410 GHz with −49-dBm power. The authors in [24] feed the four 90° out-of-phase outputs of a quadrature XCO to a rectification circuit that feeds the fourth harmonic to an external 50-Ω load. This shifts the burden of generating harmonic power from the oscillator core to the rectification circuit. A −46-dBm signal at 324 GHz is shown in 90-nm CMOS. In [25], the authors combine the fourth harmonic current at the source node of the coupling transistors of a quadrature XCO to generate a −36.6 dBm 553-GHz signal in 45-nm CMOS. They include a matching network between the common source node and the antenna to increase the fourth harmonic power transmitted. In [26], the inductance of a regular XCO is split between the core and the buffer stage. This mutually couples back the signal from the buffer to the core

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to improve the oscillator loop gain and thus improve the fundamental oscillation frequency to 300.5 GHz in 65-nm CMOS. The authors of [27] have designed a traveling-wave oscillator with a 300-GHz second harmonic output in 45-nm SOI CMOS. The geometry of the oscillator and the ground plane is such that the structure is radiative at the second harmonic. They mutually lock and spatially combine such *distributed active radiators* to improve the total radiated power. The total radiated power of a 2×1 array is -19 dBm, and that of a 2×2 array is -10.9 dBm. In [28], the same authors show a 282-GHz 4×4 beam-steering array of distributed active radiators in 45-nm SOI CMOS with 80° electronic beam scanning in each of the orthogonal axes in 2-D space. A total power of -7.2 dBm is radiated broadside with an EIRP of 9.4 dBm while consuming around 800 mW of dc power. A tuning range of 3.2% has been shown around 280 GHz. Finally, the authors of [29] attempt to maximize $f_{\rm osc}$ by increasing the small-signal startup gain of a ring oscillator. They do so by maximizing the small-signal power added per stage. They have shown a 256-GHz third harmonic oscillator with -17-dBm output power in 130-nm CMOS and a 482-GHz third harmonic oscillator with -7.9-dBm output power in 65-nm CMOS. It should be noted that in these works, the output is at the center of the ring oscillator and the on-chip routing losses of a practical implementation are not included. In [30], the authors show a voltage-controlled oscillator (VCO) in a 65-nm CMOS process with a fourth-harmonic output power of about -1.2 dBm at 292 GHz. It has a tuning range of 4.5% around 290 GHz using variable coupling between injection locked oscillators. In [31], the authors use a 90-nm CMOS process and generate -6.5 dBm of power at 228 GHz by extracting the third harmonic from a differential VCO in a Colpitts configuration. They show a tuning range of 7%. Finally, the authors of [32] have shown a doubler in 45-nm SOI CMOS generating -3–0 dBm of output power in the 170–195-GHz range with a conversion gain from -2 to -1 dB.

This brief overview suggests that while CMOS based oscillators and sources are now able to operate in the high millimeter-wave/terahertz regime, additional research needs to be done to produce output frequencies and power comparable to compound semiconductor technologies. Our work introduces a topology that maximizes the frequency of oscillation achievable in a given technology through a ring oscillator configuration with appropriately designed passive matching networks. There have been many works in the microwave community that lend significant insight into maximizing oscillation frequency and output power. The author in [33] discusses the existence of a specific voltage ratio between the drain and the gate terminal that maximizes the power gain (PG) from the gate to the drain, thus improving small-signal loop gain. Our work improves on this by standardizing the methodology of arriving at the passive network to achieve this gain. Our work also explicitly accounts for passive loss in a closed-form fashion, and allows for any phase shift per stage for a multistage ring oscillator with arbitrary number of stages. This, in turn, allows power combining of different number of stages for larger output power. The authors in [34] similarly attempt to improve loop gain of a ring oscillator, but maximize added power from the gate to the drain. Other works of interest that work on maximizing PG across a ring oscillator include [35].

This paper is organized as follows. Section II discusses the modeling of the IBM 45-nm SOI CMOS active and passive devices. Section III deals with the maximum-gain ring oscillator (MGRO) concept. Section IV discusses the design and optimization of networks that extract harmonic output power from the MGRO. It also discusses the possibility of spurious-mode oscillations, which must be suppressed. Section V discusses the measurement setup and the performance of the fabricated chips. Section VI concludes this paper.

II. 45-nm SOI CMOS Technology Characterization

A. Active Devices

The IBM 45-nm SOI CMOS technology offers floating-body (FB) devices with a channel length of 40 nm and body-contacted (BC) devices with a channel length of 56 nm. The BC devices are slower than their FB counterparts due to their longer channel length and the additional capacitive parasitics introduced by the body contact. We have measured a 10×1 μm/56 nm BC, a 20×1 μm/56 nm BC, and a 10×1 μm/40 nm FB device. The *gate-over-device* layout used in this work is shown in Fig. 1 for a BC device. For the FB device, the body-contact notches [36] are absent. The thick via-walls for the gate and the drain reduce wiring resistance. The layout allows a symmetric doubly contacted gate. The concern of capacitance between the gate and drain via-walls is mitigated by placing them sufficiently far apart, while a possible increase in drain resistance is reduced by using the winged structures in M_2, as shown. The fringing capactance from the wings to gate does not add to the gate–drain via capacitance.

Fig. 2 shows a simplified BSIMSOI 4.x model (inside the dotted box [37]) to demonstrate some of the important components that model high-frequency effects. The components that are absent in the Process Design Kit (PDK) model, namely, the non-quasi-static gate resistance $r_{\rm iir}$, and $r_{\rm BDB}$ and $r_{\rm BSB}$ in the body resistance network, have been marked in dashed boxes. Wiring self-$(L_{\rm gwire}, L_{\rm dwire})$ and mutual-$(K_{\rm gd})$ inductances, resistance $(r_{\rm gwire})$, and capacitances ($C_{\rm gswire}$, $C_{\rm gdwire}$, and $C_{\rm dbwire}$) are located outside the dotted box containing the BSIMSOI model, and are also not included in the PDK. The mutual inductance is primarily from the coupling between the drain and gate vias. Wiring parasitics are determined through parasitic extraction using the Calibre extraction tool and through EM simulations using the IE3D field solver [38].

Open-short deembedding [39] was used to deembed the pad and feedlines from the device test structures that were measured. The sufficiency of open-short deembedding up to 67 GHz has been verified by EM simulations, which confirm that the pad and the feedline can be treated as lumped components at these frequencies. The deembedding is done up to a reference plane located at the top of the gate and drain vias. The measured Mason's unilateral gain (U) and h_{21} for the 10×1 μm/56 nm BC device at a current density $J = 0.56$ mA/μm is shown in Fig. 3(a). To determine $f_{\rm max}$ and cutoff frequency f_T, a 20 dB per decade line is extrapolated from the measured U and $|h_{21}|$. A similar approach is applied for the other two devices as well. The extrapolated $f_{\rm max}$ and f_T for all three devices across current density J are shown in Fig. 3(b) and (c). The peak $f_{\rm max}$

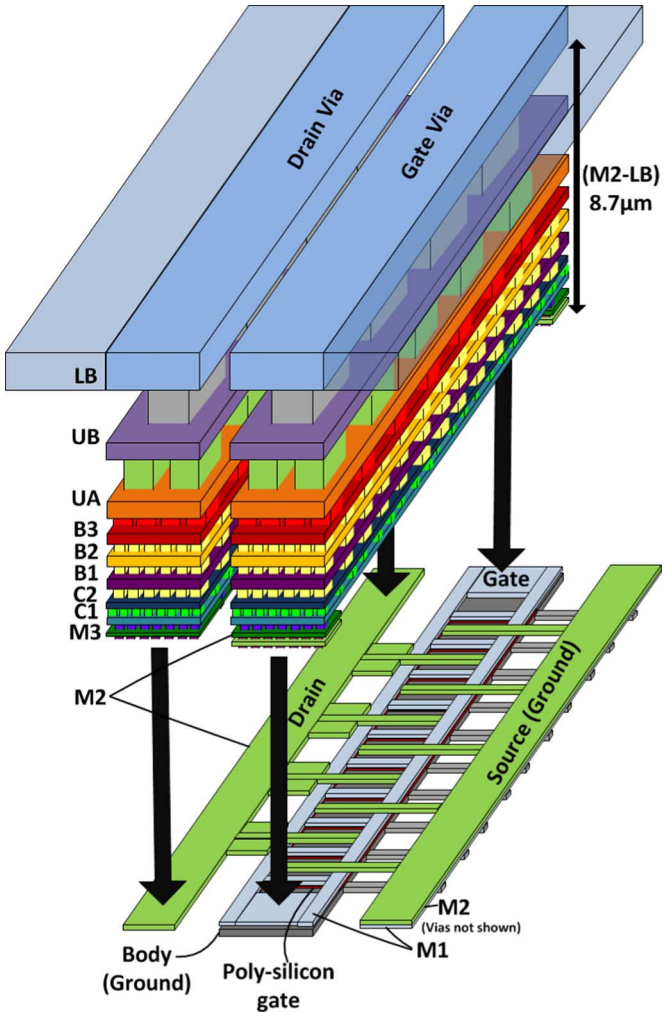

Fig. 1. Layout of a BC NFET device. This allows the gate to be doubly contacted in a symmetric fashion.

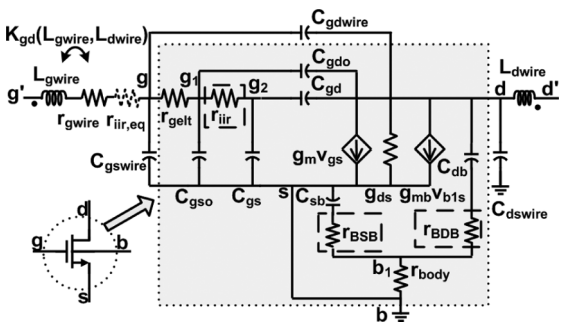

Fig. 2. Model for the NFET BC device. In the FB version, there is no b node and $r_{\rm body}$ is absent. The FB node is b_1.

of the 10×1 μm/56 nm BC device is around 210 GHz for a $J = 0.3$ mA/μm, and that of the 10×1 μm/40 nm FB device is about 250 GHz for a $J = 0.4$ mA/μm.

Mason's unilateral gain U of devices can have behavior different from a 20 dB per decade slope [40], [41]. Thus, it is important to predict figures like $f_{\rm max}$, etc. from models rather than by simply extrapolating the measured plot. In [42], we have fit the model described in Fig. 2 to determine $f_{\rm max}$ and f_T for the 10×1 μm/56 nm BC device at a $J = 0.56$ mA/μm and the results are consistent with those presented here.

Recently, the author of [43] has reported an $f_{\rm max}$ of 430 GHz in this technology for an FB 20×0.4 μm/41-nm N-channel field-effect transistor (NFET) device deembedded up to the gate and the drain's first metal contact. This finger width is not available in the PDK. Furthermore, the parasitic inductance, capacitance, and resistance of the gate and drain vias and interconnects have a significant impact on the device $f_{\rm max}$. The authors of [32] have reported an $f_{\rm max}$ of 200 ± 5 GHz at a current density (J) of 0.2–0.5 mA/μm for a 30×1 μm/40-nm FB device referenced to the top of the drain and gate vias. The *gate-over-device* layout used in this work enables a symmetric doubly contacted gate, and thus allows us to achieve a higher $f_{\rm max}$ of 250 GHz for FB devices, and a similar $f_{\rm max}$ of about 200 GHz for the slower BC devices. To put this into perspective, in [26], the author has constructed an oscillator with a fundamental frequency of 300 GHz in the TSMC 65-nm CMOS technology. Consequently, the $f_{\rm max}$ of this technology is at least greater than 300 GHz.

B. Transmission Line

The inductors in our design are implemented with high characteristic impedance transmission lines. There are no accurate models in the PDK for transmission lines. Consequently, they are simulated in IE3D. Fig. 4 shows the measured characteristics of a test coplanar waveguide (CPW). We implement most of the transmission lines as CPWs for two reasons, which are: 1) it minimizes interference with nearby components and 2) the metal density in the side-shield vias helps meet metal-fill requirements. The CPW's 7.5-μm-wide signal line is in the 2.1-μm-thick top aluminium layer (LB). A ground plane approximately 6.96 μm below the signal layer is formed by tying the three bottom-most copper layers ($M1$, $M2$, and $M3$) to reduce loss. The metal thicknesses are 0.136, 0.144, and 0.144μm, respectively, and the distances between $M1$ and $M2$, and $M2$ and $M3$ are both 0.115 μm. The side ground shields at a separation of 12.5 μm from the signal line are formed by tying the top layer in LB to the ground plane through a metal and via pattern designed to satisfy metal fill requirements. A characteristic impedance of $Z_c = 70$ Ω is seen as expected from simulation. The wavelength λ and attenuation constant α also match up well with simulation up to 65 GHz. However, as indicated in [32], [44], and [45], the authors have documented an increase in transmission line loss beyond 100 GHz that is not captured in EM simulations. EM simulations predict an α of -1.17 dB/mm at 200 GHz and -1.78 dB/mm at 300 GHz for this line.

C. Capacitor Vertical Natural Capacitor (VNCAP)

In this PDK, the VNCAP, also known as metal–oxide–metal (MOM) or finger capacitor, is available. To test the performance and the accuracy of models for these capacitors, we implemented test structures for 70- and 214-fF VNCAPs. They are implemented between the metals $M3$ and $B3$. The capacitors, like the transmission line and devices, were deembedded using the open-short technique.

The PDK model for the capacitor is only valid when it is contacted at the centre of the bottom-most metal $M3$ for both plates.

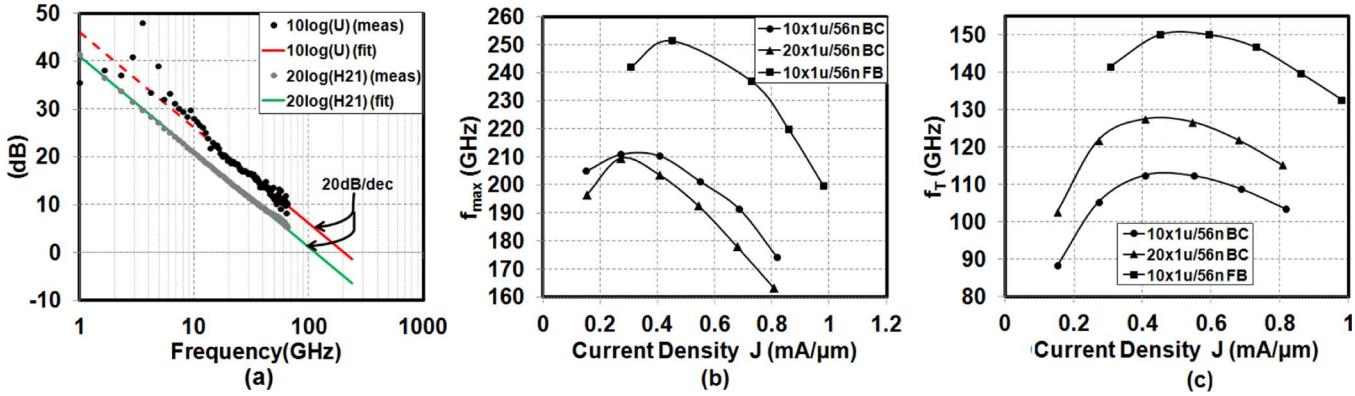

Fig. 3. (a) Line fitted by linear regression to the measured U and h_{21} plots of the 10×1 μm/56 nm BC device with a $J = 0.56$ mA/μm. (b) Comparison of the $f_{\max}$ across J from measurement for the 10×1 μm/56 nm and 20×1 μm/56-nm BC devices and the 10×1 μm/40-nm FB device. (c) Measured f_T across J for all three devices.

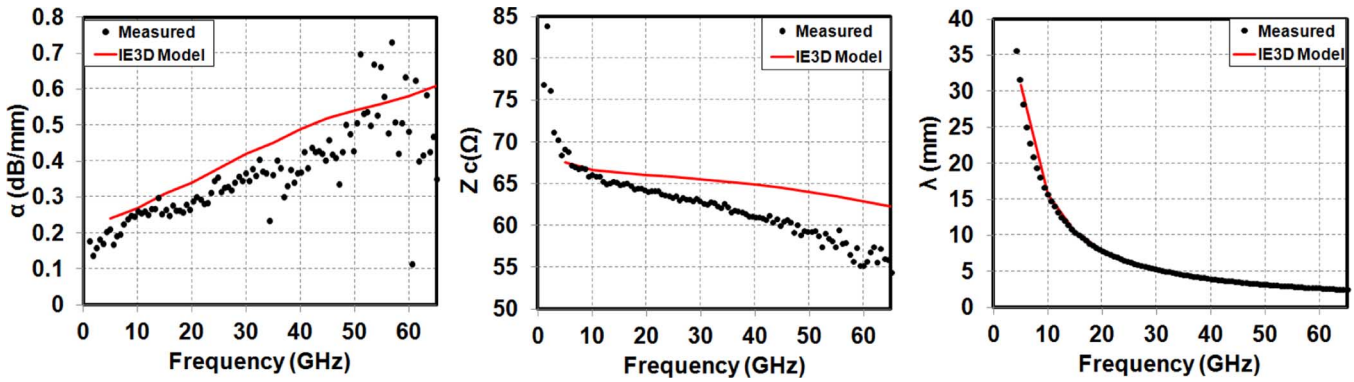

Fig. 4. Measured performance of a 70-Ω CPW in 45-nm SOI CMOS. A comparison with the simulated performance in IE3D is also shown.

In our work, the signals are in the topmost aluminium LB layer and we construct a via to contact the capacitor plates at B3. The deembedding reference plane is placed at the top of the LB via in the test structures. Both capacitors are modeled [see Fig. 5(a)] by augmenting the PDK capacitor with series inductance and resistance on either plate (5.9 pH and 0.5 Ω for the 214-fF capacitor, and 7 pH and 2 Ω for the 70-fF capacitor). This captures the effect of the via's resistance and inductance on the quality factor and self resonance, as well as any series inductance unmodeled in the PDK. The two via inductances are also mutually coupled with a k of 0.7 for both. The smaller capacitor and its vias are also modeled with IE3D [see Fig. 5(b)]. The IE3D model needs to be augmented with 4 pH and 2 Ω on either plate. This is possibly because the vias internal and external to the VNCAP are modeled as continuous bars in IE3D as the simulation of discrete vias is too cumbersome. We show a comparison between the measured performance and the models in Fig. 6. The 214- and 70-fF capacitors have self resonance frequencies of 80 and 115 GHz, respectively, indicating that they are actually inductive at the frequency of interest.

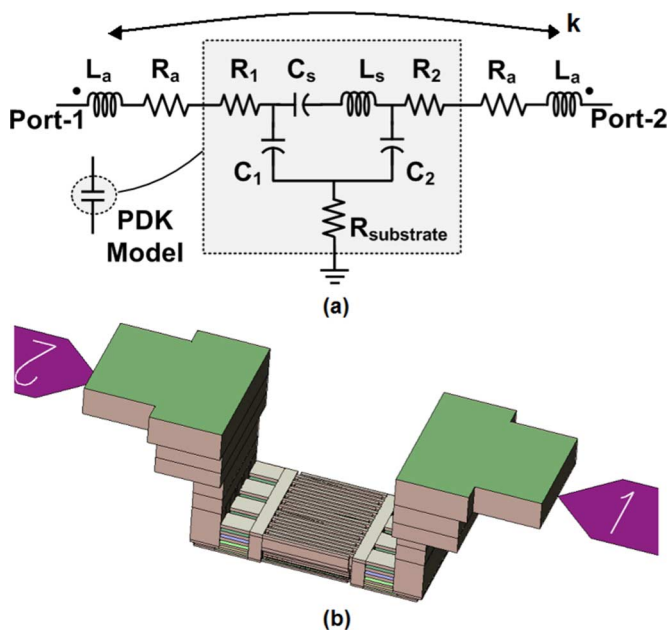

Fig. 5. (a) Model used for the VNCAP in 45-nm SOI CMOS. La and Ra are added to capture the via effect and the inductances on either plate are coupled. (b) IE3D VNCAP simulation setup.

III. MGRO Topology

While oscillators are large-signal circuits, small-signal concepts of $f_{\max}$ and maximum PG are relevant to compute the startup gain of an oscillator topology and consequently its maximum oscillation frequency.

The conventional way in which high-frequency CMOS oscillators are built is the XCO topology [see Fig. 7(a)]. The XCO

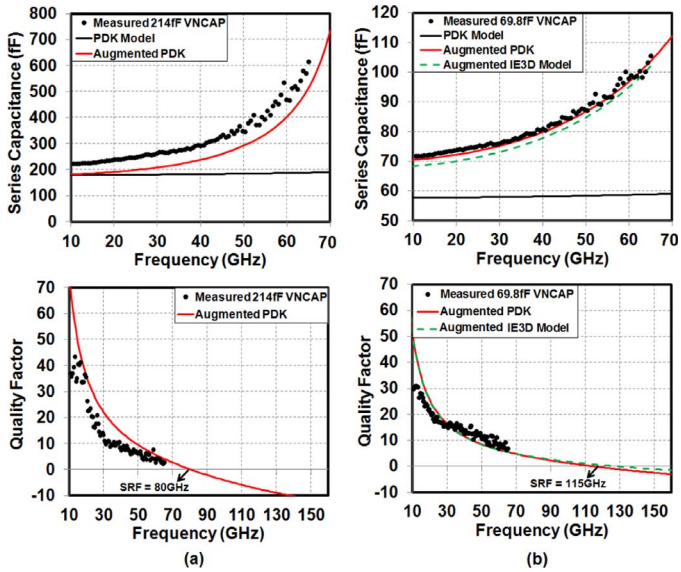

Fig. 6. Measured and simulated series capacitance ($= \mathrm{Im}y_{11}/\omega$) and quality factor ($= \mathrm{Im}(y_{11})/\mathrm{Re}(y_{11})$) of a: (a) 214- and (b) 70-fF VNCAP in 45-nm SOI CMOS.

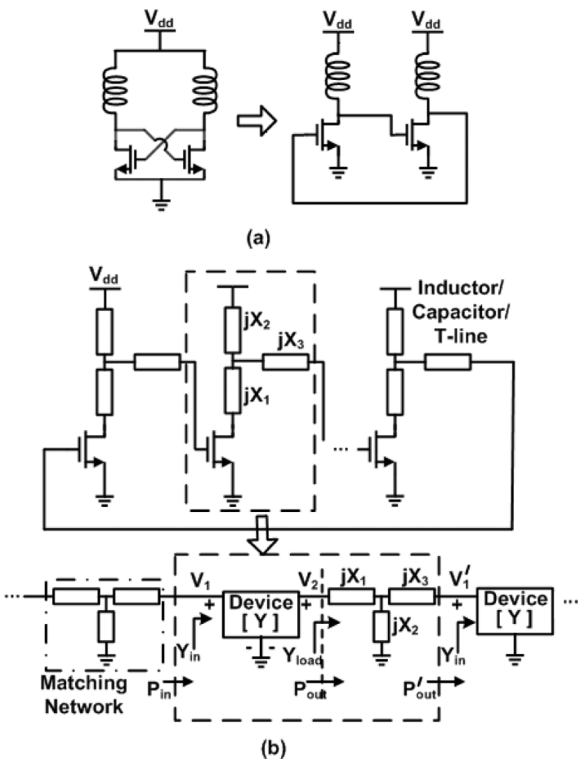

Fig. 7. (a) Cross-coupled oscillator as a two-stage tuned ring oscillator with a single inter-stage matching inductor. (b) MGRO concept.

may be viewed as a ring of two tuned amplifiers with a single effective inductor acting as the matching component between the amplifiers. This is insufficient to convert the input impedance of the second amplifier to the conjugately matched load impedance needed by the first to deliver the maximum available power gain (MAG), [46] and [47]. Consequently, the XCO achieves suboptimal PG and can be expected to exhibit a maximum oscillation frequency that is below the $f_{\max}$ of the technology. The MGRO, as shown in Fig. 7(b), rectifies the matching problem by including additional reactive components in the matching network between the stages. If the Y-parameters of each device are represented by $[\mathbf{Y}]$ with $Y_{ij} = G_{ij} + jB_{ij}$,

$$Y_{\mathrm{in}} = \frac{1}{Z_{\mathrm{in}}} = Y_{11} + G_v Y_{12} \tag{1}$$

$$Y_{\mathrm{load}} = \frac{1}{Z_{\mathrm{load}}} = -\left(\frac{Y_{21}}{G_v} + Y_{22}\right) \tag{2}$$

$$\begin{aligned} \mathrm{PG} &= \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} \\ &= \frac{|G_v|^2 \mathrm{Re}(Y_{\mathrm{load}})}{\mathrm{Re}(Y_{\mathrm{in}})} \\ &= \frac{-\left((A_v^2 + B_v^2)G_{22} + A_v G_{21} + B_v B_{21}\right)}{(G_{11} + A_v G_{12} - B_v B_{12})} \end{aligned} \tag{3}$$

where $G_v = v_2/v_1 = A_v + jB_v$ is the voltage gain across the device. P_{in} is the power flowing into the gate (port 1) of the device, P_{out} is the power delivered out of the drain (port 2), and P'_{out} is the power delivered after the matching network.[1] Y_{in} is the input impedance of the device and Y_{load} is the impedance to which the input impedance of the subsequent stage is transformed by the matching network. In the absence of passive loss, $P'_{\mathrm{out}} = P_{\mathrm{out}}$, and hence, device PG, and consequently, oscillator startup gain, can be maximized by determining the complex G_v value that maximizes PG in (3) to MAG. This may be performed either analytically or numerically if the device Y-parameters are known. Fig. 8 depicts PG circles on the real-imaginary plane of G_v at 100 GHz for a 10×1 μm/56-nm BC nMOS device including layout parasitics for a current density of $J = 0.56$ mA/μm. The maximum achievable PG is 3.3 dB. Once the optimal G_v is known, the matching network can be designed to transform Y_{in} to the requisite Y_{load}. It is evident that the maximum oscillation frequency of this methodology, namely the highest frequency at which the PG maximized to the MAG crosses 0 dB, is the $f_{\max}$ of the device.

At lower frequencies, there exist regions of the contour plot where $P_{\mathrm{in}} < 0$ and $P_{\mathrm{out}} > 0$. The circular area where $P_{\mathrm{out}} > 0$ extends below the $P_{\mathrm{in}} = 0$ line. In such regions, the device "self-oscillates." In other words, with the appropriate source and load terminations, the internal C_{gd} feedback of the device is sufficient to cause oscillation. Such behavior disappears as the frequency approaches a higher fraction of $f_{\max}$.

A. Accounting for Passive Element Loss

When the passive matching components contain loss, the maximum oscillation frequency will be lower than $f_{\max}$ and the optimal G_v value might change. Furthermore, additional guidelines are required for the design of the matching network in such a case. We can use Foster's second theorem to arrive at the following expressions [48]:

$$Y_{\mathrm{load}} = \frac{2P_{\mathrm{out}} + 4j\omega(E_{E,Y_{\mathrm{in}}} + E_{E,M} - E_{H,Y_{\mathrm{in}}} - E_{H,M})}{|G_v v_1|^2} \tag{4}$$

[1]This formulation and the developed design methodology is general and can be used for device configurations other than common source, or even configurations involving multiple devices.

where $E_{E,M}$ and $E_{H,M}$ are the stored electric and magnetic energies in the matching network, respectively. $E_{E,Y_{\rm in}}$ and $E_{H,Y_{\rm in}}$ are the stored electric and magnetic energies in the looking-in impedance of the subsequent stage, which from Fig. 7 is $Y_{\rm in}$. $P_{\rm out}$ is the total loss in $Y_{\rm load}$, and is a sum of the losses in the matching network ($P_{{\rm loss},M}$) and the subsequent stage ($P'_{\rm out}$)

$$P_{\rm out} = P_{{\rm loss},M} + P'_{\rm out}. \tag{5}$$

Assuming that the matching network may be constructed with inductors and capacitors of quality factors Q_L and Q_C, respectively, the total loss in the matching network is

$$P_{{\rm loss},M} = 2\omega\frac{E_{H,M}}{Q_L} + 2\omega\frac{E_{E,M}}{Q_C}. \tag{6}$$

Also, the loss and the stored energies in $Y_{\rm in}$ of the subsequent stage are related by the following equations:

$$\begin{aligned} Y_{\rm in} &= \frac{2P_{out'} + 4j\omega(E_{E,Y_{\rm in}} - E_{H,Y_{\rm in}})}{|v'_1|^2} \\ |v'_1|^2 &= \frac{2P'_{\rm out}}{{\rm Re}(Y_{\rm in})} \\ (E_{E,Y_{\rm in}} - E_{H,Y_{\rm in}}) &= \frac{{\rm Im}(Y_{\rm in})}{4\omega} \times \frac{2P'_{\rm out}}{{\rm Re}(Y_{\rm in})}. \end{aligned} \tag{7}$$

Using (6) and (7) in the expression for $Y_{\rm load}$ in (4), we derive an expression for the stored energy in the matching network

$$E_{E,M} - E_{H,M} = \left(\frac{|G_v v_1|^2 {\rm Im}\,(Y_{\rm load})}{4\omega} - \frac{2P'_{\rm out}{\rm Im}\,(Y_{\rm in})}{4\omega{\rm Re}\,(Y_{\rm in})}\right). \tag{8}$$

If the right-hand side (RHS) of (8) is positive, the matching network must store net electric energy; otherwise the net stored energy is magnetic. As shown in (6), $P_{{\rm loss},M} = 2\omega E_{H,M}/Q_L + 2\omega E_{E,M}/Q_C$. If the net stored energy is magnetic, to minimize $P_{{\rm loss},M}$, only inductors should be used. The use of capacitors will require an increase in the stored magnetic energy to compensate for the nonzero $E_{E,M}$. Similarly, if the net stored energy is electric, only capacitors should be used. For MOSFET devices, the matching network must typically store net magnetic energy. Furthermore, all inductor matching networks are preferable because they enable convenient gate and drain biasing, and because the quality factor of inductors at millimeter-wave and sub-millimeter-wave frequencies exceeds that of integrated capacitors. Assuming an all inductor network [setting $E_{E,M} = 0$ in (8)], using the value of $P_{\rm out}$ from (3), and setting $v_1 = 1\angle 0^\circ$ without loss of generality, the net PG including matching network loss can be written as

$$\begin{aligned} P'_{\rm out} &= P_{\rm out} - P_{{\rm loss},M} \\ &= P_{\rm out} - 2\omega\frac{E_{H,M}}{Q_L} \end{aligned} \tag{9}$$

$$\begin{aligned} {\rm PG}' &= \frac{P'_{\rm out}}{P_{\rm in}} \\ &= \frac{|G_v|^2}{2}\left[\frac{Q_L{\rm Re}(Y_{\rm load}) + {\rm Im}(Y_{\rm load})}{Q_L{\rm Re}(Y_{\rm in}) + {\rm Im}(Y_{\rm in})}\right]. \end{aligned} \tag{10}$$

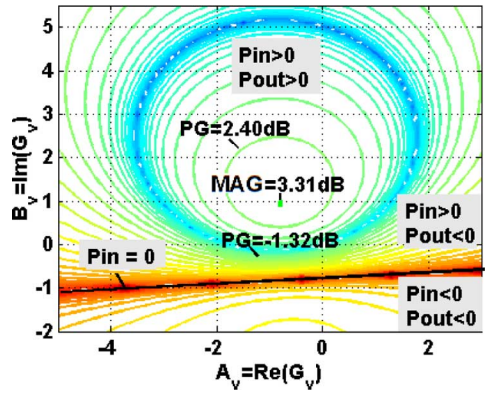

Fig. 8. PG circles on the G_v plane at 100 GHz for a 10×1 μm/56-nm BC nMOS device including estimated layout parasitics in a common source configuration. Current density, $J = 0.56$ mA/μm.

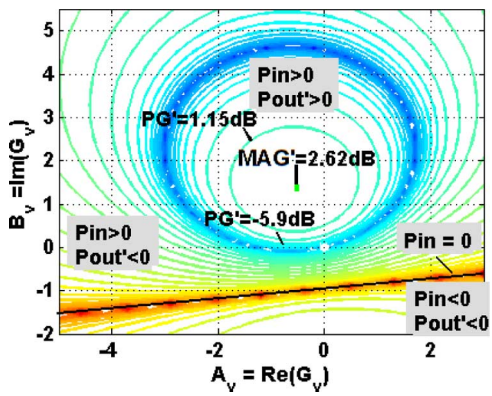

Fig. 9. Power gain (PG′) circles on the G_v plane at 100 GHz for the device in Fig. 8 with Inductor quality factor taken to be 14 at 100 GHz. Current density, $J = 0.56$ mA/μm.

Oscillator startup gain is now maximized by determining the G_v value that maximizes PG′ in (10) to MAG′ while restricting oneself to G_v values that result in net stored magnetic energy. MAG′ is the value of the device MAG when it is conjugately matched using lossy inductors. This is the first time that closed-form design guidelines that maximize startup gain in the presence of passive loss have been derived. MAG′ can be thought of as a new technology metric that quantifies achievable device PG in a ring-oscillator configuration taking into account active *and* passive device limitations. It is interesting that for such matching networks employing only inductors, $P_{\rm loss}$, and consequently, PG′ and MAG′ are independent of network topology (L-match, pi-match, etc.) or number of inductors, but only depend on Q_L. PG′ contour plots similar to Fig. 8 have been plotted to maximize PG′ with respect to G_v in Fig. 9.

Fig. 10(a) depicts the MAG′ of the 10×1 μm/56-nm BC nMOS device (including layout parasitics) versus frequency for different Q_L values. The annotated Q_L values are for a frequency of 100 GHz, and Q_L is assumed to scale linearly with frequency. Fig. 10(b) depicts the maximum oscillation frequency (namely, the frequencies at which MAG′ = 1) of the MGRO topology as a function of Q_L, and compares it with the simulated maximum oscillation frequency of the conventional XCO topology. A significant enhancement is observed.

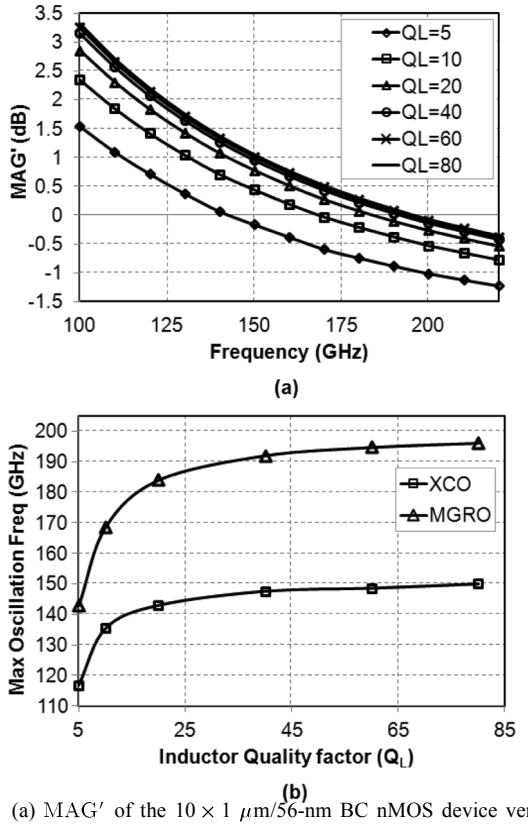

Fig. 10. (a) MAG' of the 10×1 μm/56-nm BC nMOS device versus frequency for different Q_L values. The annotated Q_L values are for a frequency of 100 GHz, and Q_L is assumed to scale linearly with frequency. (b) Maximum oscillation frequencies of the device in the MGRO and XCO topologies as a function of Q_L.

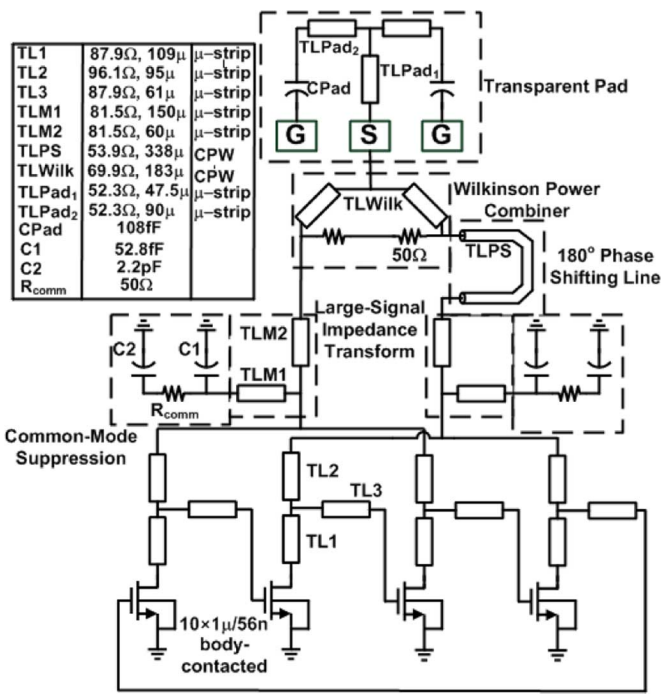

Fig. 11. Circuit diagram of the 216-GHz signal source.

B. Determining the Matching Network

While the discussion thus far has focused on maximizing PG for startup, the total phase shift in the ring must also equal an integral multiple of 2π at the desired frequency. While two reactances are sufficient to achieve the impedance transformation for optimal G_v, a third reactance is required to arbitrarily control the phase shift ϕ across a stage. This allows flexibility in the number of stages N ($N\phi = 2n\pi, n \in Z$), allowing freedom in choosing the harmonic to be extracted. Assuming a T matching network as shown in Fig. 7, the three matching reactances X_1, X_2, and X_3 may be determined using the following expressions[2]:

$$\frac{[(\mathrm{Re}(Z_{\mathrm{in}}) + j\mathrm{Im}(Z_{\mathrm{in}})) + jX_3]\, jX_2}{(\mathrm{Re}(Z_{\mathrm{in}}) + j\mathrm{Im}(Z_{\mathrm{in}})) + jX_3 + jX_2} + jX_1 = Z_{\mathrm{load}} \quad (11)$$

$$\angle\left[(G_v Y_{\mathrm{load}})\, \frac{jX_2}{jX_2 + (jX_3 + Z_{\mathrm{in}})} \times Z_{\mathrm{in}}\right] = \phi. \quad (12)$$

The requirement for X_1, X_2, and X_3 to be positive (all-inductor matching network) does place some restrictions on ϕ. This, however, need not restrict our choice of the harmonic to be extracted, as discussed in Section IV-A.

In practice, at high-millimeter-wave and terahertz frequencies, these inductors would be implemented using transmission lines, which, in general, do not behave as pure two-port reactances. This deviation from the purely inductive assumption can be minimized by choosing transmission lines with high characteristic impedance (e.g., microstrips with small widths). The tradeoff is that narrow microstrips exhibit poor Q_L. Alternately, the equations above can be modified appropriately to capture transmission-line behavior of the three matching components.

The authors in [29] attempt to maximize startup by maximizing the added power ($P_{\mathrm{added}} = P_{\mathrm{out}} - P_{\mathrm{in}}$) per stage. In comparison, our work provides simple expressions, as opposed to an iterative procedure, to arrive at the interstage passive network required to achieve the maximum small-signal gain. Our methodology also allows any desired phase shift per stage, allowing flexibility in the number of stages in the ring and the harmonic to be extracted. Our analysis also includes the effect of passive loss on the maximum achievable fundamental oscillation frequency.

C. Circuit-Level Implementation

Using the theory discussed, we have implemented a 108- and 158-GHz oscillator in the 45-nm SOI CMOS process. By the contour plotting technique, a 10×1 μm/56-nm BC device, including layout parasitics, has a maximum startup gain of 2.62 dB at 100 GHz in the presence of passive loss, and 0.62 dB at 150 GHz (with $Q_L = 14$ at 100 GHz). It is to the credit of the technique described that the latter oscillator works well in measurement despite the marginal small-signal gain.

With G_v for maximum PG thus determined, Y_{in} and Y_{load} can be calculated. We now solve (11) and (12) with different values of $\phi = 360/m^\circ$ ($m \in Z$) until we get positive values of X_1, X_2, and X_3. $\phi = 90^\circ$ gives a purely inductive matching network, but $\phi = 180^\circ$ does not. Consequently, we implemented a four-stage oscillator. The choices of phase and number of stages made here are formalized in Section IV. To extract the second harmonic, we combine every second stage at the top of X_2, as shown in Figs. 11 and 12, to create virtual grounds for the

[2]Closed-form solutions are also available.

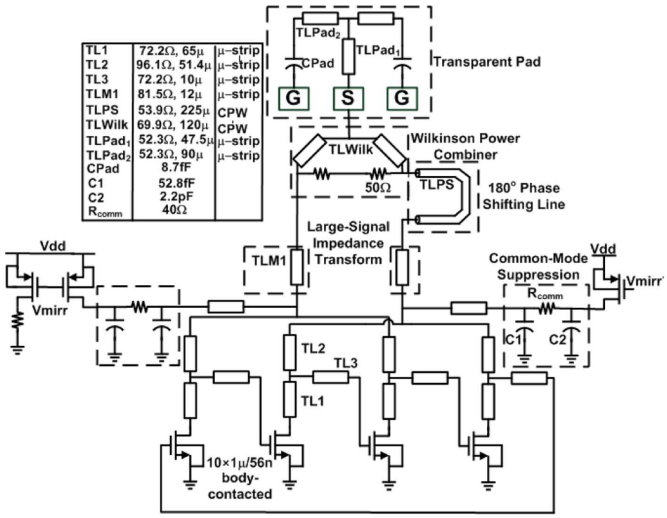

Fig. 12. Circuit diagram of the 316-GHz signal source.

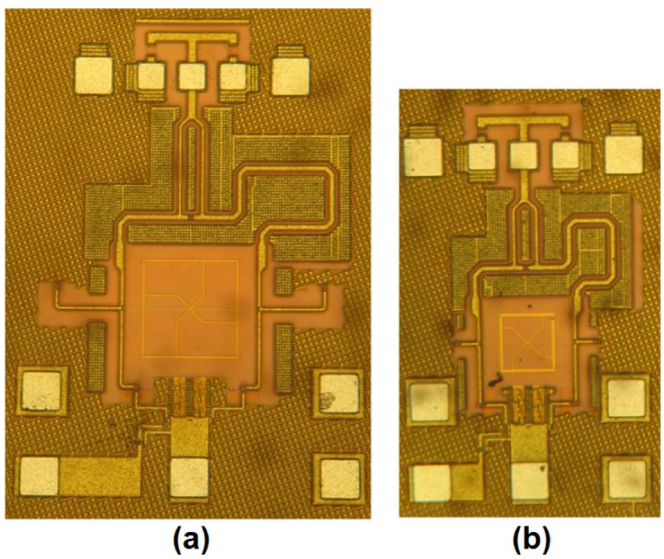

Fig. 13. Chip microphotographs of the: (a) 216- and (b) 316-GHz signal sources.

fundamental signal. This yields two outputs 180° out-of-phase at the second harmonic. Ignoring the box labeled *Large Signal Impedance Transformation* for now, they are phase shifted as shown and combined using a Wilkinson combiner. The bias for the 108-GHz oscillator is provided through the bias-tee of the probe. The bias for the 158-GHz oscillator is provided by the mirrored current source isolated in ac through the $\lambda/4$ (at 300 GHz) transmission line.

The chip microphotographs are shown in Fig. 13. The 216-GHz signal source occupies 0.83 mm × 0.63 mm of chip area, and the 316-GHz source occupies 0.75 mm × 0.45 mm.

IV. Harmonic Power Extraction and Spurious-Mode Suppression

Signals beyond $f_{\max}$ must be derived by harmonic extraction. In this section, we look at the relationship between power extraction at a desired harmonic and the design of the MGRO and the harmonic extraction network. As discussed in Section

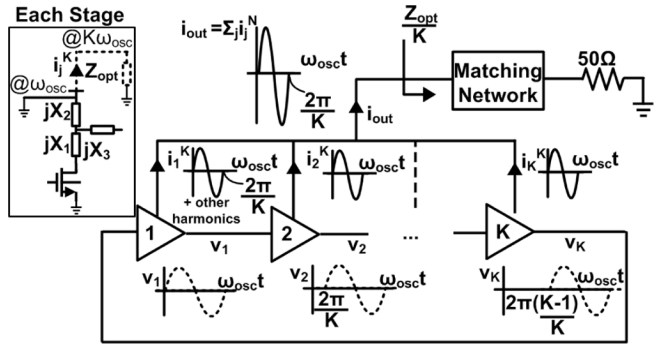

Fig. 14. Ring oscillator with K-stages to extract the Kth harmonic.

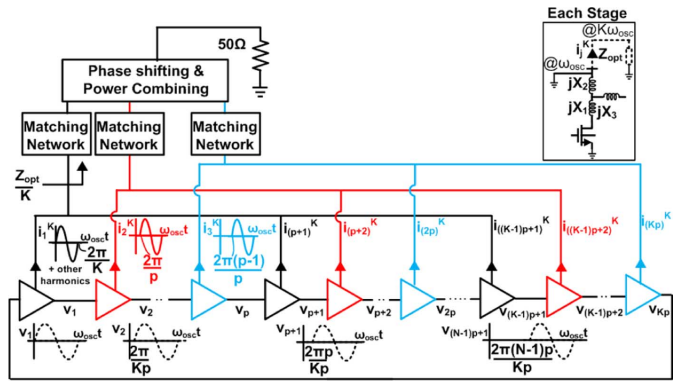

Fig. 15. Ring oscillator with $K \times p$-stages to extract the Kth harmonic. $\phi = 2\pi/K \times p$ to ensure an inductive matching network.

III, a key consideration in determining the number of stages remains the feasibility of obtaining a per-stage phase shift, which allows for an inductive matching network. The presence of too many stages encourages spurious oscillations as any frequency at which the total phase shift through the loop is a multiple of 2π is a potential mode [49]. These concerns need to be taken into account when choosing the number of stages, the harmonic to be extracted, and while designing the extraction network. The harmonic power delivered to the load can be optimized by using large-signal impedance-transforming and power-combining networks. Loss in the extraction networks must also be accounted for. Depending on the number of stages used, filtering may also be required to remove other harmonics that flow into the extraction network.

A. Extracting the Kth Harmonic

To extract the Kth harmonic from an MGRO, K-stages with a per-stage phase shift of $\phi = 2\pi/K$ can be used. All the nodes above the X_2 impedance are joined together as shown in Fig. 14. Any other lower harmonics would get suppressed in the extraction path. If $\phi = 2\pi/K$ does not yield a purely inductive interstage matching network, we could implement a per-stage phase shift of $\phi = 2m\pi/K$ $(m \epsilon \mathbf{Z})$ more amenable to this requirement in the K-stage ring. However, lower harmonics would not be inherently suppressed in the extraction path, and filtering would be required. We could also extract the Kth harmonic of a K/m-stage oscillator with a per-stage phase shift of $2m\pi/K$. All the stages would be tied together above X_2 as before, and the output current would consist of the K/mth harmonic and

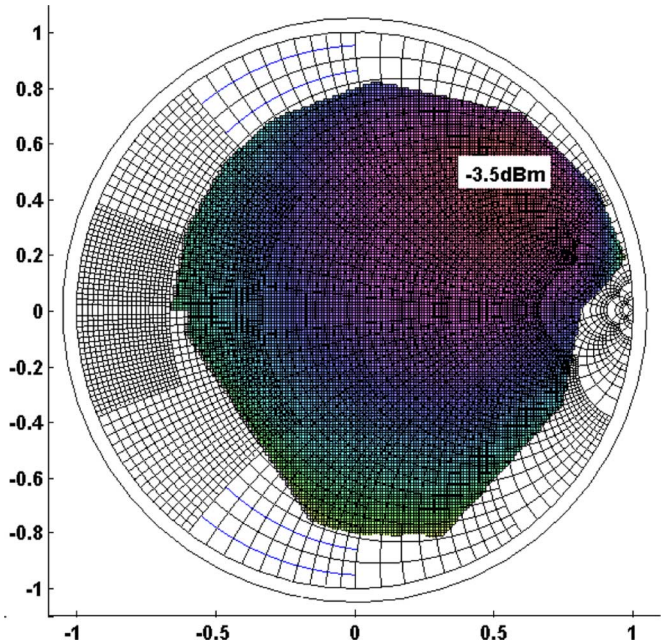

Fig. 16. Load–pull plot of the $K = 2$, $p = 2$ oscillator at 100 GHz.

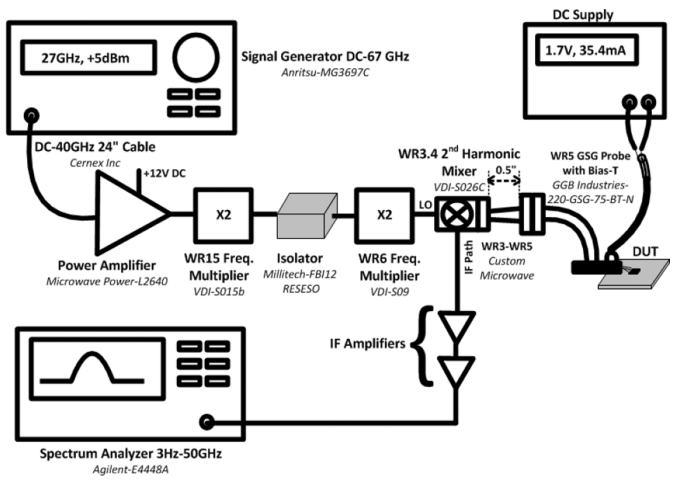

Fig. 17. 216-GHz oscillator frequency and power measurement setup with WR-3 second-harmonic mixer-downconverter (SHMD).

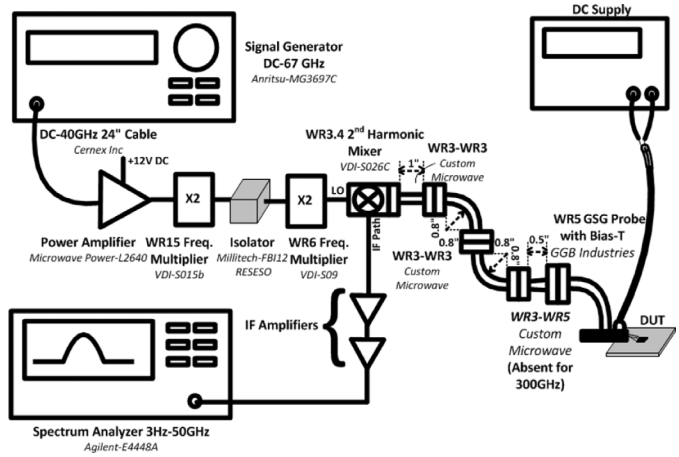

Fig. 18. 216-GHz oscillator frequency and power measurement setup with WR-3 SHMD including two additional WR3 bends and one additional WR3 straight. This measurement is to measure the loss of the latter three components.

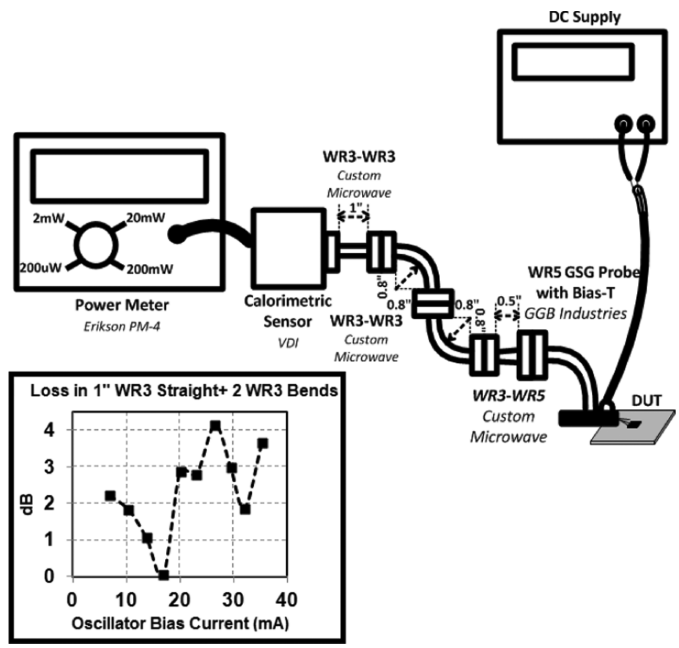

Fig. 19. Power meter measurement setup for the 216-GHz oscillator. The inset shows the measured loss of the additional two WR3 bends and the 1-in WR3 straight. Details are provided in the text.

its multiples. Once again, we would need a filter to reject all but the desired multiple. The advantage of this approach is that the ring is smaller and susceptible to fewer spurious modes.

If we need to reduce the ϕ below $2\pi/K$ to satisfy the inductive network requirements, but would like to avoid filtering of unwanted harmonics, we can extract the Kth harmonic from a $K \times p$-stage oscillator, as shown in Fig. 15, with a per-stage phase shift of $\phi = 2\pi/K \times p$. Every pth stage is joined, yielding p outputs carrying current at the Kth harmonic and separated in phase by $2\pi/p$. Appropriate phase-shifting networks are placed in each of the K paths before power combining. The increase in the number of stages in the ring does render it more susceptible to spurious modes, but these can be suppressed through the judicious introduction of loss in the extraction path without affecting the power of the desired harmonic, as is discussed later in this section. The phase-shifting and power-combining networks do introduce additional loss that must be taken into consideration. This approach has been exploited in the implemented prototypes described earlier. The second harmonic $(K = 2)$ has been extracted from a four-stage MGRO $(p = 2)$, yielding a per-stage phase shift of 90°, which satisfies the inductive matching network requirement.

B. Increasing the Output Power

To increase the ouput power in the aforementioned approaches, we could increase the number of elements in the ring while maintaining the same phase shift. Such an implementation is more susceptible to spurious modes because of the larger number of elements in the ring. Instead, we can also synchronize multiple MGROs and combine them on chip. To avoid the losses of an on chip power-combining network, we could also

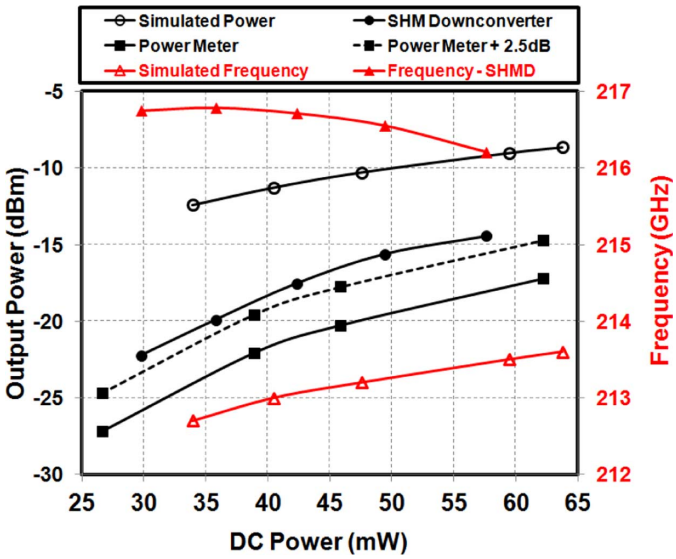

Fig. 20. 216-GHz oscillator frequency and power measured by a WR-3 SHMD and an Erickson PM4 power meter. Measurement details are in the text.

combine multiple synchronized MGROs through free-space power combining, as in [27]. This would, of course, require the interfacing of the synchronized MGROs with on-chip/off-chip antennas.

C. Maximizing the Harmonic Output Power

We now show that each stage of an MGRO needs an optimal output impedance $Z_{\rm opt}$ at the Kth harmonic, as shown in the inset of Figs. 14 and 15, to facilitiate maximum power transfer. This value is determined through load–pull simulations. For the implemented MGRO, we place an impedance transformation network composed of transmission lines that converts 50 Ω to the optimal impedance for each of the two outputs. This network is inside the box marked *Large Signal Impedance Transform* in Figs. 11 and 12. A load–pull plot of the power as a function of transformed optimal impedance is shown in Fig. 16. The peak value is different from the simulated value in Fig. 20 in Section V by 11 dB. This difference is due to the loss in the matching network, phase shifting line, combiner, and transparent pads.

Changing the number of elements in the ring while maintaining the phase shift (and hence, the design of each stage) causes the overall optimal impedance to scale inversely due to the parallel combination of the harmonic currents produced by each stage. $Z_{\rm opt}$ also scales inversely with device size, as is the case in all power-generating circuits. To minimize loss in the large-signal impedance transformation network, device size and MGRO parameters should be chosen so that the overall optimal impedance is as close to 50 Ω as possible.

D. Suppression of Spurious Modes

Reducing the number of stages in the oscillator might not curtail all spurious modes. The harmonic extraction network is normally not seen by the fundamental oscillation as it exists in the common-mode path. However, the phase shifts in some spurious modes may cause the harmonic extraction network to appear appended to the inter-stage passive matching network.

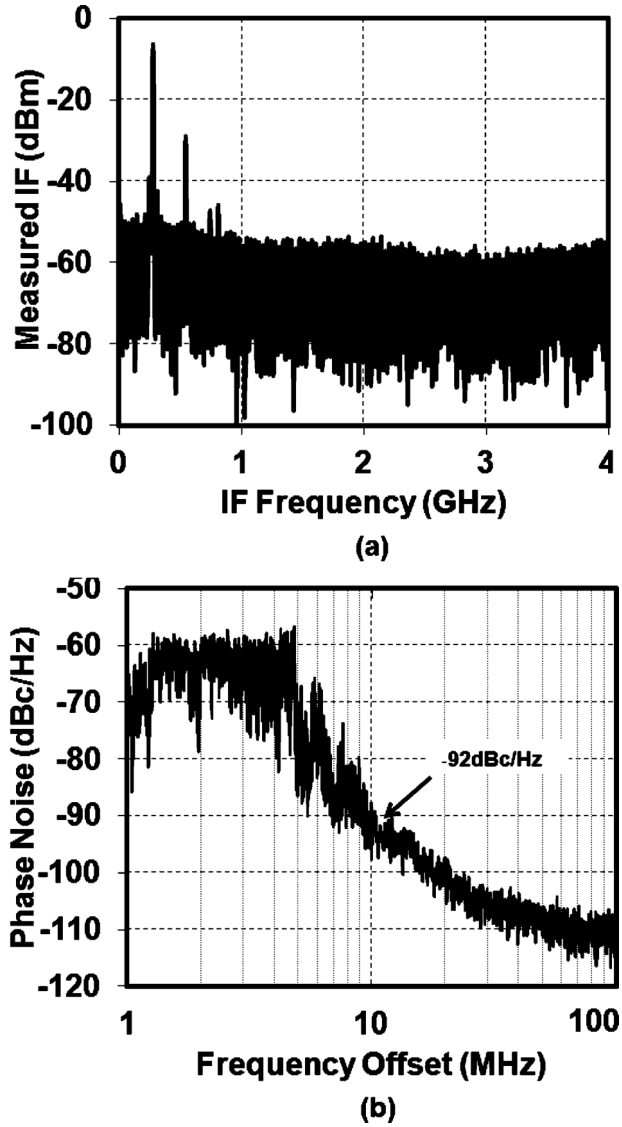

Fig. 21. (a) Measured downconverted spectrum of the 216-GHz source for a dc power of 57.5 mW, output frequency of 216.2 GHz, and calibrated output power of −14.4 dBm. (b) Measured phase noise.

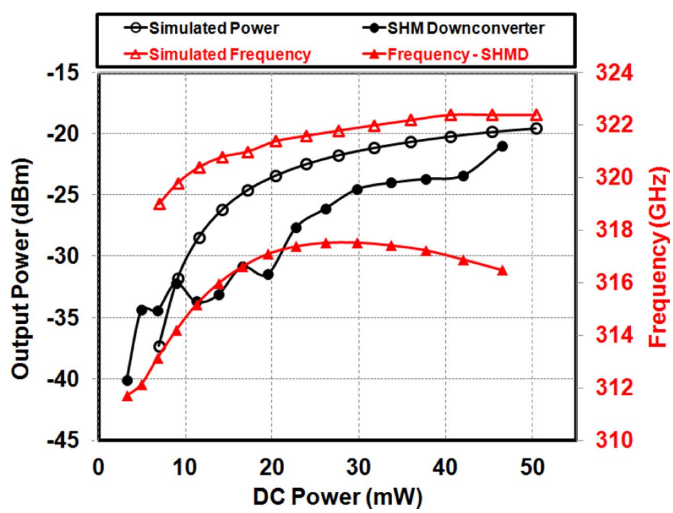

Fig. 22. 316-GHz oscillator frequency and output power measured using the WR3 SHMD.

These modes can be eliminated by the judicious placement of suppression resistors in the extraction network such that they

TABLE I
COMPARISON OF REPORTED CMOS-BASED SOURCES OPERATING ABOVE 200 GHz

Ref.	Tech.	Est. f_{max}	f_{osc}(GHz)	f_{out} (GHz)	P_{out}(dBm)	P. Noise (dBc/Hz)	P_{DC}(mW)
[26]	65nm	>300	300.5	300.5	N/A	N/A	3.7
[24]	90nm	N/A	81	324	-46	-91@10MHz	12
[23]	45nm	N/A	205	410	-49 (radiated)	N/A	N/A
[25]	45nm	N/A	133.3	533	-36.5	N/A	64
[51]	130nm	N/A	96	192	-20	-100@10MHz	16.5
[29]	130nm	135	128	256	-17	-88@1MHz	71
[27]	45nm-SOI (40nm FB NMOS)	>250 (our measurements)	150	300	-10.9(2×2array) (EIRP=-1)	NA	74.8
[28]	45nm-SOI (40nm FB NMOS)	>250 (our measurements)	90.2-98.5	276-285 (3.2%)	-7.2(4×4array) (EIRP=9.4)	NA	817
[29]	65nm	>300 [26]	160.7	482	-7.9	-76@1MHz	61
[30]	65nm	>300 [26]	70.8-74	283-296 (4.4%)	-1.2@290GHz	-78@1MHz	325
[31]	90nm	175	72.5-77.7	217.5-233.3 (7%)	-6.5@228GHz	-90.5@1MHz	86.4
is work	45nm-SOI (56nm BC NMOS)	200 (our measurements)	108.1	216.2	-14.4	-93@10MHz	57.5
is work	45nm-SOI (56nm BC NMOS)	200 (our measurements)	158.3	316.5	-21	NA	46.4

do not appear in the signal path. To this end, we have placed the R–C networks in the box labeled *Common-Mode Suppression* in Figs. 11 and 12.

V. OSCILLATOR MEASUREMENT

The signal sources are tested in chip-on-board configuration through on-chip probing. We first discuss the measurement of the 216-GHz oscillator. The setup is shown in Fig. 17. A GGB WR-5 probe was used in conjunction with a 200–320-GHz WR-3 SHMD from Virginia Diodes Inc. through a WR5-WR3 taper. Supply is provided through the bias-T of the probe. The WR-3 mixer comprises a second-harmonic mixer and a local oscillator (LO) amplifier chain that multiplies a 25–40-GHz input by a factor of 4. The value of the probe loss is determined at about 2.5 dB from the measured data provided by GGB. The measured conversion loss of the downconverter falls from 10.5 to 8.8 dB over 212–220 GHz. The signal at the IF port is small and so two amplifiers are placed in the IF path. The total loss of the amplifiers, cables, and connectors in the IF path is measured in a separate setup. The measured oscillation frequency and calibrated output power of the source is depicted in Fig. 20. The oscillator generates -14.4 dBm of power at 216.2 GHz while drawing 57.5 mW of dc power. The downconverted spectrum at this power level is depicted in Fig. 21. A phase-noise measurement of the 216-GHz oscillator is performed by measuring the phase noise of the downconverted IF spectrum, yielding -92 dBc/Hz at an offset of 10 MHz. A phase-noise analysis of tuned ring oscillators has been quantified in [50]. A phase-noise analysis of MGROs as they approach $f_{\max}$ in operation frequency is an interesting topic for future research.

We verify these results through a power meter measurement in the configuration shown in Fig. 19. The power meter setup requires some additional waveguide components, the losses of which are now discussed. The loss of the 1-in WR10-WR10 straight and the 1-in WR3-WR10 taper are measured by VDI at 0.2 and 0.35 dB, respectively. Only the two WR3 bends and the 1-in WR3 straight losses remain unknown. Custom Microwave predicts their total loss at 0.4 dB/in. Assuming negligible reflections, we determine their loss by adding them to the WR3 mixer-downconverter measurement setup, as shown in Fig. 18. The difference between the measured value in this setup with and without the three components is shown as an inset in Fig. 19. The average value is 2.5 dB. These losses are corrected for in the power-meter measurement to obtain the other two curves in Fig. 20. A close match is seen between the power measured by the SHMD and the power meter verifying the accuracy of the mixer downconversion and its linearity with respect to the RF port.

Next, we measure the 316-GHz oscillator using the same SHMD in the configuration of Fig. 18, but eliminate the WR3-WR5 taper as a WR3 probe is used. The measured frequency and power are shown in Fig. 22. A very good match to the simulated power and frequency is seen. A maximum power of -21 dBm is measured at 316.5 GHz while drawing a dc power of 46.4 mW.

A comparison of recent works is shown in Table I. $f_{\max}$ is strongly dependent on the device layout and may vary from one implementation to another even when designed using the same technology. However, in this table, we have indicated some $f_{\max}$ values from our own measurements and those reported in previous works to facilitate a judicious comparison. While the techniques described in this paper enable the functioning of the implemented oscillators at frequencies close to the limits dictated by active and passive device characteristics, several techniques discussed earlier can be exploited to further increase output power. The use of the 40-nm FB devices would improve performance. As was discussed earlier, the losses in the large-signal impedance transformation network, phase-shifting line, and Wilkinson power combiner are substantial (as high as 11 dB in the 200-GHz prototype). The phase-shifting line and Wilkinson combiner are necessitated by the choice of a four-element ring with 90° per-stage phase shift. Through appropriate device sizing and MGRO design (number of stages and phase shift through each stage), these losses can be eliminated.

VI. CONCLUSION

A MGRO topology that maximizes small-signal gain per stage to the MAG through inter-stage matching and also takes into account passive loss has been presented. The topology also

affords freedom in choosing the number of stages while satisfying the MAG condition. The robustness of such an approach is verified through the implementation of 108- and 158-GHz oscillators using the 56-nm BC devices ($f_{\max} \approx 200$ GHz) of IBM's 45-nm SOI CMOS technology with per-stage small-signal gains as low as 2.62 and 0.62 dB, respectively.

Power at frequencies beyond $f_{\max}$ can only be generated by harmonic extraction. The impact of the choice of the output harmonic on the design of the fundamental ring and the extraction network has been looked at in detail. In particular, the second harmonic of the implemented oscillators has been extracted. A network that transforms the output load to an optimal impedance to maximize harmonic power transfer is determined through load–pull simulations, and an on-chip power-combining network that sums the power from multiple stages has been implemented. The oscillators generate -14.4 dBm of output power at 216.2 GHz and -21 dBm of output power at 316.5 GHz while drawing 57.5 and 46.4 mW of dc power, respectively.

Techniques to interface CMOS terahertz sources with on-chip or off-chip radiators and the relative merits of these two approaches remain a point of interest.

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