A 60 GHz CMOS Full-Duplex Transceiver and Link with Polarization-Based Antenna and RF Cancellation

Tolga Dinc, *Student Member, IEEE*, Anandaroop Chakrabarti, *Student Member, IEEE*, and Harish Krishnaswamy, *Member, IEEE*

***Abstract*—This paper presents a fully integrated 60 GHz direct-conversion transceiver in 45 nm SOI CMOS for same-channel full-duplex (FD) wireless communication. FD operation is enabled by a novel polarization-based wideband reconfigurable self-interference cancellation (SIC) technique in the antenna domain. The antenna cancellation can be reconfigured from the IC to combat the variable SI scattering from the environment during in-field operation. A second RF cancellation path with > 30 dB gain control and $> 360^\circ$ phase control from the transmitter (TX) output to the LNA output further suppresses the residual SI to achieve the high levels of required SIC. With antenna and RF cancellation together, a total SI suppression of > 70 dB is achieved over a cancellation bandwidth of 1 GHz and can be maintained in the presence of nearby reflectors. In conjunction with digital SIC (DSIC) implemented in MATLAB, a FD link is demonstrated over 0.7 m with a signal-to-interference-noise-and-distortion ratio (SINDR) of 7.2 dB. To the best of our knowledge, this work achieves the highest integration level among FD transceivers irrespective of the operation frequency and demonstrates the first fully integrated mm-wave FD transceiver front-end and link.**

***Index Terms*—5G, CMOS, full-duplex (FD), millimeter wave, receiver (RX), self-interference (SI), SI cancellation (SIC), transmitter (TX), TX leakage, transceiver, tunable antenna, wideband.**

I. Introduction

In recent years, there have been significant research and commercial efforts toward mm-wave systems-on-chip for a wide range of applications, from short-range high-data-rate communication [1]–[8] and long range point-to-point systems [9]–[11] to vehicular radar [12]–[14] and high-resolution imaging [15]–[17]. These efforts have led to the maturation of silicon-based mm-wave technology.

Same-channel full-duplex, also known as in-band full-duplex (IBFD), is another emergent technology which has gained significant research attention in recent years. We will refer to it as just full-duplex (FD) in this paper. FD aims to double the spectral efficiency immediately in the physical layer over time division-duplexing and frequency division-duplexing systems by *transmitting and receiving simultaneously on the same frequency channel* [18], [19]. Furthermore, FD paves the way for revolutionizing wireless protocol design by eliminating the half-duplex constraint and thus can offer many new benefits in wireless networks, including significant increase in access-layer throughput, collision avoidance, and addressing the hidden node problem [19]. However, the self-interference (SI) from the transmitter (TX) to its own receiver (RX) poses a tremendous fundamental challenge in achieving FD operation. Depending on the application, the SI can be more than a billion times stronger than the desired signal and must be suppressed below the RX noise floor to enable FD operation. In other words, a total SI suppression of 90 dB or more must be achieved across multiple domains-antenna [20]–[25], RF/analog [26]–[29], and digital [18].

Although system-level demonstrations leveraging off-the-shelf components (e.g., [18]) have established the feasibility of FD, research efforts on fully integrated FD transceivers, irrespective of operating frequency, are still in their infancy. Recently, CMOS ICs for FD applications have been demonstrated at low RF frequencies with analog SI cancelers using baseband noise-canceling, duplexing low-noise amplifiers (LNAs) in [29], and frequency flat amplitude/phase control in [28], but exhibit either limited SI power handling [29] or limited cancellation bandwidth [28]. In [26], a CMOS RX with a frequency-domain equalization-based RF canceler achieving wideband SIC has been demonstrated, but the technique is not amenable to mm-wave.

In this paper, we present a fully integrated transceiver merging two exciting technologies, mm-wave and FD, which can potentially offer the dual benefits of wide BWs and improved spectral efficiency. In [30], we reported a 60 GHz fully integrated FD transceiver which employs reconfigurable and wideband polarization-based antenna, RF, and digital cancellation. This paper presents a detailed discussion of the transceiver presented in [30] with extended system analysis, antenna-cancellation tradeoff discussions, circuit descriptions, simulations, and measurements.

This paper is organized as follows. Section II discusses the architecture, focusing on system-level requirements for FD operation. Section III describes the proposed polarization-based antenna cancellation technique and its associated tradeoffs. The circuits in the 60 GHz FD CMOS transceiver are detailed in Section IV. In Section V, we present the measurements of the transceiver and demonstrate an FD wireless link. Section VI concludes this paper.

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The authors are with the Department of Electrical Engineering, Columbia University, New York, NY 10027 USA (e-mail: harish@ee.columbia.edu).

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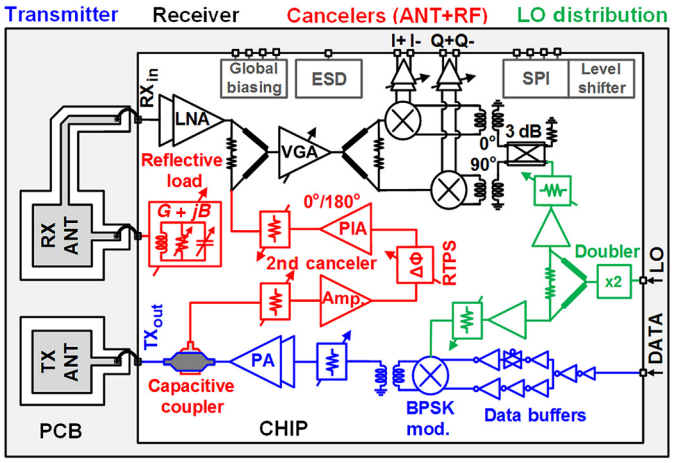

Fig. 1. 60 GHz fully integrated FD transceiver architecture featuring polarization-based reconfigurable wideband antenna cancellation and RF cancellation.

II. MM-Wave FD System Analysis

A. Architecture

The 60 GHz FD transceiver architecture is shown in Fig. 1. It is a direct conversion BPSK[1] transceiver consisting of five main parts: 1) on-PCB T/R antenna pair with polarization-based antenna cancellation; 2) TX; 3) RX; 4) the second RF canceler; and 5) LO distribution. The antenna pair is based on cross-polarized slot loop antennas, and a high-order on-chip termination is embedded within the antenna pair to enable antenna cancellation. It will be explained later in Section III. In the TX, baseband nonreturn-to-zero (NRZ) data are applied to an inverter-chain data buffer driving a BPSK modulator, directly modulating the LO signal. A transformer balun and a 3 bit reflective-type attenuator are included after the BPSK modulator for differential to single-ended conversion and TX power control. A two-stage, two-stacked class-E-like PA constitutes the final stage of the TX to achieve a high output power with high efficiency. The RX consists of a two-stage, high-gain, LNA driving a Wilkinson combiner that injects the cancellation signal from the RF canceler, an RF amplifier followed by a 2 bit attenuator, a Wilkinson-based I/Q splitter, I/Q down-conversion mixers, and two-stage baseband amplifiers.

An 18 dB coupler is integrated as the first block in the second RF canceler to couple a small copy of the transmit signal from the PA output. The TX copy is fed into an attenuator with 16 dB range driving an RF amplifier, followed by a reflection-type phase shifter (RTPS) with $>180°$ analog phase-control range and a $0°/180°$ phase-inverting amplifier (PIA). Finally, the RF cancellation signal is injected into the RX at the LNA output through another 16 dB attenuator and the aforementioned Wilkinson combiner.

LO distribution includes a balanced frequency doubler to allow a 30 GHz LO signal from off-chip. The LO signal is split after the frequency doubler and shared between the RX and the TX to keep phase noise highly correlated between the TX and the RX, reducing its impact on SIC [31], [32]. Circuit implementations of the transceiver blocks are presented in Section IV.

[1]A BPSK modulator was included in the TX for simplicity, but can easily be replaced with an I/Q modulator to support FD links with QAM and other complex modulation formats.

B. FD System Considerations

In this section, we will discuss the system-level design tradeoffs for mm-wave FD operation. All the equations will be in dB-scale except if otherwise mentioned. Fig. 2 depicts the simplified transceiver block diagram used for system-level analysis, including the antenna, second RF, and digital cancellation. The TX signal at the TX output consists of the main TX signal (P_{TX}), TX nonlinear distortions ($P_{\mathrm{TX,dis}}$), and TX noise ($P_{\mathrm{TX},n}$). SI arises due to the inherent coupling at the antenna interface as well as environmental reflections. In our analysis, $C_{T/R}$ represents the net coupling from the TX to the RX at the antenna interface, inclusive of the inherent coupling, environmental reflections, and any antenna SIC that is achieved. A total SI suppression of $P_{\mathrm{TX}} - P_{\mathrm{noise}} + 6$ dB is required to suppress the main TX signal below the RX input-referred noise floor ($\mathrm{P_{noise}} = -174\,\mathrm{dBm/Hz} + 10\log(\mathrm{BW}) + \mathrm{NF_{RX,tot}}$), assuming a 6 dB margin.

Assuming RX and TX antenna gains of G_{ANT}, an RX BW of 2.16 GHz (specified in IEEE 802.11ad standard), a typical RX NF of $\mathrm{NF_{RX,tot}} = 5$ dB and BPSK modulation with a required bit error rate of $\mathrm{BER} = 10^{-6}$ (requiring $\mathrm{SNR_{out}} = 12$ dB), the link budget can be calculated as[2]

$$P_{\mathrm{TX}} + 2G_{\mathrm{ANT}} + L_{\mathrm{FS}} > -174\,\mathrm{dBm/Hz} + 10\,\log(\mathrm{BW}) + \mathrm{NF_{RX,tot}} + \mathrm{SNR_{out}} + \mathrm{LM} \quad (1)$$

where L_{FS} is the free-space path loss and LM is the link margin for the implementation and antenna alignment losses. Assuming $\mathrm{LM} = 10$ dB, a link budget of $P_{\mathrm{TX}} + 2G_{\mathrm{ANT}} > 20$ dBm is required to achieve a 2 m long FD wireless link ($L_{\mathrm{FS}} = 74$ dB). The required total SIC and link budget are both a function of P_{TX}. A higher P_{TX} is desirable for reducing the BER or extending the link distance, whereas a lower P_{TX} demands less SIC, *resulting in a tradeoff between the link budget and SIC. On the other hand, a higher antenna gain relaxes not only the P_{TX} but also the total SIC requirement*.[3] For a state-of-the-art 60 GHz TX output power of 10–15 dBm, a G_{ANT} of 5–2.5 dBi is required, precluding the use of on-chip antennas. Hence, we have pursued on-PCB antennas in this work. For $P_{\mathrm{TX}} = +14$ dBm (and $G_{\mathrm{ANT}} = 3$ dBi), a total SI suppression of $14\,\mathrm{dBm} - (-174\,\mathrm{dBm/Hz} + 10\log(2.16\,\mathrm{GHz}) + 5\,\mathrm{dB}) + 6\,\mathrm{dB} = 96$ dB must be achieved.

An interesting question is, how to distribute this 96 dB SIC along the RX chain. At mm-waves, high-speed high-resolution ADCs form a power consumption bottleneck in the system. Considering the system in Fig. 2, the required ADC dynamic range can be expressed as

$$\mathrm{DR_{ADC}} = 96\,\mathrm{dB} + C_{T/R} - \mathrm{SIC_{RF}} = 6 \times (\mathrm{ENOB} - 2) \quad (2)$$

[2]Assuming the SI is suppressed well below P_{noise}. Note also that $NF_{RX,tot}$ includes the degradation due to SIC.

[3]This assumes that the environmental reflections are weak compared to the SI through the antenna interface, verified by our measurements.

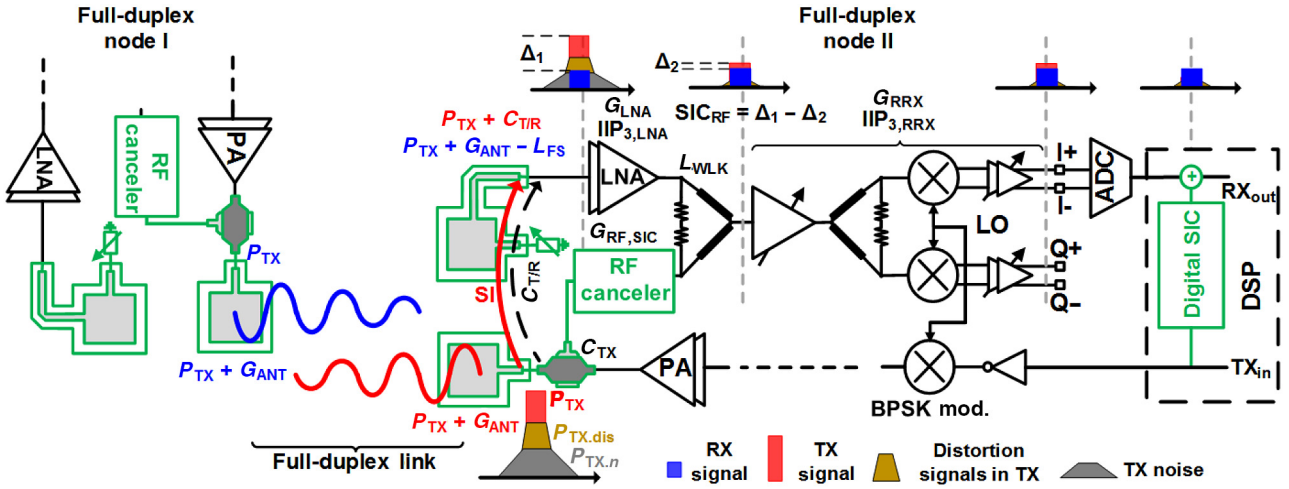

Fig. 2. Simplified FD transceiver block diagram with polarization-based antenna, RF, and digital cancellation.

where ENOB is the effective number of bits. *According to (2), it is essential to achieve a high SIC in the antenna and RF cancelers to relax the ADC dynamic range requirement*. To allow an 8 bit ADC, the antenna and second RF canceler must provide more than 60 dB SI suppression.

The antenna and RF cancelers in Fig. 2 take a copy of not only the main TX signal but also the TX distortion and noise. The TX distortion and noise are weak compared to the main TX signal and are easily suppressed below the RX noise floor by the antenna and RF cancelers. Therefore, we will neglect them in the system level analysis. However, the RX chain and RF canceler might introduce nonlinear distortions on the TX signal which require careful treatment. All these nonlinear distortions can be canceled in the digital domain since they are predictable [18], but this can be more challenging and power-inefficient at mm-wave due to the wide BW. Hence, in Fig. 2, we assume that the antenna interface should suppress the SI at the LNA input, so that third-order inter-modulation products (IM3) generated by the LNA fall below the noise floor. The resultant LNA IIP_3 requirement ($\mathrm{IIP}_{3,\mathrm{LNA}}$) is given as

$$\mathrm{IIP}_{3,\mathrm{LNA}} = \frac{3(P_{\mathrm{TX}} + C_{T/R}) - P_{\mathrm{noise}} - 3}{2}. \tag{3}$$

Equation (3) indicates that a higher suppression at the antenna interface relaxes the LNA linearity requirement. In this work, we achieve more than 50 dB suppression in the antenna canceler as will be presented in Section III, so that an $\mathrm{IIP}_{3,\mathrm{LNA}}$ less than -17.5 dBm is required for $\mathrm{NF}_{\mathrm{RX,tot}} = 5$ dB, $\mathrm{BW} = 2.16$ GHz, and $P_{\mathrm{TX}} = +14$ dBm.

The RF canceler further suppresses the SI in the RX chain, so that IM3 products generated by the rest of the RX (the RF VGA, mixer, and baseband circuits) fall below the noise floor as well. The linearity requirement for the rest of the RX ($\mathrm{IIP}_{3,\mathrm{RRX}}$) can be written as

$$\mathrm{IIP}_{3,\mathrm{RRX}} = \frac{3(P_{\mathrm{TX}} + C_{T/R} - \mathrm{SIC}_{\mathrm{RF}}) - P_{\mathrm{noise}} - 3}{2} + G_{\mathrm{LNA}} + L_{\mathrm{WLK}} \tag{4}$$

where $\mathrm{SIC}_{\mathrm{RF}}$ is the SIC amount achieved by the second RF canceler, G_{LNA} is the LNA gain, and L_{WLK} is the loss of the Wilkinson combiner. For $P_{\mathrm{TX}} = +14$ dBm, $C_{T/R} = -50$ dB, $\mathrm{SIC}_{\mathrm{RF}} = 20$ dB, $P_{\mathrm{noise}} = -76$ dBm, $G_{\mathrm{LNA}} = 18$ dB, and $L_{\mathrm{WLK}} = 4$ dB, the required $\mathrm{IIP}_{3,\mathrm{RRX}}$ becomes -25.5 dBm. *More antenna and RF SIC are essential to reduce the linearity requirement of the whole RX chain.*

Similar to the RX, the RF canceler requires careful design since it should not degrade RX NF or generate large inter-modulation products. As discussed earlier, we would like to keep IM3 products generated by the RF canceler below the RX noise floor. In this case, the IIP_3 requirement on the RF canceler in Fig. 2 can be expressed as

$$\mathrm{IIP}_{3,\mathrm{RFSIC}} = \frac{3P_{\mathrm{TX}} - P_{\mathrm{noise}} - 3 + C_{T/R} + 2C_{\mathrm{TX}}}{2} \tag{5}$$

where C_{TX} is the TX-side coupling. For $P_{\mathrm{TX}} = +14$ dBm, $C_{T/R} = -50$ dB, $P_{\mathrm{noise}} = -76$ dBm, and $C_{\mathrm{TX}} = -18$ dB (based on our implementation), $\mathrm{IIP}_{3,RFSIC}$ should be higher than $+14.5$ dBm. The RF canceler gain ($G_{\mathrm{RF,SIC}}$) should be equal to $C_{T/R} + G_{\mathrm{LNA}} - C_{\mathrm{TX}}$ for perfect cancellation. Using $G_{\mathrm{LNA}} = 18$ dB, Fig. 3 compares three different configurations for the RF canceler implementation ($G_{\mathrm{RF,SIC}} = -14$dB), and shows the $\mathrm{IP}_{1\mathrm{dB}}$ requirements for each stage to achieve an $\mathrm{IIP}_{3,\mathrm{RFSIC}} = 14.5$ dBm as well as the overall achieved NF in the RF canceler. Assuming an RF amplifier with 12 dB gain and 3 dB NF, an RTPS with 8 dB loss and a PIA with 8 dB gain and 4 dB NF (all based on our implementation), 26 dB attenuation is required, which can be distributed in the chain in various ways. A high attenuation at the front (configuration-1) is essential to relax the linearity requirement on the succeeding blocks, especially the amplifier and PIA, whereas attenuation at the end (configuration-2) reduces the canceler NF. Splitting the attenuation at the front and end trades off linearity and noise performance in the RF canceler (configuration-3). Assuming that the NF of the RF canceler is $\mathrm{NF}_{\mathrm{RF,SIC}}$, the total NF of the RX ($\mathrm{NF}_{\mathrm{RX,tot}}$) can be written in linear scale as [33]

$$\mathrm{NF}_{\mathrm{RX,tot}} = \mathrm{NF}_{\mathrm{RX}} + (\mathrm{NF}_{\mathrm{RF,SIC}} - 1)\frac{C_{T/R}}{C_{\mathrm{TX}}}. \tag{6}$$

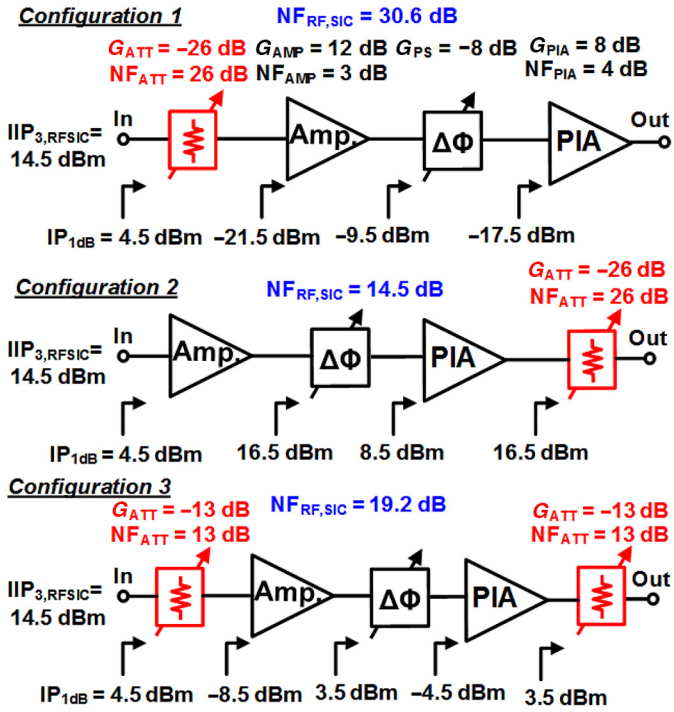

Fig. 3. RF canceler linearity and noise figure considerations: placing all the attenuation at the front (configuration-1) relaxes the linearity requirement of the amplifiers. To reduce the RX NF degradation, all the attenuation should be placed at the end (configuration-2). Attenuation may be distributed at the front and end to tradeoff the RF canceler linearity and NF, resulting in a negligible RX noise floor increase due to the RF canceler noise and IM3 products (configuration 3). In each case, the required 1 dB compression point at the input of each stage to maintain an overall RF canceler IIP_3 of $+14.5$ dBm and the overall RF canceler NF are computed and shown.

Fig. 4 presents $\mathrm{NF}_{\mathrm{RX,tot}}$ and $\mathrm{IIP}_{3,\mathrm{RFSIC}}$ versus $C_{T/R}$ for the three different configurations in Fig. 3. To plot $\mathrm{NF}_{\mathrm{RX,tot}}$ in Fig. 4, the required attenuation G_{ATT} and corresponding $N_{\mathrm{RF,SIC}}$ are recalculated as $C_{T/R}$ changes. $\mathrm{NF}_{\mathrm{RX}}$ is assumed to be 5 dB. It should be noted that the three configurations converge to each other as expected for high $C_{T/R}$ or for $G_{\mathrm{ATT}} = 0$ dB. *A lower $C_{T/R}$ reduces not only the linearity requirement of the RF canceler but also the RX NF degradation so that an RF canceler configuration with a higher NF can be tolerated.* As a result, at $C_{T/R} = -50$ dB, configuration-3 is as good as configuration-2 from a noise perspective and does not increase $\mathrm{NF}_{\mathrm{RX,tot}}$. Therefore, in this work, we distribute the attenuation at the front and back of the RF canceler (configuration-3), resulting in negligible degradation in the RX noise floor due to the canceler noise and IM3 products.

Based on these concepts and assuming a P_{TX} of $+14$ dBm, a $C_{T/R}$ of -44 dB without antenna SIC, an antenna SIC of 14 dB, and RF SIC of 20 dB (based on our measurements in Section V) as well as a BW of 2.16 GHz and $\mathrm{NF}_{\mathrm{RX,tot}}$ of 5dB, Fig. 5 tracks the SI, desired signal at the sensitivity level, RX noise floor, and SI IM3 products generated in the RX along the chain for our design. The contribution of the RF canceler noise and IM3 products are not shown for brevity because the aforementioned design principles ensure that they contribute negligibly.

In reality, as mentioned earlier, SI also arises from mechanisms other than the inherent coupling, such as

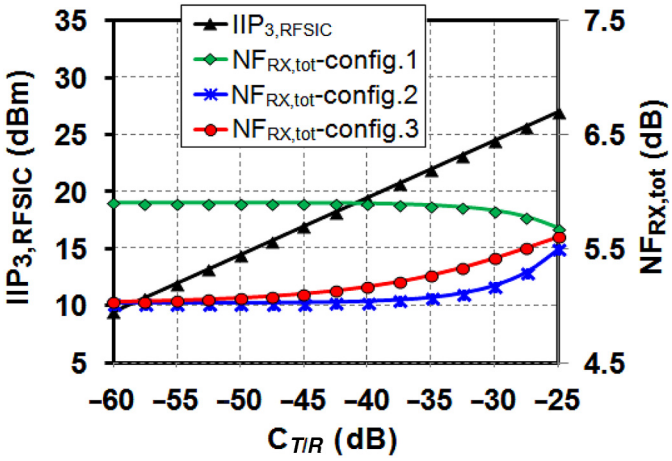

Fig. 4. Required IIP_3 for the RF canceler versus $C_{T/R}$ to keep the generated IM3 products below the RX noise floor and $\mathrm{NF}_{\mathrm{RX,tot}}$ for the three different RF canceler configurations.

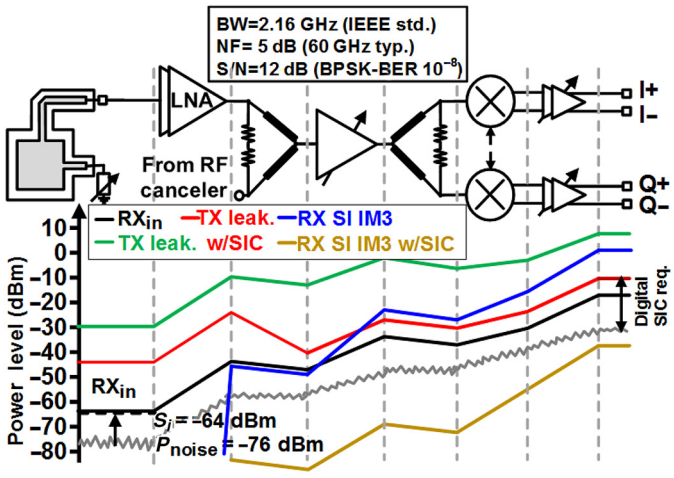

Fig. 5. Received signal, SI, RX noise floor, and SI IM3 products generated in the RX (with and without antenna and RF SIC) are tracked through the RX chain for $P_{\mathrm{TX}} = +14$ dBm, $C_{T/R} = -44$ dB without ANT SIC, ANT SIC of 14 dB and RF SIC of 20 dB. BW is assumed to be 2.16 GHz and $\mathrm{NF}_{\mathrm{RX,tot}}$ is assumed to be 5 dB. Without ANT and RF SIC, the TX leakage (SI) and its IM3 products generated along the RX mask the desired signal. SIC suppresses the SI so that IM3 products are suppressed below the RX noise floor. Additional cancellation of the main SI is required and can be achieved in the digital domain.

environmental reflections and on-chip coupling. Environmental reflections are unknown at the design time and change during in-field operation. Therefore, *the antenna and RF cancelers should be reconfigurable to combat environmental reflections and thus enable robust FD operation.* We placed the RX and TX as far from each other as possible in the layout to reduce the on-chip coupling. Other than separating the TX and RX chains, conductor-backed CPW lines with side grounds are used to implement matching networks and interface the blocks, further reducing the on-chip coupling. Our measurements show that net coupling referenced between the TX output and the RX input is lower than 78 dB over 57–66 GHz, weaker than our measured predigital SI suppression and hence not a significant concern.

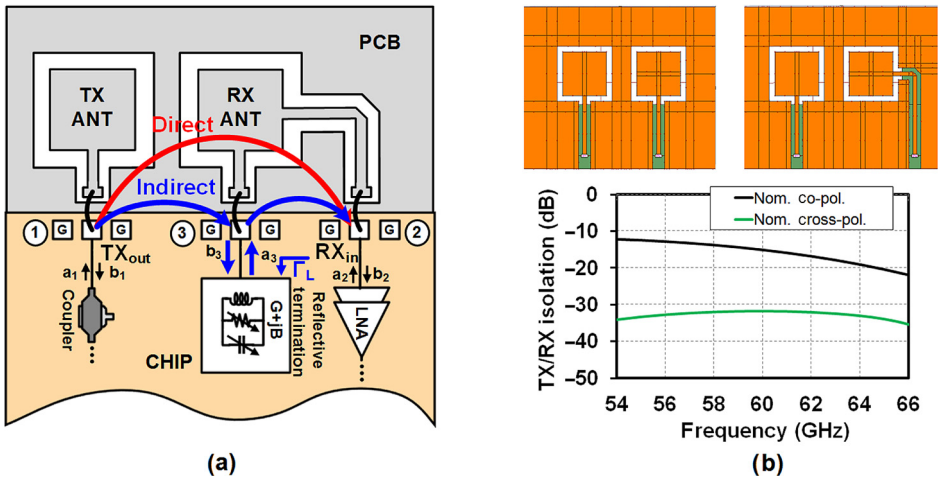

Fig. 6. Polarization-based reconfigurable SIC: (a) T/R antenna pairs with orthogonal polarizations are employed to increase initial isolation. An AUX port co-polarized with the TX antenna is introduced on the RX antenna and terminated with a reconfigurable reflective termination to perform SIC. (b) Co-polarized and cross-polarized slot-loop T/R antenna pairs at 60 GHz based on the dimensions and PCB cross section shown in Fig. 7 (image taken from a layout in IE3D, a method-of-moments-based EM simulator) and comparison of their T/R isolation.

III. Polarization-Based Reconfigurable Wideband Antenna Cancellation

The polarization-based SI cancellation technique in the antenna domain is shown in Fig. 6(a). *Apart from frequency, amplitude, and phase, which are the conventional degrees of freedom in the electronic domain, polarization is another degree of freedom in the wave propagation domain*. In this work, we first employ cross-polarized TX and RX antennas to improve the initial isolation between the TX output and the RX input. This increases the TX-to-RX isolation from 12–22 dB to 32–36 dB over 54–66 GHz [Fig. 6(b)]. These simulations are for rectangular slot-loop antennas in a PCB cross section that is described later in this section.

To improve the TX-to-RX isolation further and combat the scattering from environment, an SI cancellation technique is embedded in the antenna domain by introducing an auxiliary (AUX) port copolarized with the TX antenna on the RX antenna. As depicted in Fig. 6(a), the introduction of the AUX port creates an indirect path from the TX output to the RX input. The indirect path represents the cancellation signal which first couples to the AUX port, then reflects from a reflective on-chip reconfigurable termination, and eventually couples into the RX input to cancel the SI from the direct path. Assuming that the RX port is matched, the total isolation from the TX output to the RX input $C_{T/R}$ can be expressed as

$$C_{T/R} = \frac{b_2}{a_1} = S_{21} + \frac{S_{23}S_{31}\Gamma_L}{1 - S_{33}\Gamma_L} \tag{7}$$

where S_{21}, S_{31}, S_{23}, and S_{33} are the S-parameters of the three-port antenna structure including π-type PCB-to-chip transitions formed by on-chip pad capacitance, wirebond inductance, and on-PCB pad capacitance (ports 1, 2, and 3 are $\mathrm{TX_{out}}$, RX_{in}, and AUX ports, respectively), a_1 is the incident power wave at $\mathrm{TX_{out}}$, b_2 is the outgoing power wave at RX_{in}, and Γ_L is the reflection coefficient of the variable on-chip termination. The direct (first) and indirect path (second) terms in (7) must be set equal in magnitude and 180° out of phase to achieve perfect SIC ($C_{T/R} = -\infty$ dB).

The SIC bandwidth depends on how well the equal magnitude and out of phase conditions are satisfied across frequency. Conventional antenna or RF cancellation techniques mimic the direct path's magnitude and the phase at a single frequency [23], [34], [28] or at slightly separated frequencies [24]. In a canceler with $2N$ degrees of freedom to achieve wideband SIC, the direct path's magnitude and phase can be either mimicked at N separated frequencies or the magnitude, phase as well as their slopes can be mimicked at $N/2$ frequencies. *In this work, we choose to mimic the magnitude and phase of the direct path as well as their slopes, resulting in wideband SIC.*

A detailed algorithmic design methodology for our antenna cancellation technique is described in [35]. We will briefly outline the procedure in this section for the sake of completeness. First, the 60 GHz T/R antenna pair is designed and simulated in IE3D, a method-of-moments-based EM simulator [36]. The T/R antennas are implemented as rectangular slot loop antennas on Rogers 4350B because of their higher bandwidth. The TX and RX antennas are co-located *to ensure a small-form factor and allow potential scaling of the technique to arrays and MIMO*. Such a compact and co-located antenna pair cannot be used to double the capacity in a half-duplex MIMO scenario since the antenna spacing is much smaller than the required Rayleigh spacings for reasonable link distances (5 cm for a 1 m link at 60 GHz), causing correlation between the MIMO paths. In other words, the proposed antenna pair does not steal any resources from MIMO and can be used to design FD MIMO radios, further improving the capacity offered by MIMO. Fig. 7 shows the antenna dimensions and the four-layer PCB cross section. The TX and RX antennas are implemented on the top copper layer of a 4 mils Rogers 4350B ($\epsilon_r = 3.48$, $\tan(\delta) = 0.0037$ at 10 GHz) material. A 20 mils Rogers 4350B layer is used underneath to increase the directivity on the backside.

After finalizing the T/R antenna core, the required admittance for perfect SIC $Y_{\mathrm{L,req}} = Y_0 \frac{1-\Gamma_{\mathrm{L,req}}}{1+\Gamma_{\mathrm{L,req}}}$ is calculated across

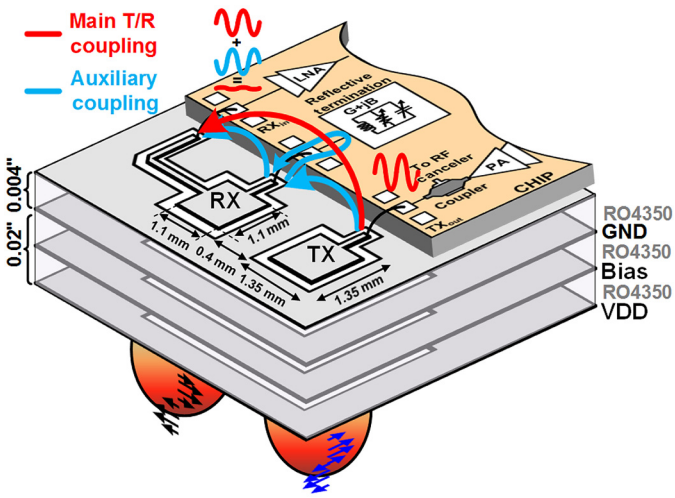

Fig. 7. Polarization-based reconfigurable wideband antenna SIC: 3-D implementation view showing antenna and PCB dimensions and cross section.

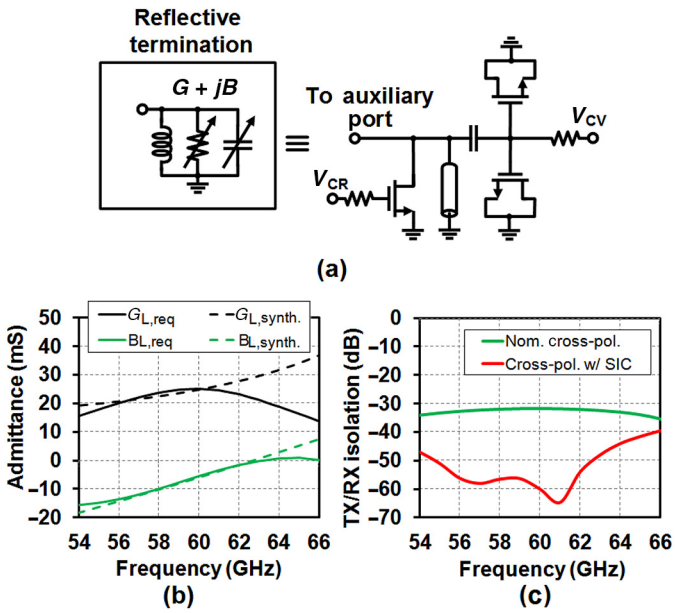

Fig. 8. (a) Schematic diagram of the implemented fully integrated reconfigurable parallel-RLC reflective termination. (b) Comparison of synthesized conductance and susceptance to the required values across frequency for perfect SIC. (c) Resultant antenna cancellation.

frequency where $\Gamma_{\mathrm{L,req}} = -S_{21}/(S_{23}S_{31} - S_{21}S_{33})$ from (7). Fig. 8(b) shows the simulated required conductance $(G_{\mathrm{L,req}})$ and susceptance $(B_{\mathrm{L,req}})$ to achieve perfect SIC across frequency. As mentioned earlier, a higher order reflective termination provides more degrees of freedom to replicate the required conductance, susceptance, and their slopes at more frequencies. In this work, we use a programmable parallel RLC termination with variable R, variable C, and fixed L Fig. 8(a). The variable C and fixed L synthesize both magnitude and slope of $B_{\mathrm{L,req}}$ at one frequency. L is set to replicate the slope of $B_{\mathrm{L,req}}$ dictated by the EM simulation of the T/R antenna structure. The variable R in parallel can synthesize arbitrary $G_{\mathrm{L,req}}$ but would result in a slope of $G_{\mathrm{L,synth}}$ that is zero. We ensure that the required slope of $G_{\mathrm{L,req}}$ is also zero using the length of the transmission lines feeding the antennas as another degree of freedom [35]. Fig. 8(b) shows the synthesized $G_{\mathrm{L,synth}}$ and $B_{\mathrm{L,synth}}$ to achieve wideband SIC. In this simulation, finite quality factors of the L and C cause slight frequency dependency in $G_{\mathrm{L,req}}$. As shown in Fig. 8(c), an SI suppression more than 50 dB is achieved over 8 GHz bandwidth in simulation. According to our EM simulation, a similar isolation could also be achieved separating cross-polarized TX and RX antennas by 5 cm, clearly not a compact solution. As mentioned earlier, this separation is of the order of the Rayleigh separation for a 1 m 60 GHz MIMO link, implying that such an approach would steal resources from a potential MIMO implementation. This wideband cancellation corresponds to a fractional bandwidth of 13.5%, vastly superior to prior antenna [23], [24] and RF cancellation works [26]–[29]. *This is a direct result of the use of a higher order termination and the replication of the magnitudes and slopes of* $G_{\mathrm{L,req}}$ *and* $B_{\mathrm{L,req}}$. This high fractional bandwidth is also a consequence of the fact that this cancellation technique is contained within the antenna pair itself. *Essentially, the antenna cancellation technique embeds the functionalities of the TX- and RX-side couplers within the antennas, resulting in main and AUX paths that are very close to each other in nature and transfer function, enhancing cancellation bandwidth.*

The reconfigurable nature of the termination enables the cancellation to be maintained in the face of varying environmental reflections, as will be experimentally demonstrated in Section V. If greater flexibility is required in the termination, for even wider bandwidth cancellation or more severe environmental reflections, higher order terminations and/or terminations with variable L (realized through a transmission-line with multiple switch-based short-circuit terminations at different lengths) can be used.

The simulated TX and RX radiation patterns at 60 GHz with and without SIC are shown in Fig. 9. The simulated TX antenna gain is 4.5 dB without SIC in the broadside direction and degrades by 1.1 dB with SIC. The effect of SIC on TX antenna gain varies with the elevation angle θ and is plotted in Fig. 10 for $\Phi = 0°$ and $\Phi = 90°$. The maximum degradation in the TX pattern is 1.1 dB at around $\theta = 0°$. The variation in the TX antenna gain occurs as a result of the radiation of the coupled TX signal at the AUX port from the RX antenna. This indirect radiation from the RX antenna interferes with the main radiation from the TX antenna in the far-field. This mechanism can be modeled as a 2×1 antenna array with nonuniform amplitude excitations and is analyzed in [35]. Based on the analysis provided in [35], the theoretical TX antenna gain degradation, the difference between the antenna gain without SIC and with SIC, is calculated for this work (using the simulated TX to AUX port coupling of 15.4 dB (phase of 25°), $\Gamma_{\mathrm{L,synth}} = 0.4\angle 137°$, and antenna separation $d = 0.384\lambda$) and compared to the EM simulations in Fig. 10. As can be seen, the simulations compare well with the theory. SIC degrades the RX antenna gain by 0.18 dB in simulation in the broadside direction. The desired signal arriving in the desired polarization hitting the antenna splits between the RX and the AUX ports due to the finite axial ratio. The signal at the AUX port reflects from the reflective termination and then couples into the RX port, interfering with the

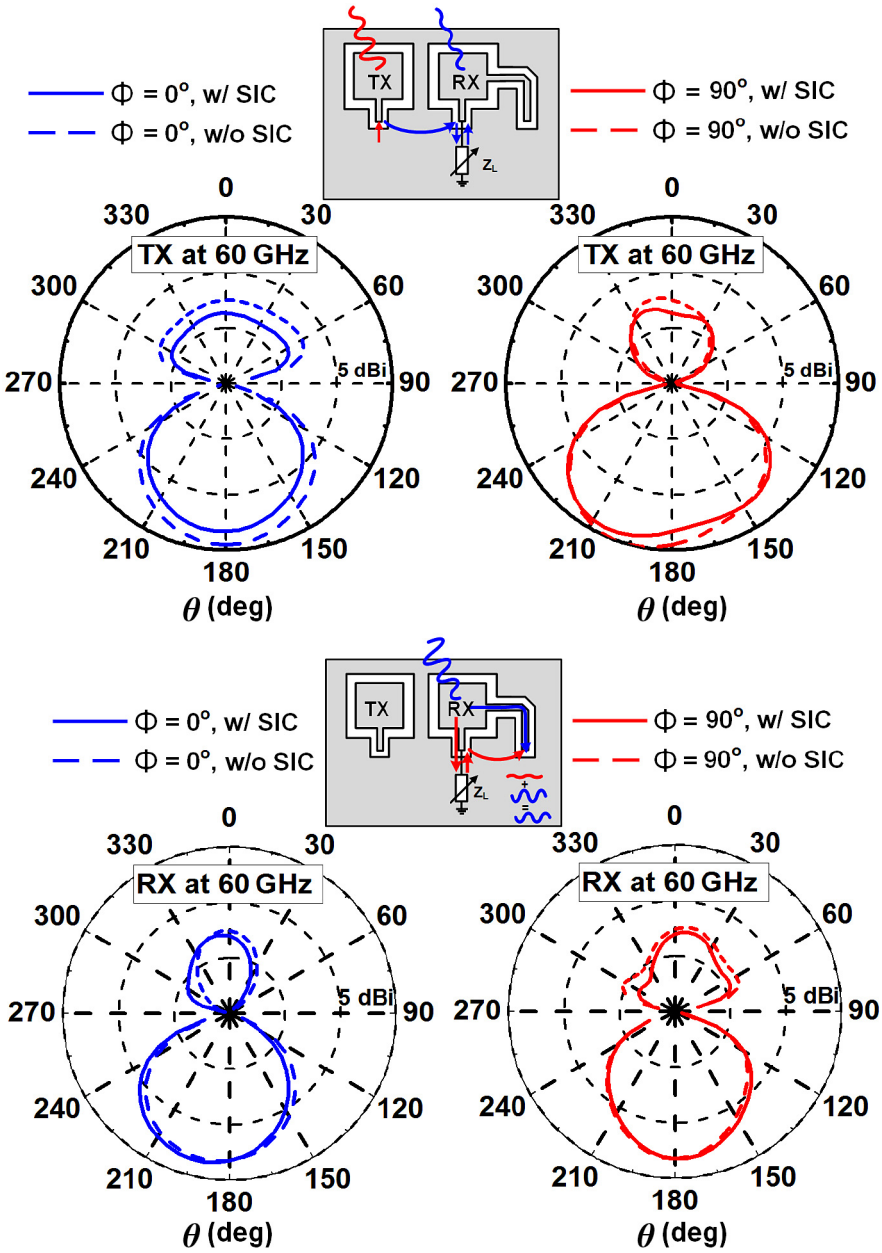

Fig. 9. TX and RX patterns with and without SIC (simulation). The radiation of the coupled TX signal at the AUX port from the RX antenna interferes with the main radiation of the TX signal in the far-field, affecting TX antenna gain. The received signal going into the AUX port reflects from the variable termination and then couples into the RX port, interfering with the desired signal and affecting the RX antenna gain.

desired signal at the RX port [35]. The total degradation in the RX antenna gain due to the introduction of the AUX port (due to power splitting between RX and AUX ports depending on the axial ratio) and SIC (compared to the case with zero reflection at the AUX port) is theoretically calculated as 0.41 dB based on the analysis in [35], which compares well with the simulation.

Further, the noise of the reflective termination due to its resistive part leaks into the RX input, forming another degradation mechanism for the RX NF. The NF degradation due to the reflective termination is theoretically calculated as 0.43 dB based on the analysis presented in [35], consistent with the simulated value of 0.52 dB.

The penalties on the TX and RX antenna gains are similar to the TX efficiency penalty and NF penalty of RF cancelers and can be reduced by increasing the TX-AUX and RX-AUX isolations, respectively. The noise leakage from the reflective termination is also similar to the NF penalty of RF cancelers and can be reduced by increasing the RX-AUX isolation.

IV. Implementation

A. Reflective Termination

The circuit diagram of the reflective termination is shown in Fig. 11. The variable R is implemented as a 15μm/40 nm body-floating NFET operating in the deep triode region, providing 0.14–44 mS conductance at $V_{\rm CR} = 0 - 1$ V. A shorted transmission line with a length of 120 μm is employed as the shunt L. An inversion-mode NFET varactor bank consisting

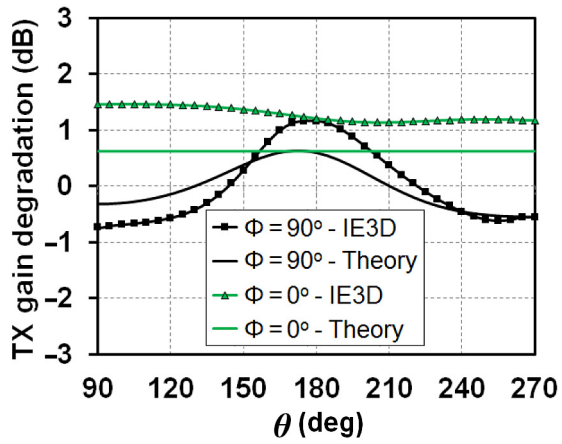

Fig. 10. Comparison of the simulated TX antenna gain degradation (calculated by subtracting the antenna gain with SIC from the antenna gain without SIC) to the theoretical degradation based on the analysis in [35].

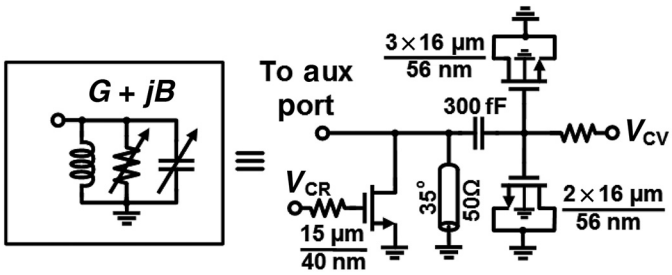

Fig. 11. Implementation of the reflective termination: variable R and C are implemented as a deep-triode NFET and an inversion-mode NFET varactor bank, respectively. L is implemented as a 120 µm long shunt transmission line.

of 2×16 µm/56 nm and 3×16 µm/56 nm devices serves as the variable capacitance. 56 nm body-contacted devices are preferred over 40 nm body-floating counterparts because of their higher tuning ratio. For a 2×16 µm/56 nm device, the simulated minimum capacitance is 38 fF with a tuning ratio of 1.82, and the quality factor varies from 27 to 10 when the control voltage $V_{\rm CV}$ is swept from 0 to 1.2 V.

B. RF Canceler

The three-port capacitive coupler depicted in Fig. 12(a) takes a small copy of the TX signal to feed into the RF canceler. It achieves a simulated −18 to −15.5 dB coupling with an insertion loss less than 0.3 dB over 50–70 GHz.

The RF canceler employs a reflective-type attenuator based on a variable shunt resistor implemented as an NFET operating in the deep triode region with $V_{\rm DS} = 0$ V for no power consumption [Fig. 12(b)]. A 3µm/40 nm body-floating NFET provides 6 Ω ON-resistance at a control voltage of $V_{C,\rm ATT1} =$ 1.2V and achieves 16 dB attenuation range at 60 GHz. $V_{C,\rm ATT1}$ is applied through a 6 kΩ resistance to make the gate float for AC, reducing the loss at $V_{C,\rm ATT1} = 0$V (0.7 dB at 60 GHz) [37].

A single-stage RF amplifier implemented in stacked topology follows the attenuator [Fig. 12(b)]. The stacked topology is chosen to improve the power handling capability by increasing supply voltage to 2.1 V [38] as well as to achieve higher reverse isolation. A small degeneration inductance (TL2) is used to ease the input matching. The amplifier, biased at a current density of 0.4 mA/µm, provides a small-signal gain of 12 dB in simulation.

Fig. 12(c) shows the circuit diagram of the RTPS consisting of a 3 dB quadrature broadside coupled-line coupler and two identical reflective CLC terminations. Vertically coupled microstrip lines are implemented using the top two metal layers to reduce the loss. Slow-wave technique (10 µm wide slots separated by 10 µm spacing in the ground plane) and asymmetry (4 µm offset) between the coupled lines are introduced in the coupler as additional degrees of freedom to simplify the design procedure, allowing control of odd and even mode impedances independently [37]. 4×16 µm/56 nm inversion-mode NFET varactors are employed in the reflection termination, resulting in a simulated phase range of 210° with a loss variation of 4.5–8.5 dB at 60 GHz.

The 0/180° PIA is derived from the RF amplifier by adding an additional cascode transistor to commutate the current at the cascode node [Fig. 12(d)]. The PIA is followed by a vertically coupled transformer balun. The balanced and unbalanced coils are implemented in a stack of UB and UA and LB [details are shown in Fig. 12(d)]. 58 fF capacitors are used in shunt and series at the balun input and output for matching to 50 Ω. The center-tap is grounded to reduce the phase imbalance. The simulated phase and amplitude imbalances are less than 1.6° and 0.5 dB over 55–65 GHz, respectively. Another reflective-type attenuator with 16 dB attenuation range is placed after the PIA.

The RF canceler provides 390° phase and 32 dB gain control range in simulation. When the RF canceler is configured as shown in the configuration-3 of Fig. 3, the simulated NF and $\rm IIP_3$ of the canceler are 15.1 dB and 14.1 dBm at 60 GHz, respectively, consistent with the system-level analysis.

C. TX and RX

Fig. 13(a) depicts the two-stage class-E-like PA implemented by stacking two 44 × 16 µm/40 nm floating-body devices to increase voltage swing at the load. Device sizes, supply, bias voltages, and gate capacitor values are selected based on the theoretical analysis and considerations described in [38] and [39]. A multiplicity-based device layout is used to keep a good balance between $f_{\rm max}$ and f_T. The PA achieves a simulated saturated output power of +16 dBm with 27.4% PAE at 60 GHz.

The BPSK modulator [Fig. 13(b)] is nothing but the PIA described earlier operating in dynamic mode with a 1.2 V supply. An inverter chain data buffer-sized with a fanout of 4 drives the switching transistor pair, whereas the LO signal is applied to the common source device. A 3 bit attenuator consisting of shunt NFET resistors is included at the BPSK modulator output for TX power control.

The LNA is implemented using two inductively degenerated cascode stages, shown in Fig. 14(a). Each stage is biased at a current density of ≈0.25 mA/µm for minimum NF. A simulated gain and noise figure of 18.5 and 2.6 dB are achieved at 60 GHz, respectively. The simulated $\rm IIP_{3,LNA}$ is −10 dBm, consistent

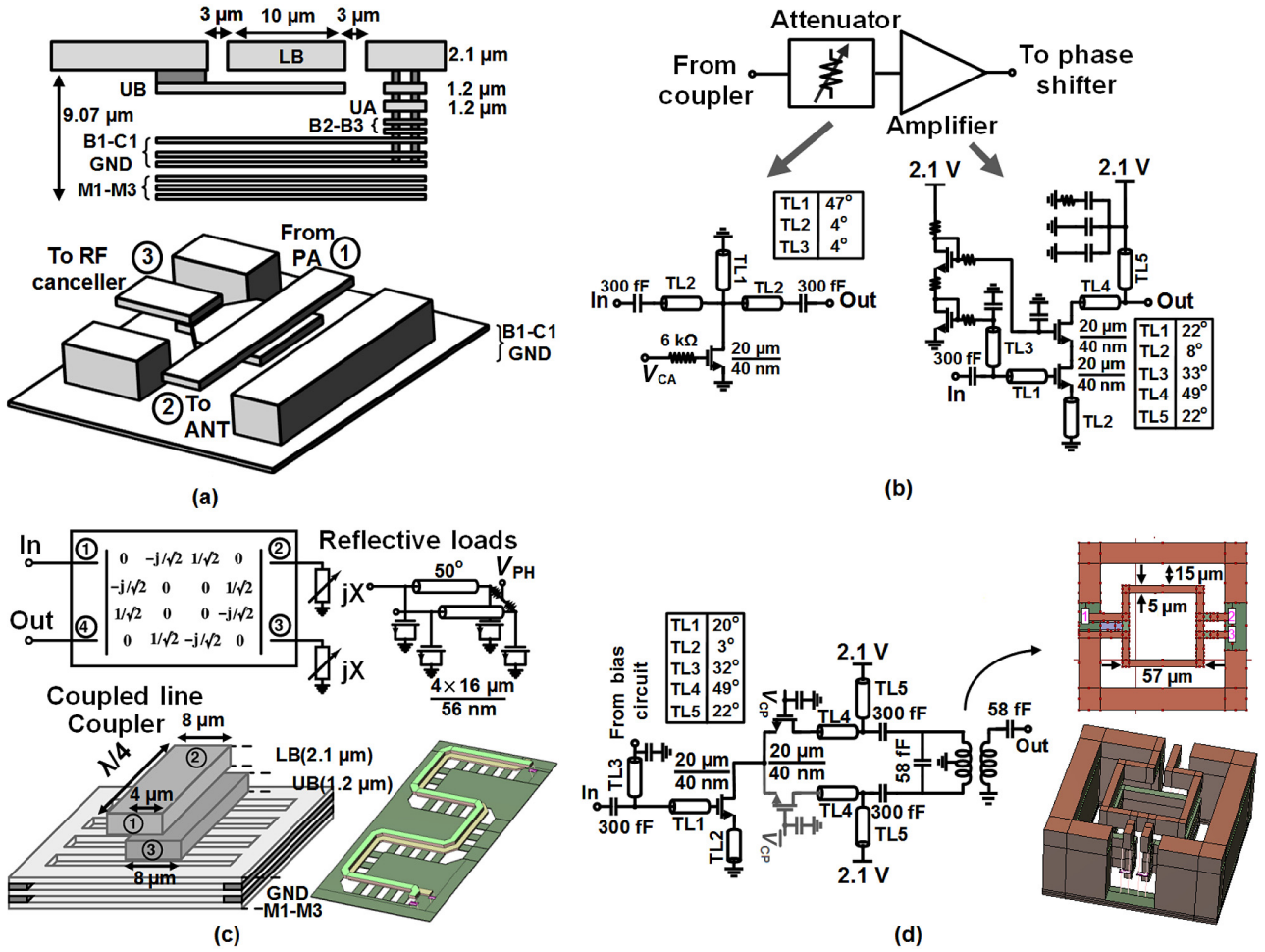

Fig. 12. Implementation of the blocks in the RF canceler. (a) Three-port capacitive coupler. (b) Variable gain amplifier consisting of the 16 dB reflective-type attenuator followed by an RF amplifier. (c) RTPS. (d) PIA. All transmission lines have 50 Ω characteristic impedance.

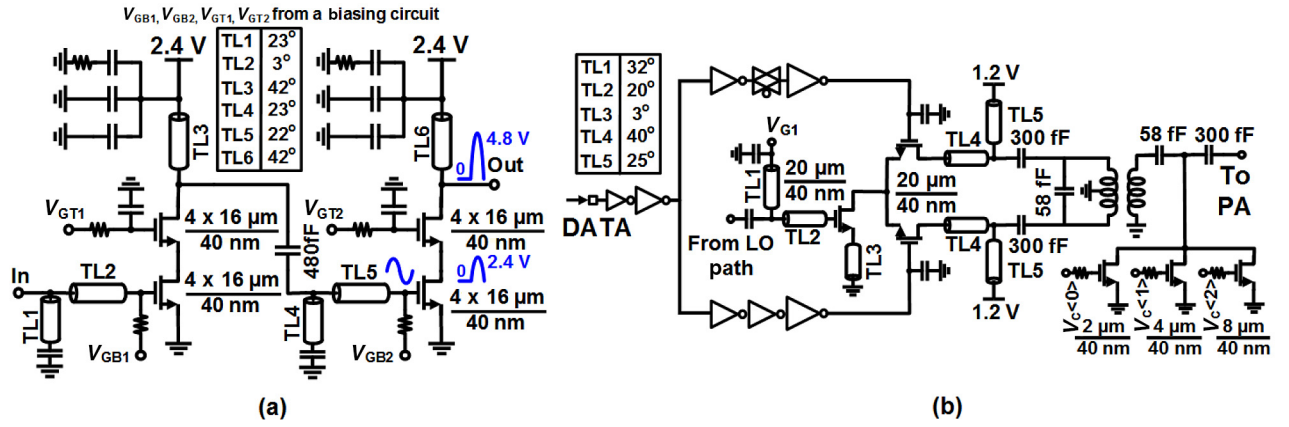

Fig. 13. TX implementation: (a) PA and (b) BPSK modulator followed by the 3 bit attenuator. All transmission lines have 50 Ω characteristic impedance.

with our system level analysis. The VGA implementation consists of a 2 bit attenuator similar to the one used at the BPSK modulator output and an RF amplifier similar to the one in the RF canceler but with a reduced supply voltage of 1.2 V. The I/Q down-conversion mixers are designed using a half-Gilbert cell topology with current-stealing to improve the conversion gain and to reduce the noise from the switching pair as well as the required LO power [40] [Fig. 14(b)]. Similar to the LNA first stage, the trans-conductance stage of the mixer is designed for minimum noise figure (inductive degeneration and current density of ≈ 0.25 mA/µm). The current stealing shunt transmission line $TL2$ steals one-third of the dc current (2 mA out of 6 mA) and resonates the parasitic capacitance at the drain of the common source device. Fig. 14(c) shows the circuit diagram of the baseband amplifier consisting of a simple differential pair first stage and an open-drain last stage to ease interfacing

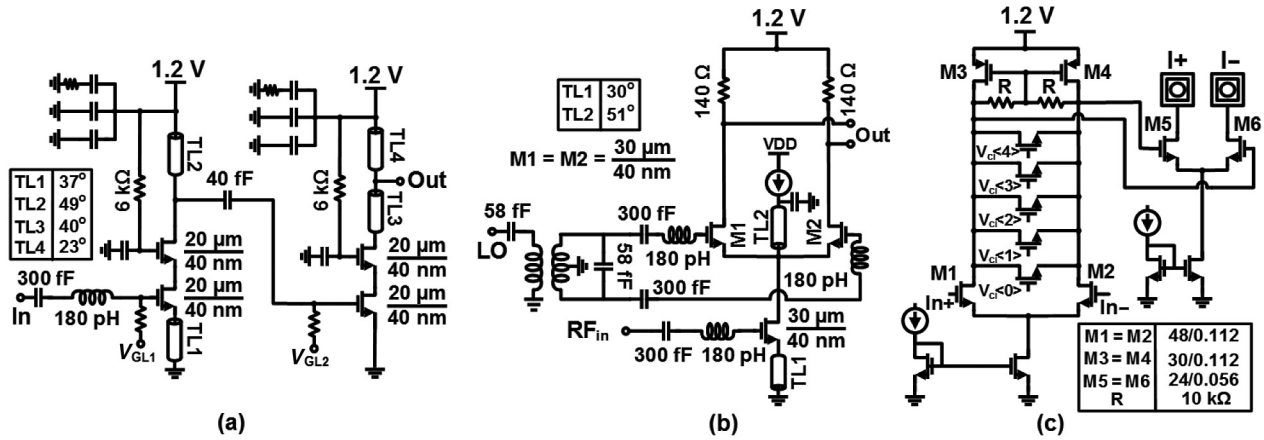

Fig. 14. RX implementation: (a) LNA, (b) current-stealing single-balanced mixer, and (c) baseband amplifier.

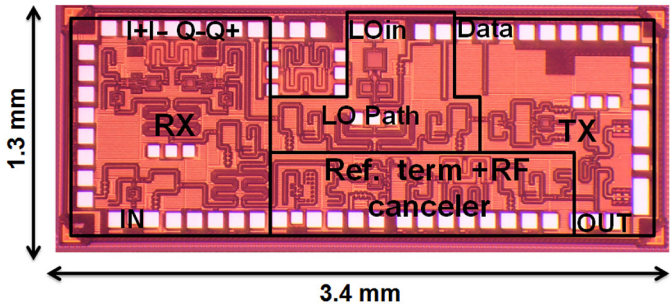

Fig. 15. Chip microphotograph of the 60 GHz 45 nm SOI CMOS fully integrated FD transceiver IC.

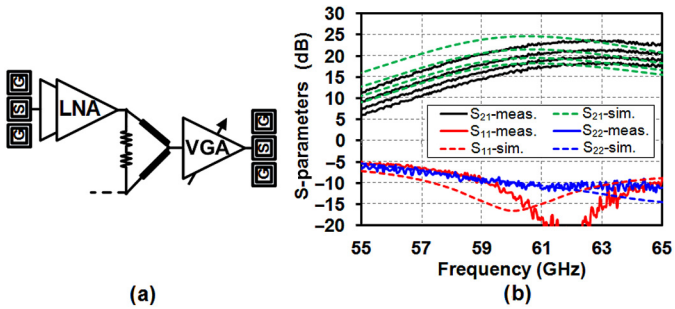

Fig. 16. (a) Measurement setup. (b) Measured and simulated S-parameters of the LNA, Wilkinson, and VGA break-out through an internal test pad. The VGA provides 5.6 dB gain control across 2 bits.

with measurement equipments. 5 bit NFET resistance bank is included in the first stage for gain control. The IIP_3 of the VGA, I/Q mixers, and baseband amplifiers is simulated as -14.9 dBm in the highest gain setting, significantly larger than the $\mathrm{IIP}_{3,\mathrm{RRX}}$ calculated in the system-level analysis.

We reused the amplifiers and attenuators in the RF canceler and BPSK modulator for the LO distribution, and a simple balanced frequency doubler is included at the input. The LO path can deliver up to 7 dBm in simulation to the BPSK modulator and IQ down-conversion mixers.

V. Measurements

The transceiver IC is fabricated in an IBM 45 nm SOI CMOS process which has an $f_{\max}$ of $\approx$ 250 GHz for 40 nm floating-body devices [38], [41] and an 11-metal back-end (Fig. 15). Internal pads are placed at the doubler output, PA input, and RX VGA output to evaluate the performance of some key sub-blocks separately.

A. Break-Out Measurements

The LNA-Wilkinson-VGA break-out is tested through RF probing using a chip-on-board-based setup, whereas the cancellation path is powered on with the lowest attenuation (highest gain) setting, presenting $\approx$50 Ω at the third Wilkinson port [Fig. 16(a)]. The connection of the VGA to the Wilkinson-based I/Q splitter is laser-trimmed to eliminate its loading. Fig. 16(b) shows the measured S-parameters of the LNA-Wilkinson-VGA break-out. The measured peak gain is 23.6 dB at 62.5 GHz with 5.6 dB gain control across 2 bits. The measured results agree well with the simulations, with a 2.5 GHz upward shift which is attributed to overestimation of capacitive parasitics at the design time as well as BEOL process variations.

The RF canceler phase and gain control range are evaluated from the TX output pad to the internal pad at the RX VGA output while the LNA and PA are powered ON [Fig. 17(a)]. Small-signal measurements of the RF canceler break-out, shown in Fig. 17(b) along with simulated results as dashed lines, display a peak gain of 1.8 dB at 59 GHz for an RTPS phase control voltage of $V_{C,\mathrm{PH}} = 0$ V and attenuator control voltages of $V_{C,\mathrm{ATT1}} = V_{C,\mathrm{ATT2}} = 0$V. An analog gain control range of 28 dB is achieved by varying $V_{C,\mathrm{ATT1}}$ and $V_{C,\mathrm{ATT2}}$ from 0 to 0.8V (32 dB gain range by varying $V_{C,\mathrm{ATT1}} = V_{C,\mathrm{ATT2}}$ up to 1.2 V) . Fig. 17(c) shows the RTPS phase range and loss variation with $V_{C,\mathrm{PH}}$ at 60 GHz at the minimum attenuation setting of the RF canceler $V_{C,\mathrm{ATT1}} = V_{C,\mathrm{ATT2}} = 0$V. The RTPS provides 206° analog phase range with 15 dB loss variation. The measured RTPS phase range compares well with the simulation and the discrepancy between the simulated and the measured loss variation is attributed to an asymmetry in the layout which causes destructive interference. The large loss variation across RTPS settings is not a significant concern in our case, since the RTPS is employed in a chain which actually requires attenuation. In other words, the excess loss for some phase settings can be compensated for in the variable attenuators. Additionally, the PIA in the RF canceler provides a discrete phase shift of 180$\pm$2° over 55–65 GHz with an

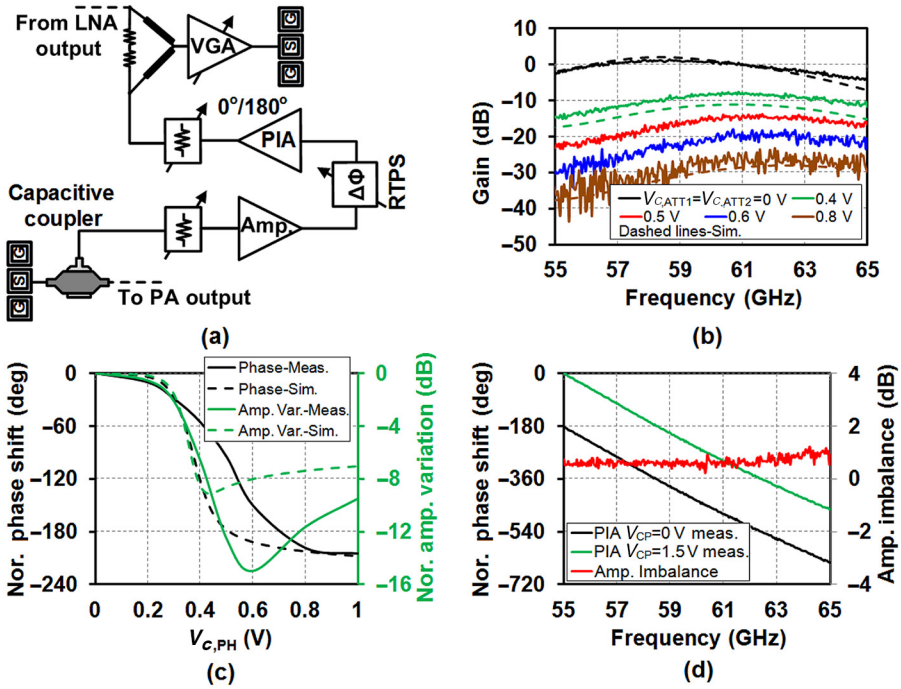

Fig. 17. Small-signal measurements of the RF canceler. (a) Measured break-out diagram. (b) Measured and simulated (dashed lines) gain and gain control across frequency ($V_{C,\mathrm{PH}} = 0\,\mathrm{V}$) . (c) Normalized phase shift and amplitude variation versus RTPS control voltage $V_{C,\mathrm{PH}}$ at 60 GHz ($V_{C,\mathrm{ATT1}} = V_{C,\mathrm{ATT2}} = 0\,\mathrm{V}$) . (d) Normalized phase shift versus frequency for both PIA settings and amplitude imbalance between the two PIA settings.

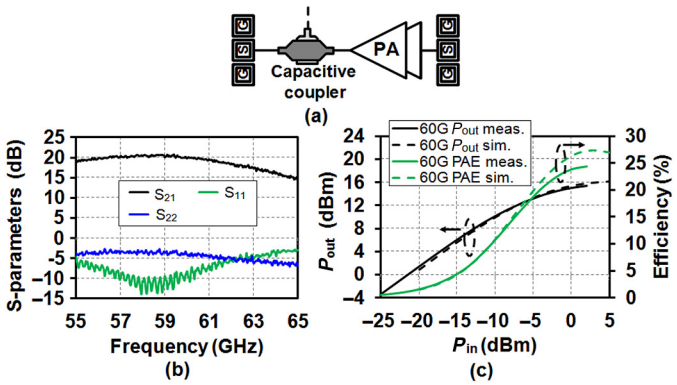

Fig. 18. (a) Measured PA break-out diagram consisting of the two-stage two-stacked class-E-like PA and capacitive coupler. (b) Small-signal S-parameters. (c) Measured and simulated output power and PAE versus input power at 60 GHz.

amplitude imbalance less than 1 dB [Fig. 17(d)]. The dc power consumption of the RF canceler is 44 mW.

The two-stage, two-stacked class-E-like PA with the 18 dB capacitive coupler at the output (simulated insertion loss of 0.3 dB at 60 GHz) is also characterized [Fig. 18(a)]. The cancellation path is powered ON with the lowest attenuation setting to present $\approx 50\Omega$ at the coupled port in Fig. 18(a). Fig. 18(b) and (c) present the small-signal and large-signal measurement results. The PA has a peak small-signal gain of 20.6 dB at 59 GHz, and a saturated output power of 15.4 dBm with 25.5% drain and 24.4% power added efficiencies at 60 GHz. The saturated output power is better than 13.7 dBm over 56–65 GHz. The large signal simulation results follow the measurements quite well.

B. TX and RX Measurements

Static measurements of the TX are performed by applying a constant digital data stream to the BPSK modulator (transmitting all zeros). Fig. 19(a) shows the TX output power versus the LO input power for different LO frequencies. A peak TX saturated output power of 15 dBm is achieved at 57 GHz with a peak system drain efficiency of 15.3%, including the doubler which is shared by the RX path. The LO–TX conversion gain, presented in Fig. 19(b), is better than 15 dB at an input power level of -6.5 to -4 dBm over 57–64 GHz. The measured TX saturated output power shown in Fig. 19(c) is more than 11.5 dBm from 56 to 66 GHz.

Fig. 20(a) shows the RX power conversion gain in the four IEEE 802.11ad channels for highest, lowest, and two intermediary selected gain settings with an LO power of 5 ± 0.3 dBm at the doubler input. The peak RX conversion gain is 40 dB in channel-3 with a 3 dB bandwidth of 2.2 GHz and gain control range of 20.8 dB. The gain control range is higher than 18 dB in all the channels. The RF gain across frequency is measured by sweeping RF and LO together to keep IF fixed at 120 MHz and superimposed in Fig. 20(a). The RX draws 56 mA from a 1.2 V supply. Fig. 20(b) presents the RX output power and conversion gain versus the input power in high-gain mode in the four channels. The RX has an input-referred 1 dB compression point of -32, -38, -39.8, and -36.6 dBm in channels 1, 2, 3, and 4, respectively. The RX noise figure shown in Fig. 20(c) is measured using gain method (cold noise) in high-gain mode and a state-of-the-art NF as low as 4 dB is achieved in channel-3.

C. System-Level Measurements

Fig. 21 shows a photo of the mm-wave PCB with the 60 GHz antennas used for cancellation and link measurements. The

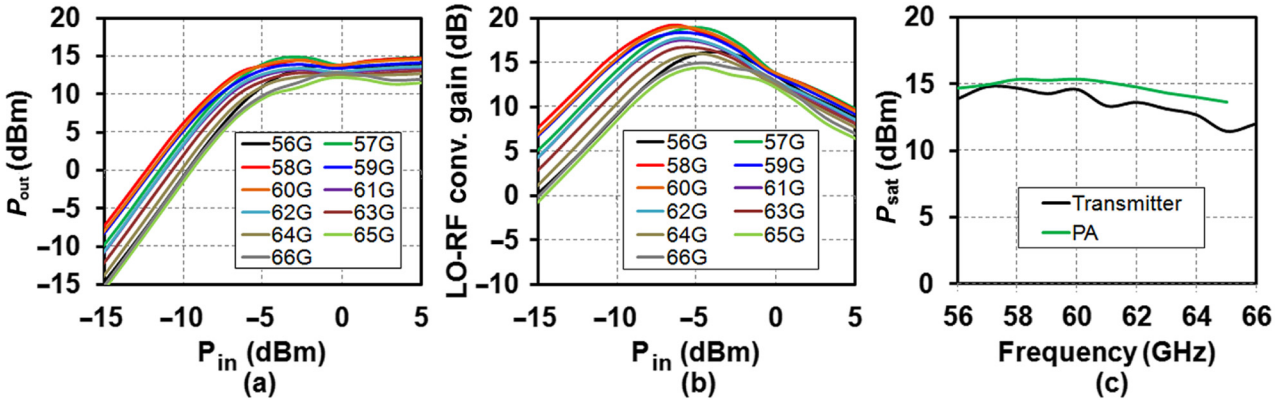

Fig. 19. TX CW large-signal measurements (transmitting all 0s). (a) TX output power versus LO input power. (b) LO-to-RF conversion gain of the TX versus LO input power. (c) PA and TX saturated output power versus frequency.

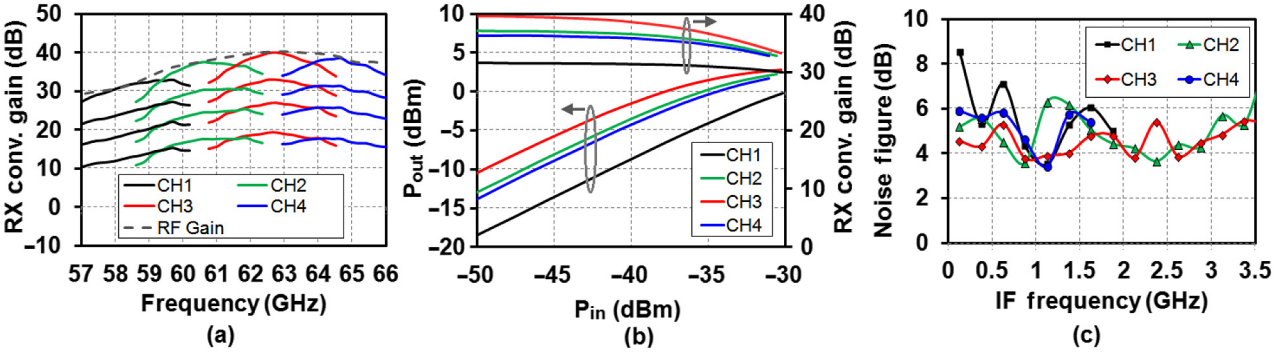

Fig. 20. RX measurements in all 4-IEEE channels. (a) RX conversion gain for highest, lowest, and two intermediary gain settings and peak RF gain across frequency. (b) Baseband output power and RX conversion gain versus RF input power for highest gain setting. (c) RX noise figure versus IF frequency for highest gain setting.

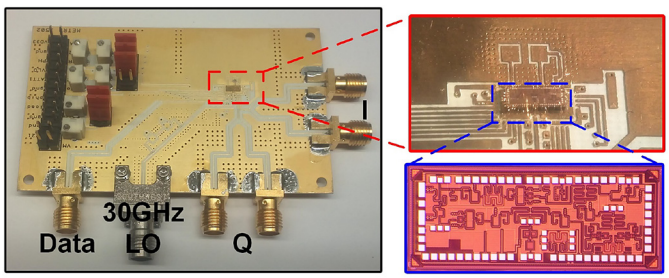

Fig. 21. Photo of the mm-wave PCB used for system-level measurements.

transceiver die directly sits on the PCB without cavity and is thinned down to 100 μm to reduce the length of the 30 and 60 GHz wirebonds. Additionally, three wires per mm-wave pad are bonded to reduce the wirebond inductance further (estimated L_{WB} is $\approx 100-150$pH and forms an artificial transmission line with 25 fF shunt on-chip and on-PCB pad

The SI at the RX output is characterized across frequency. The antenna and RF cancellation are configured together manually in the measurement. Dynamic SIC adaptation is beyond the scope of this paper. Controlling antenna and RF cancellation simultaneously gives flexibility in setting the SIC and SIC BW together. Fig. 23(a) shows the total SI suppression referenced to the TX output ($P_{\mathrm{TX}} = 11 \pm 0.4$ dBm). Another board consisting of only cross-polarized TX and RX antennas is used to measure the nominal TX-to-RX isolation. With antenna and RF cancellation together, a total SI suppression of >70 dB is achieved over a cancellation bandwidth of 1 GHz centered at 59 GHz. Fig. 23(b) shows the individual contribution of the antenna and RF cancellation. Since antenna and RF cancelers are controlled together, the values on Fig. 23(b) cannot be interpreted as the maximum achievable antenna and RF cancellation individually. Effect of environmental reflections on SI suppression is investigated by bringing a copper reflector close to the transceiver PCB.[4] The reflector 1.5 cm away from the antennas, as shown in Fig. 23(c), degrades the SI suppression by 10 dB from 58.5 to 59.5 GHz. We can recover the performance by only reconfiguring the antenna cancellation while leaving the RF canceler untouched, verifying its capability to combat the environmental reflections. It should be noted that higher propagation losses at mm-wave frequencies work in favor of FD since it alleviates the effect of environmental reflections on SI suppression. Fig. 23(d) shows that the RX output noise floor does not change when the RF canceler is activated (the TX was OFF in this measurement), in agreement with our system-level analysis.

[4]Wave reflection arises as a result of mismatch between the plane wave impedance ($Z_i \approx 377\ \Omega$) and the reflector's surface impedance. Copper has a very high conductivity which leads to a very low surface impedance, making it a very good reflector. Therefore, using copper enables us to test SIC under a very stringent condition [42].

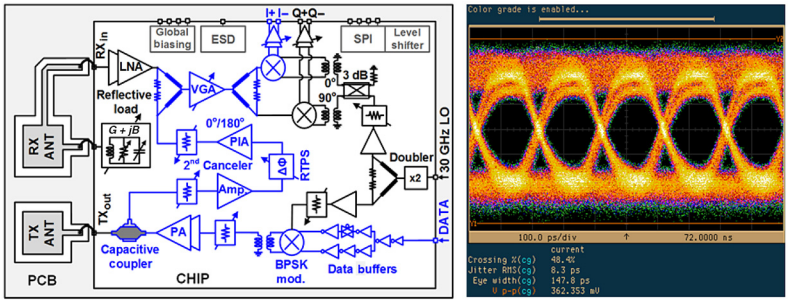

Fig. 22. TX–RX 5 Gb/s BPSK loopback test through the cancellation path.

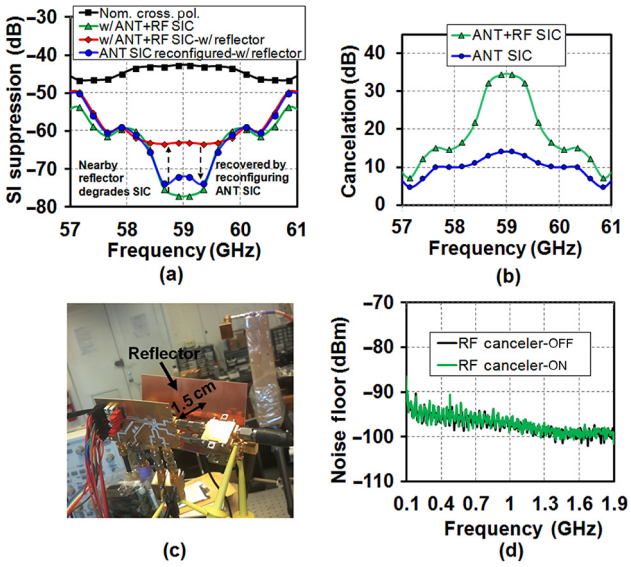

Fig. 23. (a) Measured SI suppression across frequency with antenna and RF cancellation configured. (b) Measured antenna and RF SIC. (c) Reflector is brought 1.5 cm away from the antennas to measure the effect of environmental reflections on SIC. SI suppression degrades due to the reflector, but it can be recovered by reconfiguring the antenna cancellation. (d) RF canceler's effect on the RX output noise (RBW = 51 kHz).

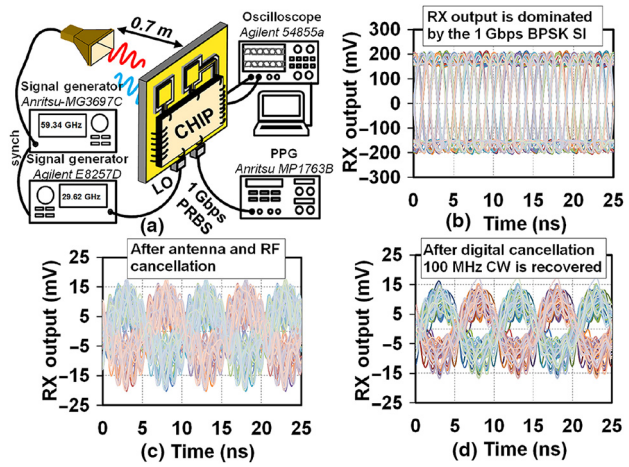

Fig. 24. (a) FD link setup. A CW signal at 100 MHz offset from the LO frequency is transmitted as the desired signal with a similar EIRP to our TX, whereas our 60 GHz transceiver transmits a 1 Gb/s BPSK signal. (b) RX output is dominated by 1 Gb/s BPSK SI when TX is on without SIC. (c) Desired signal is captured with some residual SI when antenna and RF SIC are engaged. (d) Desired signal is captured with a SINDR of 7.2 dB after DSIC.

TABLE I
SUMMARY OF FULL-DUPLEX TRANSCEIVER PERFORMANCE

Implementation	**Technology**	45 nm SOI CMOS
	Chip area	1.3 mm x 3.4 mm
Transceiver metrics	**Frequency**	57–66 GHz
	Peak RX conv. gain	40 dB (IEEE Channel-1) 32.7 dB (IEEE Channel-2) 37.7 dB (IEEE Channel-3) 38.2 dB (IEEE Channel-4)
	RX gain control range	~18 dB (IEEE Channel-1) ~20 dB (IEEE Channel-2) ~21 dB (IEEE Channel-3) ~21 dB (IEEE Channel-4)
	RX IP1dB (high-gain mode)	–32 dB (IEEE Channel-1) –38 dB (IEEE Channel-2) –40 dB (IEEE Channel-3) –37 dB (IEEE Channel-4)
	RF NF	4 dB
	TX output power	11-15 dBm at 56–66 GHz
	Peak TX efficiency	15.3% at 57 GHz
	Data rate	>5 Gbps[1]
FD metrics	**On-chip ANT+ RF SI suppression**	>70 dB (ANT+RF)
	SIC BW	1 GHz at 59 GHz
	TX ANT gain degradation due to ANT SIC	1.1 dB at 60 GHz (Simulated)
	TX ANT gain degradation due to ANT SIC	0.18 dB at 60 GHz (simulated)
	RX NF degradation due to RF SIC	Negligible (Measured)
	RX NF degradation due to ANT SIC	0.52 dB at 60 GHz (simulated)
	FD link	0.7 m (SINDR = 7.2 dB)[2]
Power consumption	**TX+TX-side LO dist**	206 mW[3]
	RX+RX-side LO dist	111 mW
	RF canceler	44 mW

[1]Loop-back test through the RF Canceler. A 1.485 Gbps video stream has been sent through the transceiver in half duplex mode over 1 m link distance [44].
[2]In conjunction with digital cancellation in MATLA.
[3]Includes doubler power consumption.

Finally, a simple same-channel FD link is demonstrated over 0.7 m (the demo video is available in [43]). Fig. 24(a) depicts the demonstration setup. A 24 dBi horn antenna transmits a CW signal from an Anritsu MG3697C at 59.34 GHz

TABLE II
COMPARISON TO STATE-OF-THE-ART 60 GHz CMOS TRANSCEIVERS

	This Work	[2]	[4]	[6]	[7]	[8]
Technology	45 nm SOI CMOS	65 nm CMOS	40 nm CMOS	90 nm CMOS	65 nm CMOS	40 nm CMOS
Chip area	1.3 mm x 3.4 mm	~8.6 mm x 8.1 mm	5.6 mm x 4.7 mm	~3.75mm x 3.6mm	4.2 mm x 4.2 mm	12.5 mm^2
Number of elements	1TX/1RX	32TX/32RX	16TX/16RX+1	1TX/1RX	1TX/1RX	4TX/4RX
Duplexing	Half/full-duplex	Half-duplex	Half-duplex	Half-duplex	Half-duplex	Half-duplex
RX single-element conv. gain	40 dB	–	–	60 dB	23 dB	45 dB
RX single-element NF	4 dB	<10 dB	<10 dB (2 dB switch)	7.1 dB	<4.9 dB	7.9–8.7 dB (SSB)
TX single-element output power	+15 dBm	+9 dBm[3]	>+8 dBm	+8 dBm	+5.6 dBm	+10.8dBm[3](Class-A) +8dBm[3](Class-AB)
TX total EIRP	+18.3 dBm (Peak CW)	+28 dBm (at –19 dB EVM)	+24 dBm (at –23 dB EVM)	+8.5 dBm (at –22 dB EVM)	–	–
Peak TX efficiency	15.3%[5] / 23%[6]	22% (PA Efficiency)	<7.4% (PA at OP_{1dB})	16.4% (PA) 1.7% (entire TX[6])	–	6.6%[7] (Class-A) 4.3%[7] (Class-AB)
Data rate	>5 Gbps[1]	3.8 Gbps at 50 m	4.6 Gbps at 10 m 3 Gbps at 20 m	1.8 Gbps at 0.4 m	3.1 Gbps at 1.8 m (QPSK) 6.3 Gbps at 0.05 m (16-QAM)	3.5 Gbps at 3.6 m (QPSK) 7 Gbps at 0.7 m (16-QAM)
SI suppression	>70 dB (ANT+RF)	NA	NA	NA	NA	NA
SIC BW	1 GHz at 59 GHz	NA	NA	NA	NA	NA
TX P_{DC}	206 mW[2]	1820 mW[6]	1190 mW[6]	347 mW[6]	319 mW[6]	724 mW(Class-A)[6] 584mW(Class-AB)[6]
RX P_{DC}	111 mW	1250 mW[6]	960 mW[6]	274 mW[6]	223 mW[6]	397 mW[6]
canceler P_{DC}	44 mW	NA	NA	NA	NA	NA

[1]Half-duplex mode measured with loop-back test through the RF canceler. Supports 1080p/60 Hz/8 bit video stream (1.485Gbits) over 1 m [45].
[2]Includes doubler power consumption as well.
[3]Output 1 dB compression point.
[4]With TX side LO distribution power consumption.
[5]Without TXside LO distribution power consumption.
[6]Includes synthesizer.
[7]Reported as $\mathrm{P_{1dB}}$/ $\mathrm{P_{DC}}$.

with an effective isotropic radiated power (EIRP) similar to our TX ($\approx$ 20 dBm). Our TX is configured for highest CW output power setting, resulting in an estimated EIRP of 18.3 dBm ($P_{\mathrm{TX}} = 14.3$ dBm, simulated TX antenna gain of $G_{\mathrm{TX}} = 4.5$ dBi and assuming a chip-to-PCB transition loss of 0.5 dB based on EM simulation). Our transceiver transmits a 1 Gb/s BPSK signal (SI) with an LO frequency of 59.24 GHz (100 MHz offset between the desired CW signal and LO). The RX output is monitored and captured using an Agilent 54855A oscilloscope with 6 GHz BW, essentially an 8 bit 20 GSPS ADC. In the absence of antenna and RF SIC, the RX output is dominated by SI [Fig. 24(b)]. Antenna and RF SIC enable the discerning of the 100 MHz desired CW signal in Fig. 24(c). In this plot, the captured signal is shifted by half-cycle and superimposed to show the signal quality visually like an eye-diagram. Digital SI cancellation (DSIC) is performed on the digitized signal in MATLAB using a 100-taps adaptive LMS filter with varying step size μ to reduce the settling time of the filter coefficients. To this end, our code initially uses a large step size of $\mu = 0.8$ during the first 80 k samples for coarse estimation of the filter weights, and as the weights converge to their final values, μ is dropped by half for every subsequent 20 k samples. The LMS filter settles in a total of 320 k samples, corresponding to a settling time of 16 μs. As can be seen in Fig. 24(d), DSIC further suppresses the SI, resulting in an even cleaner received signal in Fig. 24(d) with an SINDR of 7.2 dB. To the best of our knowledge, this work achieves the highest integration level among FD transceivers irrespective of the operation frequency and demonstrates a simple FD link for the first time using IC technology.

D. Performance Summary and Comparison

Table I summarizes the transceiver performance. Table II compares this work to other published state-of-the-art 60 GHz CMOS transceivers. It is worth repeating that, different from the other 60 GHz systems, which are generally mature phased-array systems, this work brings a new concept (mm-wave FD) to the table. Additionally, the comparison shows that this work surpasses the other works in the table in output power and NF on a per-element basis as well as TX efficiency, while not our focus. Further, it has an EIRP which is better than other single-element designs and even comparable with multielement designs. A 1080p/60 Hz/8 bit 1.485 Gb/s video stream has been sent through our transceiver in half-duplex mode over 1 m link distance [44], showing that this work can support high-speed file transfer between mobile devices.

VI. Conclusion

This paper presented a fully integrated 60 GHz zero-IF transceiver with polarization-based wideband antenna cancellation, RF, and digital cancellation for FD applications. The antenna cancellation can be electronically reconfigured by the transceiver IC to combat environmental reflections. The antenna and RF cancellation together provide a total SI suppression of >70 dB over 1 GHz bandwidth. In conjunction with DSIC implemented in MATLAB, a simple FD link using RFIC technology is demonstrated for the first time (irrespective of frequency) over 0.7 m. Combining FD operation with beam-steering capability is essential to realize the true benefits offered by mm-wave FD. This is a remaining challenge for future research.

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Tolga Dinc (S'09) received the B.S. and M.S. degrees in electrical engineering from Sabanci University, Istanbul, Turkey, in 2010 and 2012, respectively. He is currently working toward the Ph.D. degree in electrical engineering at Columbia University, New York, NY, USA.

From 2010 to 2012, he was a Research Assistant with Sabanci University and worked on the design of SiGe BiCMOS front-end circuits for X-band phased arrays. In the summer of 2015, he was a Design Engineering Co-Op at Texas Instruments, Dallas, TX, USA. His research interest include end-to-end design of mm-wave integrated systems for high-speed communication applications.

Mr. Dinc was the recipient of the 2010 MTT-S Undergraduate/Pre-Graduate Scholarship Award, the 2012 Sabanci University Gursel Sonmez Research Award, and the IEEE RFIC Symposium Best Student Paper Award (1st Place) in 2015.

Anandaroop Chakrabarti (S'11) received the B.Tech. degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India, in 2010, and the M.S. degree in electrical engineering from Columbia University, New York, NY, USA, in 2011, where he is currently working toward the Ph.D. degree.

In the summer of 2013 and 2014, he was a Research Intern with the IBM T. J. Watson Research Center, Yorktown Heights, NY, USA, working on power amplifiers in SiGe 9HP and techniques to reduce the phase noise of silicon oscillators. His research interests include mm-wave and RF circuits and systems in silicon, digital-intensive transmitter architectures, massive mm-wave multi-input-multi-output (MIMO) systems, and related applications.

Mr. Chakrabarti was the recipient of the IEEE Microwave Theory and Techniques Society (MTT-S) Graduate Fellowship in 2013, the Qualcomm Innovation Fellowship in 2014, and a co-recipient of the IEEE RFIC Symposium Best Student Paper Award (1st Place) in 2015.

Harish Krishnaswamy (S'03–M'09) received the B.Tech. degree in electrical engineering from the Indian Institute of Technology, Madras, India, in 2001, and the M.S. and Ph.D. degrees in electrical engineering from the University of Southern California (USC), Los Angeles, CA, USA, in 2003 and 2009, respectively.

In 2009, he joined the Department of Electrical Engineering, Columbia University, New York, NY, USA, where he is currently an Associate Professor. His research interests include integrated devices, circuits, and systems for a variety of RF, mm-wave and sub-mm-wave applications.

Dr. Krishnaswamy serves as a member of the Technical Program Committee (TPC) of several conferences, including the IEEE International Solid-State Circuits Conference (2015–present) and IEEE RFIC Symposium (2013–present). He was the recipient of the IEEE International Solid-State Circuits Conference (ISSCC) Lewis Winner Award for Outstanding Paper in 2007, the Best Thesis in Experimental Research Award from the USC Viterbi School of Engineering in 2009, the Defense Advanced Research Projects Agency (DARPA) Young Faculty Award in 2011, the 2014 IBM Faculty Award, and the 2015 IEEE RFIC Symposium Best Student Paper Award (1st Place).