Matching the Power, Voltage, and Size of Biological Systems: A nW-Scale, 0.023-mm^3 Pulsed 33-GHz Radio Transmitter Operating From a 5 kT/q-Supply Voltage

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***Abstract*—This paper explores the extent to which a solid-state transmitter can be miniaturized, while still using RF for wireless information transfer and working with power densities and operating voltages comparable to what could be harvested from a living system. A 3.1 nJ/bit pulsed millimeter-wave transmitter, 300 μm by 300 μm by 250 μm in size, designed in 32-nm SOI CMOS, operates on an electric potential of 130 mV and 3.1 nW of dc power. Far-field data transmission at 33 GHz is achieved by supply-switching an LC-oscillator with a duty cycle of 10^{-6}. The time interval between pulses carries information on the amount of power harvested by the radio, supporting a data rate of $\sim$1 bps. The inductor of the oscillator also acts as an electrically small ($\lambda/30$) on-chip antenna, which, combined with millimeter-wave operation, enables the extremely small form factor.**

***Index Terms*—Antennas, low power design, monolithic integrated circuits, radio frequency oscillators.**

I. Introduction

SOLID-STATE systems and biological systems have many complementary capabilities. For example, solid-state systems are uniquely capable of coupling to the radio-frequency (RF) electromagnetic spectrum for the transfer of information, while biological systems have capabilities for specific molecular recognition and the exploitation of biochemical energy sources. Nevertheless, biological systems and solid-state systems are characterized by fundamentally different physical form factors, power densities, and operating voltages, which create many challenges in mating these functions, most evident in the area of implanted medical devices [1].

In this work, we explore the extent to which solid-state systems can be miniaturized, while still using RF for wireless information transfer and while working with power densities and operating voltages comparable to what could be harvested from a living system. In our case, the radio transmitter is of the scale of 300 μm, the size of the vacuoles of large monads, such as *Thiomargarita namibiensis* (Fig. 1(b)). These vacuoles are reported to have metabolic rates on the nW scale [2], most of which support a proton motive force (PMF) across the membrane that could be harnessed to power such a system.

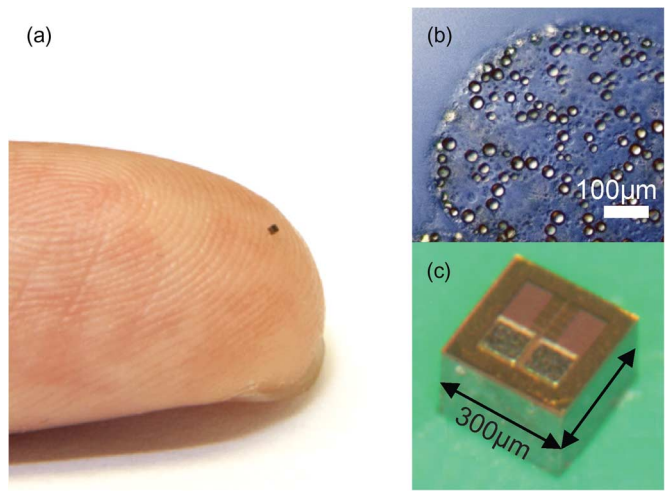

Fig. 1. (a) Transmitter on fingertip and (b) *Thiomargarita namibiensis*, at the same scale with (c) die photo.

We explore fundamental limits to the minimum power, voltage, and size achievable for such solid-state systems. Using thermodynamic arguments, Landauer showed that there is a minimal energy required for computation at the level of $kT \ln 2$ $\sim$2.85 zJ at room temperature per bit [3]. Practical minimum energies for CMOS circuits performing active computation are achieved with subthreshold operation [4]–[6] in which leakage power is balanced against dynamic power dissipation. In our case, communications requirements demand power levels significantly above the average available power. This requires duty-cycling the solid-state system, in which long periods of inactivity are time multiplexed with substantially shorter periods of communication activity.

The lowest supply voltage at which a circuit can operate is set by the need to achieve a minimum on-current-to-off-current (I_{on}/I_{off}) ratio in transistors. With digital logic involved, a supply voltage of $\sim 4kT/q$ is needed to restore a digital state with static CMOS [7]. Since in practice, higher supply voltage levels are needed to meet other circuit requirements, such as

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transistor gain for startup in analog oscillators, efficient voltage multiplication that can start-up at the available input supply voltage at the front-end is an important component in these systems.

The size of the system is limited by the need to couple to RF radiation efficiently. Small loop antennas have small radiation resistance and high reactance, making it difficult to deliver power to them. The amount of radiation produced by an ideal small loop antenna is determined by the radiation resistance $R_{rad} = 20\pi^2(C/\lambda)^4$, where C is loop circumference and λ is wavelength [8]. For an ideal 300 μm diameter loop antenna, R_{rad} is 22.8 mΩ and 0.693 $\mu\Omega$, respectively, at 33 GHz and 2.45 GHz. The latter will inevitably be dwarfed by the ohmic resistance of the antenna, dictating higher frequencies of operation for our system.

The transmitter developed here consumes 3.1 nW in a nearly cubic 300 μm by 300 μm by 250 μm form factor (Fig. 1) in 32-nm SOI CMOS. These lower power levels are achieved through extreme duty-cycling (10^{-6}) of an LC millimeter-wave oscillator, in which the inductor is repurposed as an electrically small $(\lambda/30)$ electromagnetic (EM) radiator. Power is integrated for about a second to provide the energy for an approximately 1 μs-wide 33 GHz pulse by gating of the oscillator power supply. The large amount of capacitance required for energy storage ($\sim$14 nF on the chip) is achieved through deep-trench capacitors extending 3.6 μm into the substrate. A switched-capacitor voltage multiplier boosts a 100–190 mV input voltage to over 300 mV to provide for oscillator startup, achieving a continuous-wave (CW) equivalent isotropically radiated power (EIRP) of more than -50 dBm and minimum reading distance of 18 cm at 10 dB SNR. The interval between pulses is inversely proportional to the energy stored, meaning that it carries information on the amount of power harvested by the radio. This information is encoded in the radio pulse stream at a bit rate of approximately 1 bps. Section II describes in more detail the trade-offs between operating power, operating voltage, and system size and the need for extreme duty cycling of the LC oscillator. The resulting duty cycling of communications puts constraints on the receiver described in Section III. Section IV describes the considerations that went into the choice of carrier frequencies. Details of the implementation of the transmitter are given in Section V with measured results in Section VI. Section VII describes how variability affects circuit performance and Section VIII concludes.

II. Trade-Offs Between Operating Power, Operating Voltage, and System Size

Power consumption of a logic gate consists of both dynamic and static power. The dynamic power arises from the charging and discharging of capacitance, while the static power is due to subthreshold, gate, and junction leakage. Subthreshold leakage power which dominates the other sources of leakage in the deep-subthreshold regime determines the lower bound for power dissipation in our system. Shown in Fig. 2, this power is proportional to $V_{DD}e^{(qV_{DD}/nkT)}$, where n is an ideality factor, typically between 1 and 1.5 [9].

In our system, the on-chip radiating LC oscillator, however, requires higher startup voltages ($\sim$300 mV) than biologically available levels, which must be supplied by the on-chip voltage multiplier, and significantly higher operating power levels ($\sim$ 50 μW), both of which are noted in Fig. 2. The pair of cross-coupled devices in the oscillator must reach levels of current and voltage that ensure enough transconductance to overcome LC tank resistance and achieve startup, requiring near-saturation operation. This higher power and voltage is duty-cycled with an idle state operating at the input voltage (the power of which is also noted in Fig. 2) as described in Section III to achieve the required average power level. The system size is dominated by the on-chip single-turn inductor that also functions as an electrically small loop antenna. As the inductor becomes larger, the parallel resistance of the LC tank increases, requiring less g_m to overcome it for startup and reducing the required oscillator power consumption. Therefore, there exists a direct trade-off between system size and power consumption.

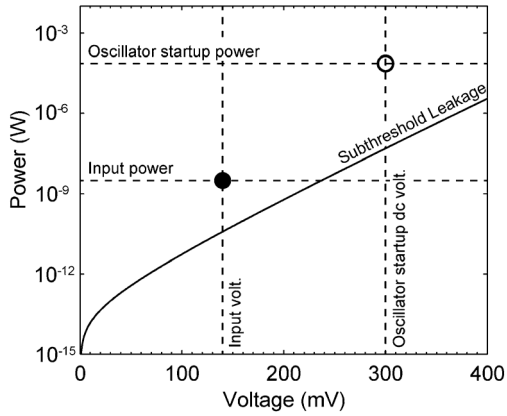

Fig. 2. Allowed power-voltage ranges of operation for the switched capacitor circuitry and LC oscillator are bounded by fundamental system constraints and biologically available limits. Two distinct operating points of the transmitter are marked as circles: idle (closed) and transmitting (open).

III. Communications Implications of Duty Cycling

To meet oscillator startup dc conditions far more power-consuming than the required average power (Fig. 2), we have implemented aggressive duty cycling of the oscillator on-off control circuit. The duty cycling event can be represented as a train of rectangular functions with two core parameters: duty-cycling ratio (DC) and single pulse width (T_{pulse}).

For detection, the power received from a monotonously-on signal source (P_R) must satisfy

$$P_R + 10\log_{10}(DC) > -174 + NF + 10\log_{10}(BW) \quad (1)$$

where DC is the duty cycle, NF is the noise figure of the receiver in dB, and BW is the bandwidth of the transmitted pulse. BW is inversely proportional to T_{pulse}.

The duty-cycling ratio is set to approximately 10^{-6} based on the ratio between the oscillator's continuous-wave dc power consumption and the available harvested power. The single pulse width that can be supported is limited by the achievable on-chip capacitive energy storage. Increased capacitive storage enables larger T_{pulse}, which reduces the bandwidth of the transmitted pulse, easing the link budget depicted in (1) at the expense of communication data rate. As we will further explain in Section V, the amount of on-chip capacitance for a chip area of 300 μm by 300 μm only supports pulse widths as wide as 1 μs. With our duty-cycling ratio, this amounts to a maximum achievable data rate of approximately 1 bps.

IV. Carrier Frequency Optimization

To improve radiation efficiency and load matching, RFID chips to-date preferably exploit off-chip antennas which are much larger than the associated ICs, increasing overall system size to millimeter- or centimeter-scale [10], [11]. In this work, we seek to bring the size of our radio transmitter down to the hundreds-of-microns size scale. Any antenna of this size will be electrically small unless the operating frequency is scaled to THz, which is impractical in today's scaled CMOS technologies.

The use of an on-chip integrated antenna eases integration at these size scales but brings additional losses in the metallization layers and silicon substrate [12]. We use an electrically-small loop antenna that also functions as the single-turn inductive load of an on-chip LC oscillator to further conserve space. We find that a 300 μm-diameter square loop antenna shows optimal low-power startup conditions at 33 GHz, bringing the transmitter into the millimeter-wave regime. There has been extensive recent work on highly-integrated millimeter-wave transceivers in CMOS capable of high-data-rate communication over moderate distances [13], [14]. Such transceivers commonly rely on high dc power in both the transmitter and the receiver due to the symmetric nature of the link to achieve such rates over moderate transmission distances. There has also been recent work on millimeter-wave/terahertz oscillators that operate near the f_{max} of the CMOS technology [15]. Such oscillators require the device to be biased at reasonable current densities to achieve the maximum available gain to meet stringent startup requirements.

In this application where the maximum available power is bounded by the desire to remain in the nW regime, we seek to maximize the amount of far-field radiation energy generated per unit dc power. To achieve this, we choose a carrier frequency that allows minimal power consumption while meeting the startup condition of the LC oscillator.

Transmission loss (T) is given by the following equation, where P_R is power received at the receiver antenna, P_T power inserted into the transmitter antenna, G_T and G_R antenna gains, λ the wavelength of the carrier frequency, and R the transmission distance:

$$T = \frac{P_R}{P_T} = G_T G_R \left(\frac{\lambda}{4\pi R}\right)^2 \times Absorp \qquad (2)$$

$Absorp$, the amount of radiation absorbed by conductive material surrounding the antenna, is dependent on frequency. This reduction in EM field penetration depth prevents the transmitter from operating deeply in a conducting medium, such as electrolytic buffer. Skin depth ($\delta = \sqrt{2\rho/\omega\mu_r\mu_0}$), the depth at which radiation power reduces by a factor of $1/e$, is on the order of a few tenths of a millimeter at 33 GHz in physiologically relevant media [16]. The asymmetric nature of the link will allow the use of high-gain antennas on the receiver side to overcome high absorption for small penetration distances. In the forthcoming analysis, we assume operation under very thin tissue, hence negligible amounts of radiation absorbed.

Two main factors contribute to $T - G_T$, the product of radiation efficiency and antenna directivity, and the path loss, $(\lambda/4\pi R)^2$, as governed by the Friis transmission equation. Fig. 3(a) shows the simulated T (as determined by the product of these two factors) for the antenna assuming a receiver antenna gain of 15 dB. The increase in path loss with frequency is more or less compensated by the increase in radiation efficiency of the transmitting antenna, resulting in a moderate decline with frequency.

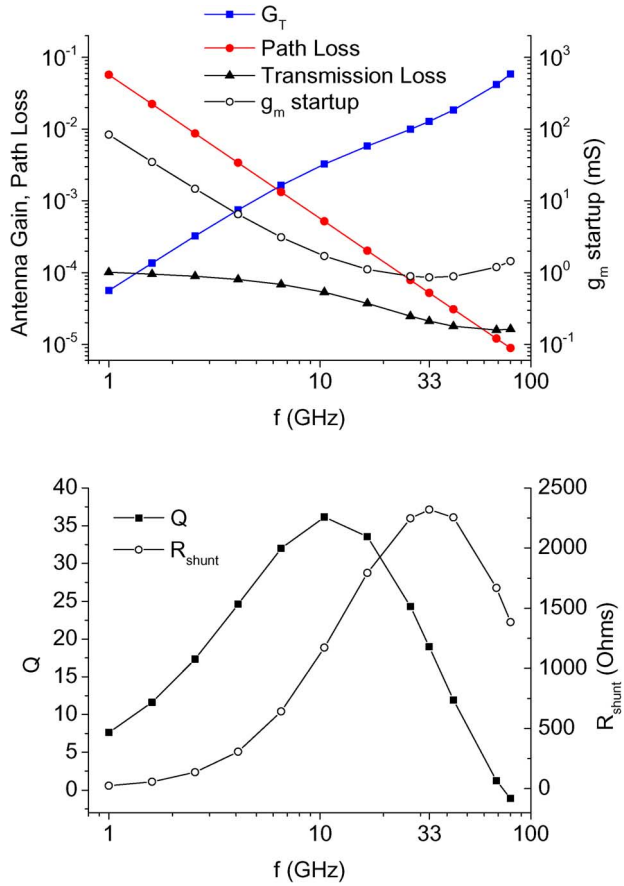

Fig. 3. (a) Frequency dependence of antenna gain (G_T), path loss ($(\lambda/4\pi R)^2$), and transmission loss (T); assumes 10 cm transmission distance and 15 dB G_R. $g_m startup = 2{R_{shunt}}^{-1}$ is also shown. (b) Q factor and R_{shunt} of 300 μm-wide loop antenna; simulated with IE3D assuming back-side thinning to 50 μm.

Given that T varies by a relatively small amount of 7.8 dB across the frequency range of 1–80 GHz, the choice of carrier frequency is determined by the start-up condition of the LC oscillator which varies by 97 times (19.9 in dB) over the same range: $g_m > 2{R_{shunt}}^{-1}$, where R_{shunt} is the oscillator's shunt resistance and g_m is the transconductance of the transistors M1 and M2 (Fig. 4(g)). When on, M1 and M2 are biased in weak inversion to consume minimal current, making g_m proportional to the drain current I_{bias} [9]. Fig. 3(a) shows that the value of g_m required for startup reaches a minimum at approximately 33 GHz.

The minimum g_m startup point (Fig. 3(a)) is caused by the peaking of R_{shunt}. The loop antenna in this design can be viewed as a single-turn inductor on top of a conducting substrate. For such an inductor of a fixed dimension, there is a frequency where its Q is maximum. At low frequencies, the Q of spiral inductors is dominated by series ohmic losses in the spiral metallization and increases with frequency [17]. At high frequencies, the spiral Q is dominated by shunt substrate losses and decreases with frequency [17]. In between, an optimal frequency for Q is observed. The net shunt resistance of the LC tank, R_{shunt}, will also exhibit a resultant peak frequency. It is at this frequency that the g_m for startup is minimized. For the

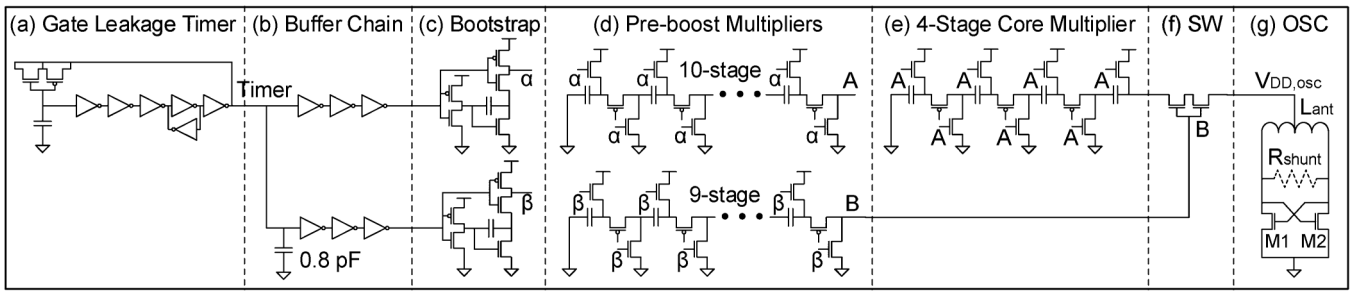

Fig. 4. System architecture.

single-turn inductor used here, this peak occurs at a frequency of approximately 33 GHz as shown in Fig. 3(b).

From Fig. 3(a), we find that at 33 GHz, startup $I_{bias} \approx 200\ \mu$A is approximately 17 times less bias current than would be required at an operating frequency of 2.45 GHz for the same form factor antenna, typical for many RFID tags, while resulting in only 4 dB less T, which can readily be overcome with improved gain on the receiver side. Our transmitter ICs are implemented with nominal oscillation frequencies (f_{osc}) of 29 GHz and 33 GHz by varying the sizes of M1 and M2.

V. Implementation

The transmitter system architecture is shown in Fig. 4. The entire system is controlled by an always-on $\sim$1 Hz timer. This relaxation oscillator uses leakage through a transistor gate of only 0.3 nA. The resulting clock controls a three-stage voltage multiplier which drives an LC oscillator, the inductor of which also acts as the system antenna. Constraints on available energy storage limit transmitted pulses to 1 μs duration and 200 μA current magnitude resulting in an effective duty cycle of 10^{-6}.

The chip is implemented in 32-nm SOI technology that offers deep-trench capacitors with nearly 60 times higher capacitance density (250 fF/μm^2) than metal-metal capacitors, making it an ideal energy storage device for the highly area-restricted system. These capacitors provide a total capacitance of 14 nF within the available chip area, which, if replaced with metal-metal capacitors, would occupy an area of 3 mm^2. They do, however, carry a series resistance of more than 100 Ω for each 5 pF of capacitance, which must be carefully managed in the design of the voltage multiplier. Additional series resistance comes from the switches of the voltage multiplier which are operating at I_{on}/I_{off} ratios of only 40 for the first stage. The output impedances for this converter is approximately 200 Ω, creating the potential for a large transient output voltage droop. To mitigate this, three stages of voltage boosting, all with current-starved gates, are employed to provide successively better switch function at each stage, as described in Section V-B below.

We describe in more detail the design of the voltage multiplier and radiating oscillator.

A. Ultra-Subthreshold Switched Capacitor Voltage Multiplier

Fig. 5 shows transient behavior of critical clock signal path node voltages involved in the three stages of voltage boosting. Starting from a 130 mV swing power supply, each successive stage achieves larger swing and faster switching speed, ultimately leading to the capacitors' rapid discharge of current into the oscillator.

The entire system is controlled by an always-on $\sim$1 Hz clock (Fig. 4(a)), composed of a gate-leakage unit followed by

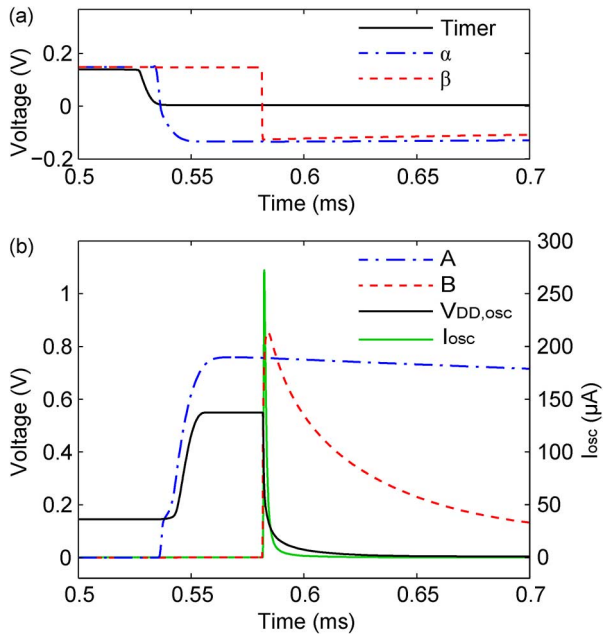

Fig. 5. Transient simulation of critical circuit node voltages and current during a capacitor-to-oscillator charge transfer event. The antenna radiates within the narrow peak of I_{osc}. Subplots (a) and (b) display the same time window but are separated for clarity. Legend is in agreement with Fig. 4.

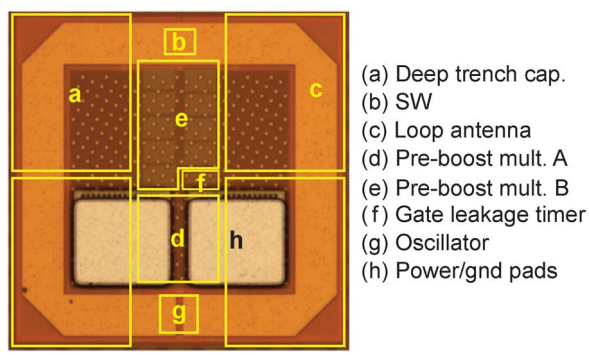

Fig. 6. Die photo with circuit positions noted.

a Schmitt trigger [18]. The 130 mV swing output of the gate leakage timer (Fig. 5(a), *Timer*) is input into two independent buffer chains, one of which is delayed by 50 μs with the addition of a non-tunable 0.8 pF deep trench capacitor. These two time-offset 130 mV square waves emerging from these chains each feed into a bootstrapped driver, producing output swings up to 250 mV. The bootstrapped output (α) and the delayed bootstrapped output (β) drive "pre-boost" voltage multipliers with ten and nine capacitors, respectively. The pre-boost output from the ten-stage multiplier (A) has a 750

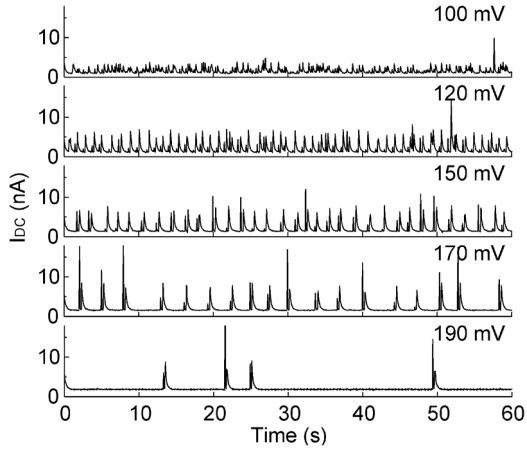

Fig. 7. Gate-leakage timer oscillatory transients at V_{DD} levels given above. Current was measured by dc-powering the power/gnd pads in Fig. 6(h).

mV swing and drives the switches of the four-stage core multiplier (Fig. 4(e)), producing a more-than-300 mV supply for the oscillator $(V_{DD,osc})$. The pre-boost output from the nine-stage multiplier (B), which has a 900 mV swing and is delayed approximately 50 μs from A, opens the switch (SW) between the capacitor tank of the core multiplier and the LC oscillator, biasing the cross-coupled pair above the startup condition of $\sim$ 200 μA current (I_{osc}) for 1–3 μs until the capacitance of the core multiplier is sufficiently discharged. The antenna radiates at 33 GHz while the oscillator startup condition is met.

This process repeats itself at each falling edge of the gate-leakage timer. The ratio of oscillator on-time to timer clock period is approximately 10^{-6}. To deliver a total of 0.15 nJ, computed from LC oscillator dc power consumption multiplied by pulse duration, to the oscillator in a single pulse requires 3.09 nJ be drawn from the input supply for an overall switched-capacitor efficiency of 4.9%. Ultra-subthreshold operation of the timing circuit produced an as-designed yield of 25% for these parts as a result of random variability in 32-nm CMOS as described in more detail in Section VII.

B. Millimeter-Wave Ultra-Low-Power Radiating Oscillator and Layout

To exploit a limited chip area of 300 μm by 300 μm, a single-turn loop antenna (Fig. 6(c)) acts as both the far-field radiator and the inductor of the LC oscillator. The loop is fabricated at the topmost metal layer with a path width of 40 μm and inductance of 553 pH at 33 GHz. Similarly, millimeter-wave operation is achieved with the capacitance of the LC tank provided only by the device capacitance of the cross-coupled transistors (Fig. 4(g)). Each minimum-length (40 nm) device is given a width of 13.1 μm. An nMOS-only oscillator is implemented as it improves the power generation efficiency of the oscillator due to the higher speed of nMOS transistors. The nMOS cross-coupled transistor pair is laid out with an arrangement suggested by Liang *et al.* that achieves maximal drain efficiency through reducing terminal parasitics [19].

The layout (Fig. 6) takes full advantage of the chip area bounded by the antenna perimeter. Deep-trench capacitors occupy much of the area under the loop inductor, providing 13.7 nF for the four-stage voltage multiplier. The center contains the metal-metal capacitors of the nine-stage pre-boost multiplier, which is kept as distant as possible from adjacent metals to minimize parasitic coupling. Other on-chip components including the bootstrap drivers and gate-leakage timer are symmetrically placed in the center of the chip in order to produce an unskewed antenna radiation pattern. Two 90 μm by 90 μm pads (Fig. 6(h)) are also symmetrically placed on-chip, inside the loop antenna, for the input power supply.

On-chip ESD protection is a challenge for the two power-ground pads. They are connected with two back-to-back ESD protection diodes. Although one diode in this approach is forward biased, simulation showed that for V_{DD} values below 200 mV, only 175 pA of leakage current is drawn, representing only 0.6% of total power consumption.

VI. Measured Results

Fig. 7 shows gate-leakage timer oscillatory transients with respect to changes in V_{DD}, observed indirectly through the supply current of the full chip. Periodic peaks in the system's current consumption (I_{DC}) suggest proper discharge of core multiplier deep-trench capacitors, thereby confirming timer oscillation. Oscillation is observed over the range of input supplies from 100 to 190 mV. This clock frequency (f_{timer}) reaches 1 Hz at a V_{DD} of 130 mV and inversely scales with voltage with a rate of $\sim$1 Hz/20 mV, agreeing with simulations. Each peak represents the timer's transition from discharge-state to charge-state.

The chip's RF transmission characteristics are studied with a 15 dB horn receiver antenna 10 cm away as presented in Fig. 8. Fig. 9 presents the duty-cycled oscillation recorded both as raw RF signal with a spectrum analyzer, and an IF signal after down-converting to $\sim$3 MHz by mixing with a 32.39 GHz carrier. Fig. 9(a) shows the spectrum analyzer output of the RF signal sampled in the frequency-domain with a 500 Hz bandwidth, but plotted against the time axis. The three traces indicate oscillator states of *on*, *off*, and 10^{-6} duty-cycled, respectively. The data confirms that the duty-cycled signal power level toggles between that of *on*- and *off*-states. Fig. 9(b) shows the same signal mixed to baseband using the setup in Fig. 8(a). The inset is a zoomed-in view of a single radiation pulse, showing that the LC oscillator transient reaches steady-state within the 1 μs pulse width.

Fig. 10(a) shows the measured phase noise of the 33.1 GHz oscillator at supply voltages of 335 mV (which is near the supply voltage provided by the voltage multiplier during pulsed operation) and 500 mV. At 10 MHz offset, the phase noise is

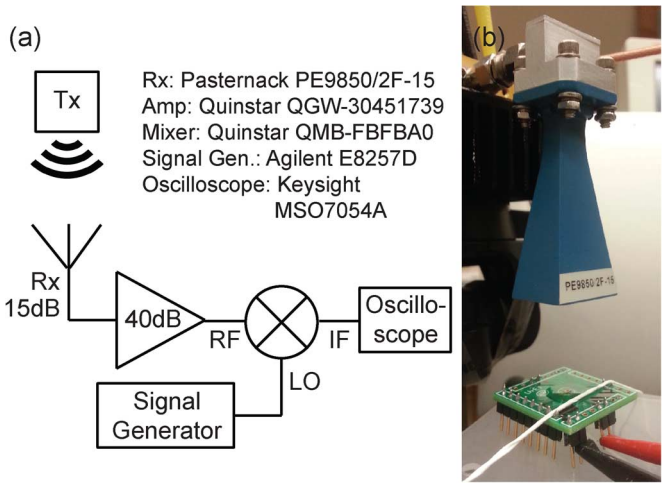

Fig. 8. (a) Schematic of RF measurement setup and (b) picture of horn receiver antenna at 10 cm transmission distance.

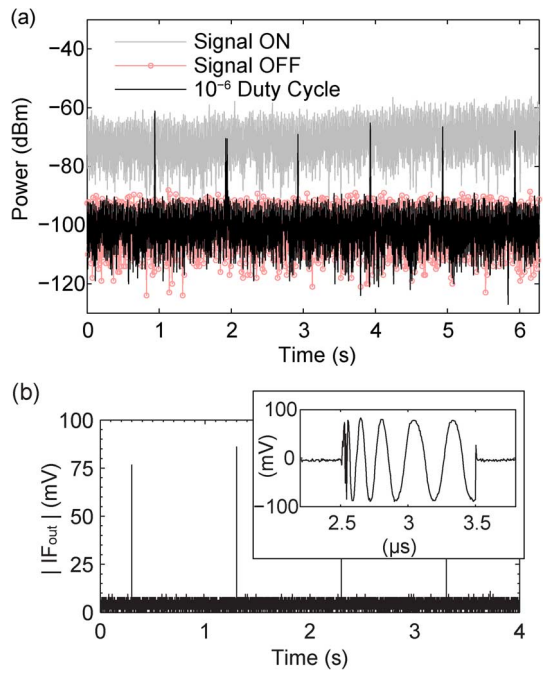

Fig. 9. Time-domain waveforms of (a) receiver output (RF) of 32.29 GHz oscillator monotonously-on, monotonously-off (noise floor), and 10^{-6} duty-cycled; (b) RF mixed to baseband (IF) with inset showing the zoom-in of a single peak. Measurements taken for $V_{DD,osc} = 300$ mV.

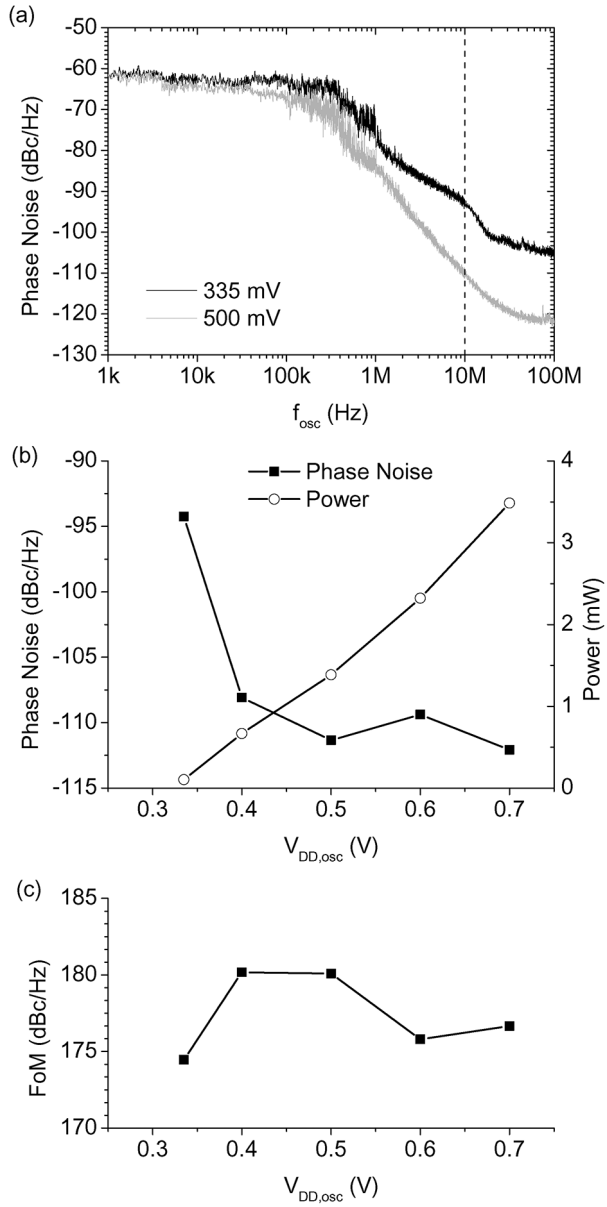

Fig. 10. (a) Oscillator phase noise at startup (335 mV) and higher (500 mV) supply voltages; (b) 10 MHz-offset phase noise and power; and (c) FoM across different $V_{DD,osc}$ levels.

-94.24 and -111.34 dBc/Hz, respectively. Fig. 10(b) shows the phase noise at 10 MHz offset across different supply voltages as well as the power consumption. It can be seen that phase noise generally improves with supply voltage. A popular figure of merit (FoM) that captures the trade-off between phase noise and power dissipation is $-L + 20\log(\omega_o/\Delta\omega) - 10\log(P_{DC})$, where L is the phase noise in dBc/Hz at an offset $\Delta\omega$ from the carrier frequency ω_o. Fig. 10(c) plots the FoM versus supply voltage. At a supply voltage of 335 mV, the power consumption is 0.104 mW and the FoM achieved is 174.5 dBc/Hz. At 500 mV, the FoM improves to 180.1 dBc/Hz.

The oscillator startup behavior as a function of bias voltage is characterized in Fig. 11, for modules designed for both 29- and 33-GHz f_{osc} operation. CW EIRP of -49.89 dBm and -56.40 dBm are achieved at oscillator startup voltages $(V_{DD,osc})$ of 0.284 V and 0.327 V for the 29 GHz and 33 GHz designs, respectively. Relatively low CW EIRP values are caused by the small dc power consumption of the oscillator and extremely small size of the antenna. EIRP for the 33 GHz module increases to -20.83 dBm at 0.5 V $V_{DD,osc}$.

Table I compares the performance of the transmitter with Pellerano *et al.*, an RFID chip operating at 45 GHz [11]. The energy consumed per transmitted bit is comparable between the two designs ($\sim$3 nJ/b), while we use only about 7% of the area (this number will only decrease when including the antenna size of Pellerano *et al.*, which has not been stated) and dc power that is more than three orders of magnitude smaller (but at 5000 times lower bit rate). Table I compares the designs using $(\text{bit} - \text{energy} \times \text{area})^{-1}$ as a second FoM, again, not including the antenna size of Pellerano *et al.* Fig. 12 reports the size of our system in comparison with other reported small wireless systems previously developed [20], showing our design to

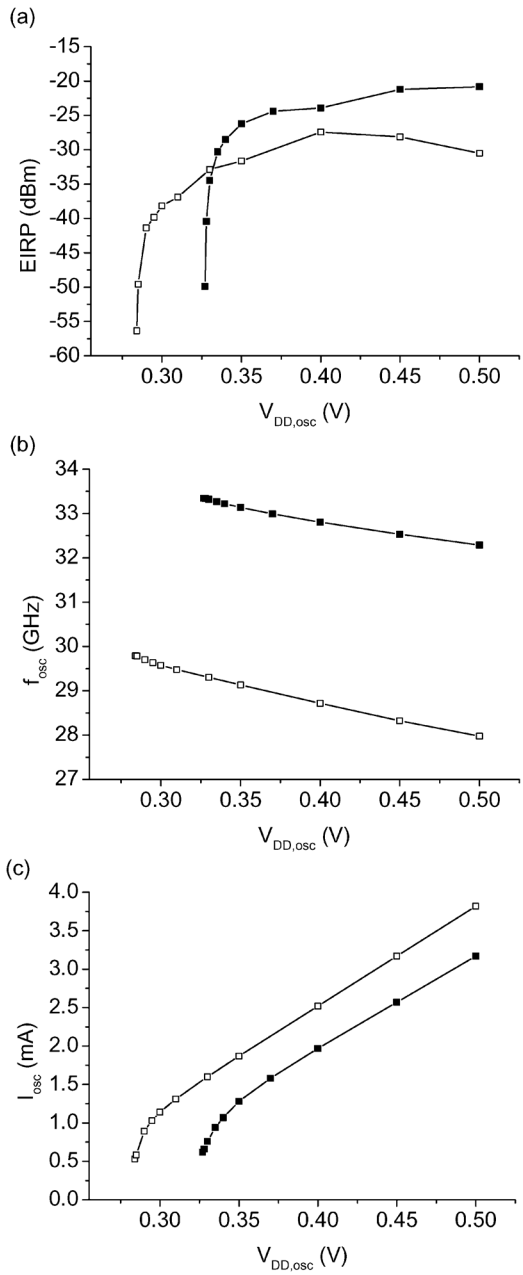

Fig. 11. RF oscillator characteristics of (a) EIRP, (b) f_{osc}, and (c) I_{osc} for 33 GHz (closed) and 29 GHz (open) designs versus $V_{DD,osc}$ (Fig. 4(g)). Measured = from a single die.

be more than one order of magnitude smaller by volume than any previously reported radio design.

VII. Variability

Stringent power and voltage conditions give rise to large performance variations in both the millimeter-wave oscillator and its control circuitry. The sensitivity of the oscillator's EIRP, dc power consumption, and carrier frequency with respect to $V_{DD,osc}$ (Fig. 11) makes it difficult to predict exact carrier frequencies. This requires careful sweeping of the narrow receiver bandwidth (<10 kHz) to find the carrier.

Current-starved buffer chains in the control circuit introduce timing variations that directly affect the amount of transmitted power. The gate-leakage timer frequency (Fig. 13(a)) is especially prone to mismatch variations, due to sensitivity of Schmitt trigger threshold levels in the ultra-subthreshold region. The varied durations of the gate-leakage-timer clock lead to varied durations in the oscillator discharge events, resulting in widely distributed bit rates across chips. An excessively high bit rate prevents deep-trench capacitors from charging fully, resulting in lower transmitted power.

Fig. 13(b) shows that oscillator discharge events occur across a wide range of peak locations and amplitudes. Timing uncertainty in the delay buffer chain (Fig. 4(b)) causes peaks to occur at different times. Longer idle time before the discharge leads to more leakage through CMOS switches, resulting in smaller values of I_{osc}. This is confirmed by the histograms in Fig. 14; there is a particularly large functionality variation in f_{timer} and average system power consumption. Among the 80 dice tested, a total of 18 pulsed with an expected clock frequency of ~1 Hz. Thirteen of these showed complete functionality. The rest lost functionality due to either insufficient ESD protection or PVT variations. The number of functional chips increased at higher supply voltages and power levels.

TABLE I
Transmitter Specifications

	This work	Pellerano *et al.* [11]*
Carrier frequency	33 GHz	45 GHz
System area	0.3 × 0.3 mm^2 (antenna included)	1.3 × 0.95 mm^2 (without antenna)
Reading dist. (equivalent 13 dB SNR)	12.7 cm**	1.3 cm*** (10^{-3} BER)
dc input power	3.1 nW	> 19 μW
Bit rate	1 bps	5 kbps
Energy cost per bit	~3.1 nJ	> 3.8 nJ
FoM, (bit-energy×area)$^{-1}$	3.6 nJ^{-1}mm^{-2}	< 0.2 nJ^{-1}mm^{-2}

*Values obtained/calculated based on input power of 2 dBm.

**Measured with 15 dB receiver antenna gain.

***Calculated for 3 dB receiver antenna gain.

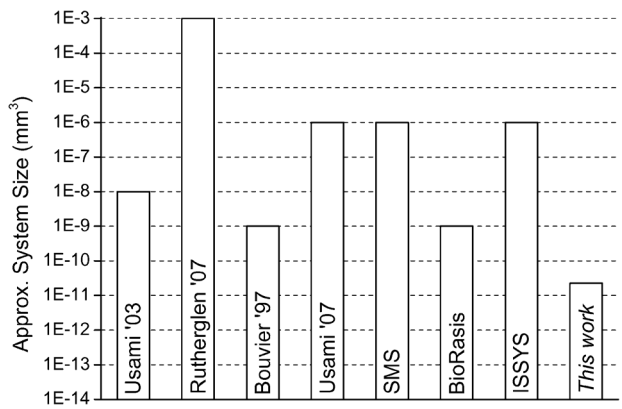

Fig. 12. System size comparison, antennas included, with other small radios: reproduced from [20]. From left, [21]–[24], and next three cited from [20].

VIII. Conclusion

In this work, we explored the limits of power, voltage, and size in the design of a radio transmitter. Achievable power levels are limited by subthreshold leakage, operating voltages by $4kT/q$, and size by the thermal noise floor at the receiver. Voltages and power levels are chosen to match those available

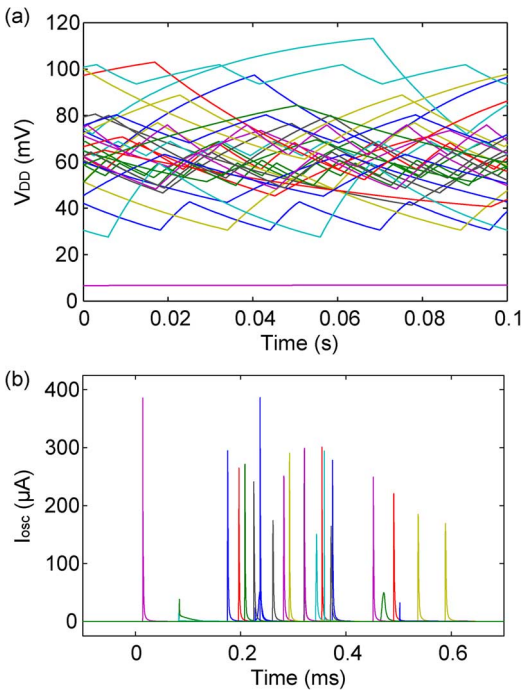

Fig. 13. 30 runs of Monte Carlo simulations showing timing uncertainty in (a) period of gate leakage timer, and (b) peak location and magnitude of antenna discharge current transients.

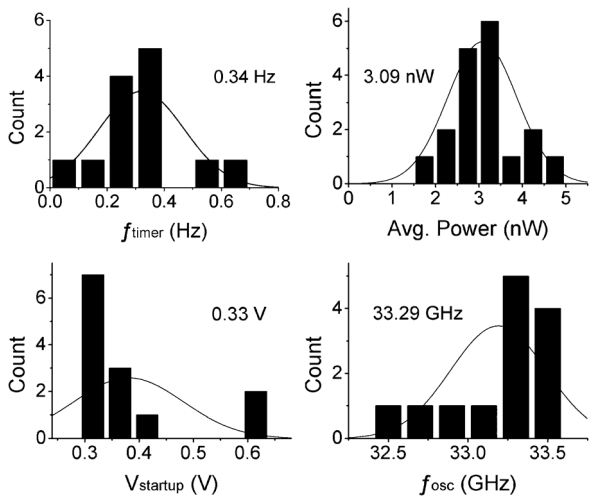

Fig. 14. Chip-to-chip performance distribution across 13 samples, with corresponding median values. $V_{startup}$ is the lowest value of $V_{DD,osc}$ to achieve 10 dB SNR at 10 cm reading distance. The histogram for average power has the benefit of 18 samples.

from biological transmembrane potentials. The goal of this effort was to explore the possibility of making a radio transmitter small enough and low-power enough to be powered by a single cell.

Extreme duty cycling (by a factor of 10^{-6}) and sub-Hz data transmission rates are key power-saving features of the design. Limitations in available power dictate simple modulation approaches, such as on-off keying or pulse-position modulation. In this prototype, the time interval between pulses carries information on the amount of power harvested by the radio. The ability to support on-off keying can be included with a single switch designed to be triggered by an electrochemical reaction. The seemingly low data rate of 1 bps is sufficient in monitoring biological processes, a considerable fraction of which change over much longer time scales.

Practical limitations in the design of a sub-millimeter-scale radio were also considered. Quality factor of on-chip passives limit duty-cycling and switched capacitor circuit efficiencies. Process variations have significant effects on the transmitter performance. To achieve yields greater than 25%, we had to operate at higher nominal voltages and power levels. Although the design has room for further optimization, the sensitivity of the Schmitt trigger/switched capacitor cascade against supply voltage levels and transistor mismatch entail a practical limit for performance yield. A mass deployment scheme is suggested to solve such uncertainty, which also takes full advantage of the extremely small system size and biological-level power density of the transmitter.

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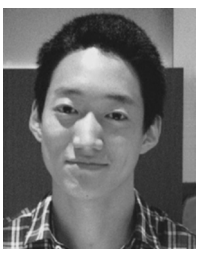

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