Analysis and Design of a 0.6- to 10.5-GHz LNTA for Wideband Receivers

Linxiao Zhang, Yang Xu, Karthik Tripurari, Peter R. Kinget, and Harish Krishnaswamy

***Abstract*—A low-noise transconductance amplifier (LNTA) for wideband receivers based on a g_m-boosted current mirroring topology that operates over 0.6- to 10.5-GHz is presented. g_m boosting relaxes the G_m and S_{11} bandwidth (BW) tradeoff and the noise figure (NF) and input matching tradeoff. The active feedback synthesizes a second-order input impedance profile that further extends the S_{11} BW. Despite the high G_m obtained over large BW, high linearity is maintained through the predistortion inherent in the current mirroring topology. The LNTA is used in a 65-nm CMOS wideband channelizing iterative downconversion receiver targeting spectrum and signal analysis for cognitive radio and performs active signal splitting across two paths with a total postlayout simulated G_m of 242 mS (170 and 72 mS in paths 1 and 2, respectively). S_{11} BW and G_m BW both exceed 10.5 GHz. Minimum LNTA NFs simulated in the two paths are 4 and 4.8 dB, respectively. Simulated wideband IIP3 and blocker P1dB are $+6$ and $+1.5$ dBm, respectively. Measurements of a direct conversion receiver in path 2 closely match simulations.**

***Index Terms*—Boosting, CMOS integrated circuits, current-mode circuits, distortion, software radio, transconductance, wideband.**

I. Introduction

CURRENT-MODE direct-conversion receivers employing a front-end low-noise transconductance amplifier (LNTA) driving passive mixers have become extremely popular for wideband receivers [1]–[4]. The LNTA is critical, as it must achieve wideband input matching with low noise penalty. High transconductance (G_m) must be achieved over a wide bandwidth (BW) to reduce the noise contribution of the baseband transimpedance amplifier (TIA). The out-of-band linearity is typically dominated by the input nonlinearity of the (single-stage) LNTA, as voltage gain is avoided prior to filtering in the baseband TIA. Cognitive-radio receivers performing spectrum and signal analysis are particularly challenging, as extremely wide instantaneous S_{11} and G_m BWs are required. Furthermore, very high G_m is required for receivers with multiple concurrent outputs [5].

A common instantaneously wideband LNTA architecture is the noise-canceling LNTA [2], [4] (initially introduced as a voltage-mode LNA in [6]), which uses a path to provide input matching and another to sense and cancel its noise [see Fig. 1(a)]. Complete noise cancellation requires two separate downconversion paths. A partial noise-canceling LNTA [1] combines the signal currents before downconversion at the cost of higher noise figure (NF) [see Fig. 1(b)]. Fundamentally, single-stage LNTAs employing a common-source (CS) transconductance amplifier exhibit an undesirable tradeoff between g_m and input parasitic capacitance, which translates to a G_m–BW tradeoff. Moreover, a CS stage's NF decreases as its g_m increases, giving rise to an NF–BW tradeoff [7]. This precludes the use of single-stage LNTAs in extremely wideband receivers, or receivers needing extremely high G_m.

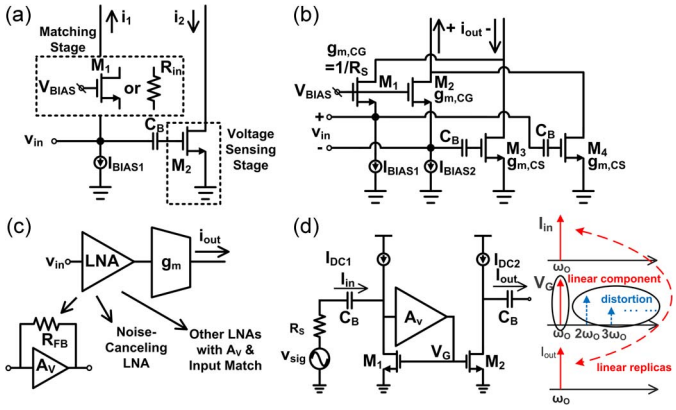

Fig. 1. High-level depictions of commonly used instantaneously wideband LNTA structures, namely, (a) complete noise-canceling LNTA, (b) partial noise-canceling LNTA, (c) voltage-mode LNA followed by a g_m cell, and the (d) proposed g_m-boosted current mirroring LNTA.

An alternate approach is a multistage LNTA with voltage gain to alleviate the G_m–BW–NF tradeoff [see Fig. 1(c)]. The voltage-gain stage can achieve broadband input matching in a number of ways, including resistive feedback, noise canceling [6], [8], distributed amplification [7], and others. However, the use of voltage gain typically compromises linearity.

In this brief, we present a multistage LNTA circuit based on a g_m-boosted current mirroring topology that maintains high linearity through its inherent predistortion [see Fig. 1(d)]. Since the voltage-to-current conversion distortion profiles are matched for M_1 and M_2, $I_{\rm in}$ and $I_{\rm out}$ have to be linearly scaled replicas of each other despite the distorted gate voltage V_G. The active feedback in the current mirroring architecture synthesizes a second-order input impedance with a zero that extends the S_{11} BW. This is similar to a gyrator operating on a load capacitor to synthesize an active inductance at the input that compensates for input capacitance. When compared with the partial noise-canceling LNTA as a baseline, the proposed LNTA achieves more than two times improvement in BW and

Manuscript received August 18, 2014; revised October 31, 2014; accepted December 3, 2014. Date of publication December 23, 2014; date of current version April 23, 2015. This work was supported by the DARPA CLASIC program. This brief was recommended by Associate Editor M. Onabajo.

The authors are with the Department of Electrical Engineering, Columbia University, New York, NY 10027 USA (e-mail: hk2532@columbia.edu).

Color versions of one or more of the figures in this brief are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2014.2385371

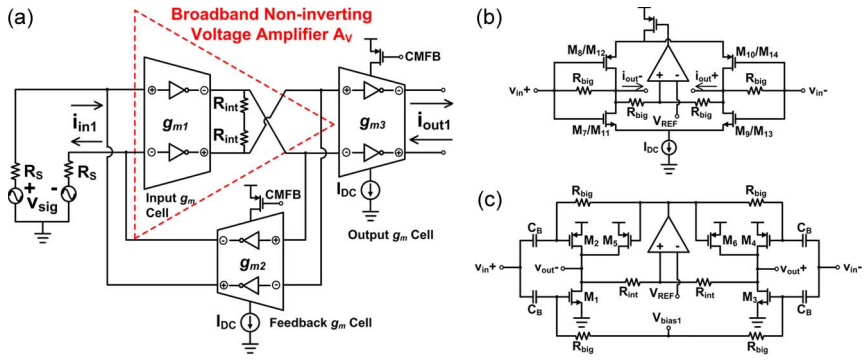

Fig. 2. (a) Circuit implementation of the proposed g_m-boosted current mirroring LNTA. (b) Circuit diagram of the g_m cells used to provide input matching and voltage-to-current conversion (g_{m2} and g_{m3}). (c) Circuit diagram of the voltage amplifier performing g_m boosting.

six times improvement in G_m for the same NF. The concepts are experimentally validated through measurements from a wideband channelizing receiver in 65-nm CMOS that uses this LNTA [5].

II. Tradeoffs in Conventional and Proposed LNTAs

The partial noise-canceling LNTA [see Fig. 1(b)] used in [1] is simulated to show the tradeoffs associated with conventional LNTAs. Increasing the width of $M_{3,4}$ while keeping the bias point constant will lead to a linear increase in $G_m = g_{m,\mathrm{CG}} + g_{m,\mathrm{CS}}$. However, this also gives rise to a linear increase in input node capacitive loading, which degrades the S_{11} BW. This G_m–BW tradeoff is simulated for the complementary implementation described in [1] as a baseline design and shown in Fig. 3(a). A parasitic $C_{\mathrm{pad}} = 300\ fF$ is assumed to model an electrostatic-discharge-protected input pad.

The partial noise-canceling LNTA NF is $1+\gamma$, where γ is the device excess noise factor [1]. This NF is independent of the sizing of $M_{3,4}$ [see Fig. 3(b)] because, while the noise contribution of the CS stages decreases with larger $M_{3,4}$, the LNTA deviates from the perfect noise-canceling condition, and the common-gate (CG) stages contribute more noise. In essence, this LNTA achieves the NF of a CG LNTA while achieving higher G_m at the expense of the S_{11} BW. In a complete noise-canceling LNTA [4], the CG noise is cancelled independent of $g_{m,\mathrm{CS}}$ at the expense of an extra downconverting path, enabling a CS stage as large as is allowed by the S_{11} BW to suppress NF.

Fig. 2 depicts the circuit diagram of the proposed wideband LNTA based on the g_m-boosted current mirroring principle. The complementary g_{m2} and g_{m3} CS cells form a current mirror, whereas g_{m1} loaded with R_{int} forms a voltage amplifier, i.e., A_V, that boosts their transconductance. Complementary implementation enables high linearity [9] and larger g_m for a given current. The decoupling of the g_{m3} cell from the input node implies that the S_{11} BW is limited by the input capacitance of g_{m1}, which can be smaller than the input stage of a single-stage LNTA to achieve the same overall G_m. It will be shown that the active feedback further extends the S_{11} BW. The voltage amplifier also improves the noise performance, as a smaller g_{m2} can be used to achieve input matching. The LNTA also maintains high linearity as the nonlinear voltage-to-current (V–I) conversion of g_{m3} is predistorted by the identical V–I profile of g_{m2} in feedback. Drain-side nonlinearity can be predistorted as well by designing the load presented by the current-driven passive mixer so that the voltage swings at the drain nodes of g_{m2} and g_{m3} are also the same.

The voltage amplifier needs to provide a noninverting voltage gain, which was achieved by cross-coupling the output nodes. Since this voltage gain is noninverting only in differential mode, there can be stability concerns in common mode. The current sources in g_{m2} provide common-mode rejection to help ensure stability. Such current sources also appear in g_{m3} to ensure that its V–I conversion profile is identical to that of g_{m2}. Furthermore, $M_{5,6}$ in g_{m1} lower the common-mode impedance at its output node to ensure stability at RF frequencies.

A. Quantitative Analysis of the Improved G_m–BW Tradeoff

In order to analyze the S_{11} BW, one can model the input, feedback, and output g_m cells with ideal g_m cells along with their input and output capacitive loads $C_{\mathrm{in}1,2,3}$ and $C_{\mathrm{out}1,2,3}$ and their output resistances $r_{o1,2,3}$. r_{o2} is larger than the input impedance synthesized by the g_{m1}–g_{m2} feedback loop by a factor equal to the intrinsic gain times the g_m-boosting voltage gain and, therefore, can be neglected. The single-ended input impedance is

$$Z_{\mathrm{in}}(\omega) = \frac{j\omega/C_{\mathrm{in}} + \omega_{\mathrm{int}}/C_{\mathrm{in}}}{(j\omega)^2 + j\omega\cdot\omega_{\mathrm{int}} + \omega_A^2} \tag{1}$$

where $C_{\mathrm{in}} = C_{\mathrm{in}1} + C_{\mathrm{out}2} + C_{\mathrm{pad}}$ and $C_{\mathrm{int}} = C_{\mathrm{out}1} + C_{\mathrm{in}2} + C_{\mathrm{in}3}$ are the total capacitance at the input node and the intermediary node, respectively; $\omega_{\mathrm{int}} = 1/R_{\mathrm{eff}}C_{\mathrm{int}}$; $R_{\mathrm{eff}} = R_{\mathrm{int}}//r_{o1}$; and $\omega_A = \sqrt{g_{m1}g_{m2}/C_{\mathrm{int}}C_{\mathrm{in}}}$. Note that the dc input matching condition $(Z_{\mathrm{in}}(\omega=0) = 1/g_{m1}g_{m2}R_{\mathrm{eff}} = R_S)$ has been assumed. The proposed LNTA utilizes active feedback to synthesize a second-order input impedance with a zero that mitigates the degrading impact the input capacitance has over the S_{11} BW. This is similar to an inductor synthesized by a gyrator operating on a load capacitance (C_{int}).

By setting $S_{11}(Z_{\mathrm{in}}) = -10$ dB, the expression for the S_{11} BW is $\omega_{S_{11}}(\alpha) = \omega_A(1/2((\alpha^2+(1/\alpha)^2-14/9)^{1/2}+16/9)^{1/2} - 1/2(\alpha^2+(1/\alpha)^2-14/9))^{1/2}$, where $\alpha = \omega_{\mathrm{int}}/\omega_A$. One finds

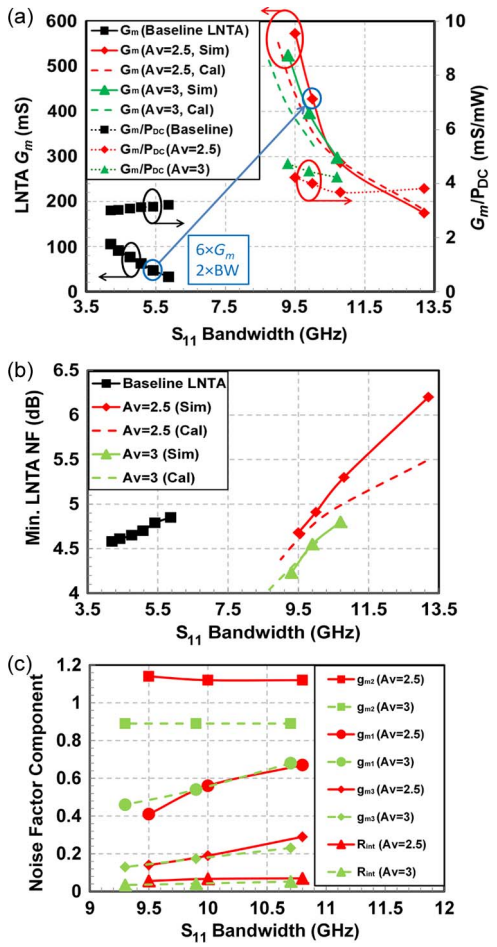

Fig. 3. (a) Simulated G_m–BW tradeoff for the baseline (partial noise canceling) and proposed LNTAs. (b) Simulated NF–BW tradeoff for the baseline (partial noise canceling) and proposed LNTAs. (c) Noise factor components of the proposed LNTA for different A_V values.

that $\omega_{S_{11}}$ is maximized at $\alpha = 1$. The maximum $\omega_{S_{11}}$ is

$$(\omega_{S_{11}})_{\mathrm{MAX}} = \omega_{\mathrm{int}} \cdot \frac{1}{3}\sqrt{3\sqrt{\frac{11}{2}} - 2} \approx 0.748\omega_{\mathrm{int}}. \quad (2)$$

Substituting the input matching equation and the definitions of ω_{int} and into $\alpha = 1$ yields

$$(C_{\mathrm{pad}} + C_{\mathrm{in1}} + C_{\mathrm{out2}})R_S = (C_{\mathrm{out1}} + C_{\mathrm{in2}} + C_{\mathrm{in3}})R_{\mathrm{eff}}. \quad (3)$$

The LNTA transconductance gain at low frequencies is given by $G_m = g_{m1}R_{\mathrm{eff}}g_{m3}$. There are four design variables: g_{m1}, R_{int}, g_{m2}, and g_{m3}. Once g_{m1} and R_{int} are chosen, is determined by the input matching condition, and g_{m3} is determined by (3) since the input and output capacitance of a transconductance cell are proportional to its g_m. In Fig. 3(a), the G_m–BW tradeoff of this LNTA is simulated. For each curve, $g_{m1}R_{\mathrm{eff}} = A_V$ (the g_m-boosting voltage gain) is kept constant, and g_{m1} is varied. These simulations are based on process design kit models, including device layout parasitics. For $A_V = 2.5$, the proposed LNTA achieves more than two times S_{11} BW, compared with the partial noise-canceling design, and more than six times G_m. For the same comparison points, the transconductance power efficiency (G_m/P_{DC}) improves from 3.1 to 4 mS/mW. Theoretical values show good agreement with simulations.

Although G_m flatness is not required for wideband cognitive/software-defined radio where signal BW is much lower than the range of operating frequencies, it is important to maintain high G_m to alleviate the noise requirements of the circuits downstream. Simulations show that the G_m −3-dB BW is consistently higher than the S_{11} BW, leaving the latter as the operation BW limiting factor.

B. Quantitative Analysis of the NF–BW Tradeoff

Assuming that input matching is ensured, the NF is given by

$$F = 1 + \frac{\gamma}{A_V} + \frac{\gamma}{g_{m1}R_S} + \frac{4\gamma/g_{m3} + R_{\mathrm{eff}}^2/R_{\mathrm{int}}}{R_S A_V^2}. \quad (4)$$

The second and third terms represent the noise contributions of the feedback g_m cell g_{m2} and the input g_m cell g_{m1}, respectively. The last term is the noise contribution of the output g_m cell g_{m3} and R_{int} and can be neglected due to A_V^2 in the denominator. The noise factor expression shows that low-noise operation favors larger A_V and g_{m1}. Since the LNTA input node capacitive loading increases with g_{m1}, an NF–BW tradeoff exists and is simulated in Fig. 3(b). Simulations indicate that the proposed LNTA shows comparable NF with the partial noise-canceling design while achieving two times S_{11} BW and six times G_m. The simulations also match the calculations based on (4). Simulation results [see Fig. 3(c)] also confirm the noise factor contributions of the various components within the LNTA. As predicted, the noise contribution of the feedback g_m cell is only dependent on A_V. The contribution of the input g_m cell g_{m1} is only dependent on the g_{m1} value itself, which, in turn, varies inversely with the S_{11} BW. The noise contributions of the output g_m cell g_{m3} and R_{int} are small as expected.

C. Linearity Performance

The CS stage in the baseline partial noise-canceling LNTA achieved a simulated IIP3 of +15 dBm, and the complete LNTA with 100-mS G_m, loaded with a resistor of 10 Ω modeling the input impedance of a passive mixer downconverter, showed a simulated IIP3 of +12.5 dBm.

In the proposed LNTA, both g_{m2} and g_{m3} cells are biased with the same overdrive voltage of 250 mV as in the partial noise-canceling LNTA and, thus, are able to achieve the same +15-dBm IIP3. However, due to the current sources and the common-mode feedback (CMFB) circuitry, supply voltages are raised from 1.2 to 1.6 V for g_{m2} and g_{m3} for this study (but kept at 1.2 V in measurement to match the rest of chip).

The input match predistortion linearizes the current amplification, but when driven with a finite R_S, the linearity of the proposed LNTA is limited by the nonlinear current division between R_S and the LNTA input impedance. g_{m1} is chosen to be 80 mS for the simulation in Fig. 4, whereas g_{m2} and g_{m3} are chosen to fulfill low-frequency input matching and maximum S_{11} BW conditions. R_{int} is varied to get different A_V values. When the input and output of the g_{m2} cell are connected $(A_V = 1)$, the IIP3 of the input current is +18.5 dBm.

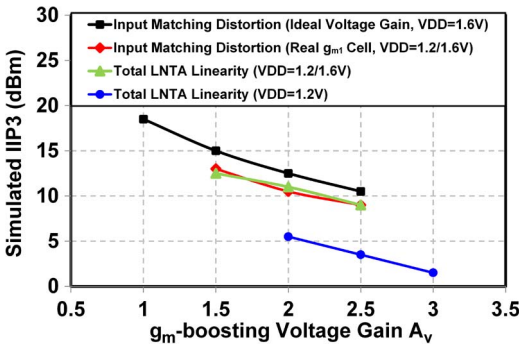

Fig. 4. Simulated IIP3 performance of the proposed LNTA.

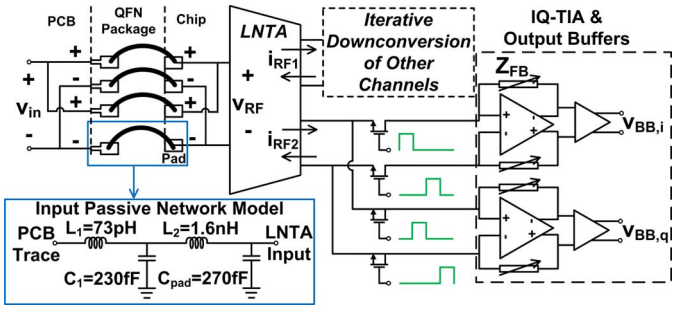

Fig. 5. Direct-conversion path in a 65-nm CMOS 0.6- to 9-GHz iterative downconversion channelizing receiver [5] along with QFN package parasitics. The estimated wirebond inductance on each input is 1.6 nH, including coupling.

If a perfectly linear voltage gain is inserted to boost g_m, linearity degrades because a larger voltage swing appears at the gate node of the g_{m2} cell. In fact, we found in the simulation that the input current IIP3 proportionally degrades with the larger gate voltage swing: twice the A_V corresponds to 6 dB lower IIP3. Moreover, if the device transconductance is boosted by the real voltage amplifier, the input current IIP3 further degrades by 1.5–2 dB (see Fig. 4). The overall LNTA's output current IIP3 is virtually identical to the input current IIP3, demonstrating the linearity of the current mirroring. Even with a gain-boosting voltage of 2, the overall LNTA exhibits comparable linearity (+11-dBm IIP3) to the simulated partial noise-canceling design. The LNTA IIP3 degrades by 6 dB when the supply voltage (VDD) of the LNTA is kept at 1.2 V because the voltage headroom of the feedback g_m cell g_{m2} is reduced.

III. Sixty-Five-Nanometer CMOS 0.6- to 10.5-GHz 242-mS LNTA

The proposed LNTA was implemented in 65-nm CMOS within a 0.6- to 9-GHz iterative downconversion channelizing receiver [5] that has multiple concurrent downconversion paths with a single local oscillator (LO) input (see Fig. 5). The LNTA provides two current outputs by splitting the output g_m cell into two branches. One of the branches drives a direct downconversion path that can be used to evaluate the LNTA up to 4.2 GHz (limited by LO divider functionality) by varying its LO. This path uses a four-phase 25% duty cycle passive mixer and a TIA with a 1-GHz BW (see Fig. 6). In such receivers, a multioutput high-G_m LNTA with isolation between outputs

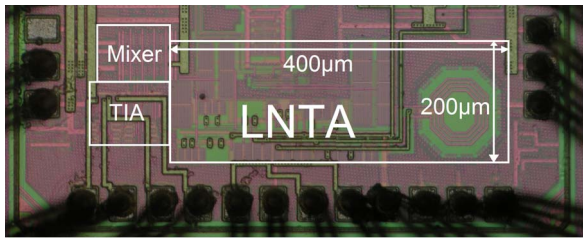

Fig. 6. Die photo of the channelizing receiver showing the proposed LNTA and the direct-conversion path.

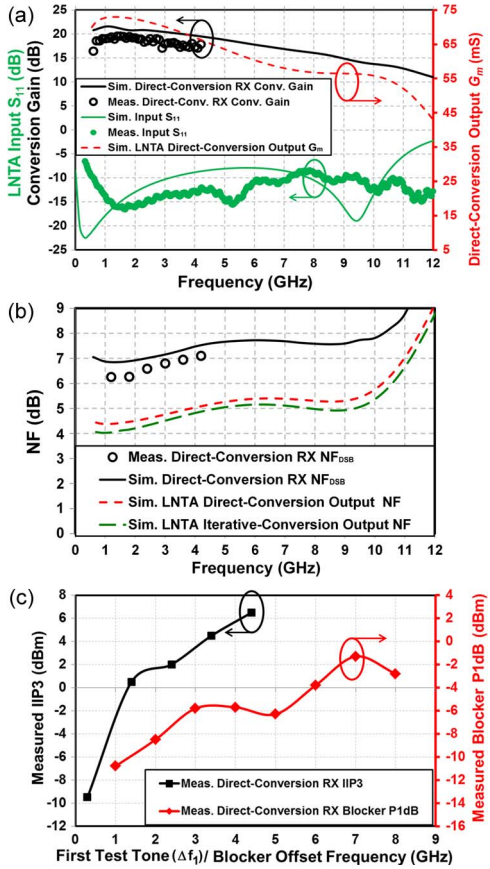

Fig. 7. (a) LNTA S_{11}, direct-conversion output G_m and direct-conversion receiver conversion gain. (b) LNTA (both outputs) and direct-conversion receiver NF. (c) Measured direct-conversion receiver IIP3 and blocker 1-dB compression points with test tones/blockers located at different frequency offsets (LO is $f_{\rm LO} = 1$ GHz, desired signal is $f_{\rm in} = 1.5$ GHz, and, for IIP3, $\Delta f_2 = 2 \times \Delta f_1 + f_{\rm LO} - f_{\rm in}$.).

is the only practical way to split the signal as currents among multiple concurrent paths.

The LNTA design point has an $A_V = 2.5$ (chosen based on the NF–linearity tradeoff) and a theoretical total G_m of 286 mS. Theoretical minimum NF and BW are 5.3 dB and 10.8 GHz [see Fig. 3(a) and (b)]. Low-threshold-voltage devices with customized device layouts were utilized to achieve better noise performance and higher f_T. In addition, a peaking inductance of 2.2 nH was inserted in series with $R_{\rm int}$ to increase the BW. The chip was packaged in a commercial 48-pin QFN package. Wirebond inductance in series with the LNTA input degrades input matching. Each of the LNTA's differential inputs was connected to two package pins through two wirebonds in

TABLE I
PERFORMANCE COMPARISON WITH INSTANTANEOUSLY WIDEBAND CMOS RECEIVERS AND LNAS

	LNTA Topology	LNTA G_m (mS)	*S11* BW (GHz)	Operating BW (GHz)	NF_{min} (dB)	Harmonic Rejection	Wideband IIP3 (dBm)	B1dB (dBm)	LNTA IDC(mA) @VDD(V)	CMOS Process	Meas. Setup
[1] (RX)	Partial Noise-canceling	100^{sim}	0.08-5.5	0.4-0.9$^{\#}$	3.5	Yes	+16	+2	14@1.2	65nm	Packaged
[3] (RX)	50Ω-terminated CS Stage + Baseband Distortion Cancellation	90.7^{sim}	1-2.7	1-2.5	7.25	No	+12	-3	NR@1.2	65nm LP	NR
[4] (RX)	Complete Noise-canceling	100^{sim}	0.3-1.7	0.3-1.7	4.2	No	+12	+2	5.5@2.5 6@1.2	65nm	Packaged
[7] (LNA)	Noise-canceling Distributed LNA	NA (A_V=12dB)	DC-9.5	DC-9.5	2.8 (LNA)	NA	+4$^{\Delta}$	-7$^{\Delta}$	12.8@1.4	65nm	RF Probing
[8] (RX)	Noise-canceling LNA + g_m cell	NR (A_V=18-20dB)	0.8-6	0.8-6	5	Yes	-3.5	-13.5	9.6@2.5	90nm	NR
This Work (RX)	**g_m-boosted Current Mirroring**	**242^{sim} ***	**0.6->12**	**0.6-4.2$^{\#}$ 0.6-10.5^{sim} ****	**6.2 4.5^{sim} ****	**No**	**+6.5**	**-1.5**	**60@1.2**	**65nm**	**Packaged**

^{sim} – Simulated. $^{\#}$ – Limited by LO path. NA – Not applicable. NR – Not reported. $^{\Delta}$ – Will degrade if followed by a g_m cell or mixer.
* – Split between different paths. ** – At the direct conversion output of the LNTA.

parallel, resulting in a lower effective inductance. The four signal wirebonds were alternatively arranged in an $S+$, $S-$, $S+$, $S-$ configuration, further reducing the effective inductance through coupling (see Fig. 5).

In postlayout simulations, the LNTA provides a G_m of 170 and 72 mS at the iterative downconversion and direct-conversion outputs, respectively. The S_{11} BW is 10.5 GHz, and the 3-dB BW of G_m in the direct-conversion path is 11.3 GHz [see Fig. 7(a)]. The two LNTA outputs have different minimum NFs of 4 and 4.8 dB since the noise contributions of the output g_m cells slightly increase after the splitting [see Fig. 7(b)]. The direct-conversion receiver has a minimum NF of 6.8 dB due to harmonic noise folding and baseband TIA noise. The supply voltage of the input and output g_m cells was kept at 1.2 V to match that of the rest of the chip. As discussed earlier, this lowers the LNTA wideband IIP3 to +6 dBm (test tones at 2 and 2.5 GHz). Simulated blocker 1-dB compression point (B1dB) was +1.5 dBm. The input, feedback, and output g_m cells consume 33, 0.8, and 28 mA, respectively.

In measurement, S_{11} is lower than -8 dB up to beyond 12 GHz. The direct-conversion receiver's conversion gain [see Fig. 7(a)] matches the postlayout simulations closely within 2 dB up to 4.2 GHz, which can be attributed to the tolerance of the TIA feedback resistance. Postlayout simulations extend beyond 4.2 GHz through the use of ideal LO drive. This fixed-IF swept-LO conversion gain has lower BW than that of the LNTA G_m since the input impedance of the passive mixer is high, due to high input impedance of the wideband (1 GHz) TIA (90 Ω under nominal settings) caused by limited wideband TIA amplifier gain. A direct-conversion receiver with a more selective TIA would be able to better leverage the LNTA's G_m BW. Measured direct-conversion receiver NF ranges from 6.2 to 7 dB and matches simulation [see Fig. 7(b)]. Measured IIP3 and blocker P1dB [see Fig. 7(c)] reach +6.5 and −1.5 dBm, respectively, for test tones at out-of-band frequencies, consistent with LNTA simulations. Due to the wide TIA BW and harmonic mixing, large test tone offsets are required for the receiver out-of-band linearity to be limited by the LNTA.

The proposed LNTA is compared with similar state-of-the-art instantaneously wideband CMOS receivers and LNAs in Table I. The BW achieved in this LNTA is the highest among all. This LNTA achieves much higher G_m with competitive blocker P1dB and noise performance (particularly considering the lack of harmonic rejection in the direct-conversion receiver path, resulting in noise folding) compared with single-stage LNTAs. The out-of-band IIP3 achieved is somewhat degraded when compared with single-stage LNTAs but is significantly higher than works employing voltage-mode LNAs.

IV. CONCLUSION

An LNTA based on a g_m-boosted current mirroring topology that alleviates the G_m–NF–BW tradeoff in conventional LNTAs has been presented. Linearity is maintained despite the use of voltage gain for g_m boosting through the inherent predistortion. The provided theoretical analyses and design guidelines are validated by measurements from a 65-nm CMOS 0.6- to 9-GHz channelizing iterative downconversion receiver.

REFERENCES

[1] Z. Ru, N. Moseley, E. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3359–3375, Dec. 2009.
[2] D. Murphy *et al.*, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, Dec. 2012.
[3] S. Youssef, R. van der Zee, and B. Nauta, "Active feedback technique for RF channel selection in front-end receivers," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3130–3144, Dec. 2012.
[4] J. Zhou, P. Kinget, and H. Krishnaswamy, "A blocker-resilient wideband receiver with low-noise active two-point cancellation of 0dBm TX leakage and TX noise in RX band for FDD/Co-existence," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 352–353.
[5] H. Krishnaswamy *et al.*, "RF channelizer architectures using iterative downconversion for concurrent or fast-switching spectrum analysis," in *Proc. IEEE Int. MWSCAS*, Aug. 2014, pp. 977–980.
[6] F. Bruccoleri, E. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.
[7] J. Zhu, H. Krishnaswamy, and P. Kinget, "A DC-9.5GHz noise-canceling distributed LNA in 65nm CMOS," in *Proc. IEEE RFIC Symp.*, Jun. 2013, pp. 177–180.
[8] R. Bagheri *et al.*, "An 800-MHz-6-GHz software-defined wireless receiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2860–2876, Dec. 2006.
[9] E. Keehr and A. Hajimiri, "A wide-swing low-noise transconductance amplifier and the enabling of large-signal handling direct-conversion receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 30–43, Jan. 2012.