Large-Scale Power Combining and Mixed-Signal Linearizing Architectures for Watt-Class mmWave CMOS Power Amplifiers

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***Abstract*—Millimeter wave (mmWave) CMOS power amplifiers (PAs) have traditionally been limited in output power due to the low breakdown voltage of scaled CMOS technologies and poor quality of on-chip passives. Moreover, high data-rates and efficient spectrum utilization demand highly linear PAs with high efficiency under back-off. A novel linearizing architecture which simultaneously employs large-scale power combining, linearization through dynamic load modulation, and improved efficiency under back-off by supply-switching and load modulation is introduced. A quarter-wave combiner that exploits lumped spiral inductor equivalents of quarter-wave transmission lines with higher characteristic impedance enables one-step, low-loss, eight-way combining with a measured efficiency of 75% at 45 GHz. Eight-way combining of stacked SOI CMOS PAs results in a PA array with watt-class (>27 dBm) saturated output power (3× higher than prior art) and ultra-wideband operation (33–46 GHz) in 45 nm SOI CMOS. Another 45 nm SOI CMOS prototype, a three-bit digital to mmWave PA array, utilizing the proposed linearizing architecture achieves 23.3 dBm of saturated output power at 42.5 GHz, PAE_{-6dB}/PAE_{peak} = 67.7% as well as excellent linearity (DNL < 0.5 LSB} and INL < 1 LSB using end-point fit).**

***Index Terms*—45 GHz, device stacking, digital-mmWave data conversion, linearization techniques, millimeter-wave integrated circuits, power amplifier, power combiner, SOI CMOS process.**

I. Introduction

In THE LAST decade, advancements in technology scaling have enabled CMOS integrated circuits to operate at mmWave frequencies. A major drawback of migrating to deeply scaled technologies is the limited breakdown voltage as well as poor quality of on-chip passives, which form the bottleneck in efficient power generation at mmWave. These, in conjunction with the high path loss at these frequencies, have typically limited the deployment of mmWave transceivers to short-range links. However, burgeoning long-range applications such as satellite communication in the 45 GHz band and high data-rate wireless backhaul in the 71–76 GHz and 81–86 GHz bands have innervated research efforts for the development of high-power, energy-efficient PAs. Recent works involving series stacking of multiple devices [1]–[3] in PAs have demonstrated moderate output powers (around 17–20 dBm) with high efficiency (20–35%) in fine-line CMOS at mmWave frequencies [4]–[10], but watt-level output power is yet to be achieved at these frequencies.

A second major challenge arises from the trade-off between efficiency and linearity. Quasi-linear PA classes (like class-A, class-AB, class-B) are typically less efficient than their nonlinear counterparts (like class-E, class-D^{-1}, etc.). To efficiently utilize the spectrum and achieve high data-rates, PAs are operated in highly backed-off regions to handle high-order modulations in a linear manner. This causes the average transmitter efficiency to plummet since the quintessential PA is most efficient near P_{sat} and exhibits poor efficiency under back-off. PAs employing architectures such as outphasing [11] and Doherty [8] have been proposed as efficiency enhancement solutions. However, the load modulation effect in outphasing is quite weak and does not provide significant benefits in efficiency under back-off. The Doherty architecture offers considerable improvement in efficiency under back-off but requires extensive linearization.

This paper details a linearizing PA architecture at mmWave frequencies, first introduced in [12], that *simultaneously enables high saturated output power* (P_{sat}) *through large-scale power combining, linearity through dynamic load modulation, and high efficiency under back-off through supply-switching and load modulation*. A lumped quarter-wave combiner that enables eight-way power combining with a high 75% measured efficiency at 45 GHz is proposed. The use of this combiner in conjunction with stacked Q-band class-E-like SOI CMOS PAs [5], [9] results in watt-class operation ($P_{sat} > 0.5$ W) from a 45 nm SOI CMOS PA array with a 1 dB bandwidth spanning 33–46 GHz owing to combiner-PA co-design [12]. A 42.5 GHz three-bit digital to mmWave PA array employing the linearizing architecture achieves $PAE_{-6\mathrm{dB}}/PAE_{\mathrm{peak}} = 67.7\%$, a highly-linear digital control word (DCW) to output amplitude profile and low AM-PM distortion [12]. The fundamental concept of the linearizing architecture, the lumped quarter-wave combiner and measurement results of the aforementioned prototypes were first introduced in [12]. This paper deals with the factors affecting various design choices in implementing watt-class PAs using this architecture such as the choice of device size, number of PA unit-cells combined and impedance transformation ratio of the combiner using theoretical analysis

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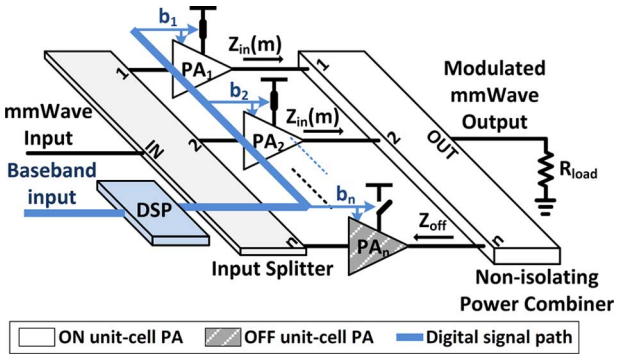


Fig. 1. Digitally-controlled load modulated power-DAC architecture.

corroborated by simulations and measurement results. This paper also expands on design considerations for implementing highly linear direct digital-to-mmWave DACs using this architecture. Effects of PA unit-cell deviation from ideal behavior and requirements on the combiner to achieve the desired load-modulation effect as well as the linearity vs. efficiency under backoff tradeoffs are thoroughly discussed and corroborated with theoretical analyses, simulations and measurements.

This paper is organized as follows. Section II describes the proposed architecture that enables large-scale power combining and linearization with high efficiency under back-off. In Section III, the challenges associated with on-chip large-scale mmWave power combining are delineated. A non-isolating combiner architecture with the desired load modulation ability is presented along with design guidelines. The effect of non-idealities in the sub-blocks on the linearity and efficiency under back-off of the proposed architecture are discussed in Section IV with design guidelines on how to mitigate them. The implementation details of two PA prototypes in a 45 nm SOI CMOS process based on the proposed combiner and linearizing architecture are discussed in Section V. Section VI reports the measurement results of the two PA prototypes and compares them with state-of-the-art mmWave power amplifiers. Section VII concludes with a summary of the accomplishments of this work.

II. Linearized Power-DAC Using Supply-Switching and Digitally-Controlled Load Modulation

A digitally controlled, supply-switched and load modulated switching PA architecture shown in Fig. 1 is proposed to enable *high output power*, *low efficiency-degradation under back-off* and *high linearity*. The architecture employs several (n) switching-class mmWave PA unit-cells which can be individually turned ON or OFF by means of a digital control bit. These are combined using a non-isolating power combiner to make an overall linear mmWave DAC with high back-off efficiency through the load modulation of the combiner and the elimination of DC power consumption in OFF PAs. Salient features of this architecture are outlined below.

A. Stacked Switching-Class Power Amplifier Unit-Cells

Switching power amplifier classes such as D and E [13]–[15] are extensively utilized at RF frequencies since they facilitate (ideally) lossless operation by eliminating the co-existence of high voltage across and high current through the device. Recently, switching PAs have been demonstrated at mmWave frequencies as well using scaled CMOS technologies [16]. Series stacking of multiple devices in PAs [1] is a promising technique that enables the use of higher supply voltages by distributing the overall voltage stress equally amongst the various stacked devices [2], [3]. The concept of device stacking has been recently demonstrated in the mmWave regime for quasi-linear PAs [6], [7] as well as switching-class PAs [4], [5], [9], [10], [17] to implement moderate-power, high-efficiency stacked PAs in CMOS. The stacked Class-E-like PAs described in [5] and [9] generate 17–20 dBm of output power at 20%–35% PAE, a significant improvement over prior state-of-the-art mmWave PAs (with and without power-combining) [16], [18]–[24]. This indicates that on-chip power combining of eight to sixteen of these PAs can enable watt-class output power in CMOS at mmWave for the first time. Our proposed architecture utilizes these Class-E-like stacked PAs as unit-cells in the array.

B. Load Modulation for Linearity and High Back-Off Efficiency

Linearity of output amplitude $(A_{\rm out})$ with the number of PAs turned ON (m) can be achieved in any power-combined system that satisfies conditions (11) and (15) detailed in the Appendix. However, it is not particularly beneficial to use an isolating combiner due to its poor efficiency under back-off characteristics. Consider the case of a PA array which contains n supply-switchable PAs that are combined using an isolating combiner and satisfies the conditions for linear $A_{\rm out}$ vs. m as discussed in the Appendix. The total output power of such a system is

$$P_{\rm out}(m) = m \times P_{\rm unit} \times \eta_{\rm comb}(m) \tag{1}$$

where $\eta_{\rm comb}(m)$ is the efficiency of the combiner as a function of m and $P_{\rm unit}$ is the output power of each ON unit-cell which remains constant with m due to the isolating nature of the combiner. Since the output amplitude of the PA array is linear with $m(\sqrt{P_{\rm out}(m)} \propto m)$ the efficiency of the combiner may be written as

$$\eta_{\rm comb}(m) \propto \frac{m^2}{m \times P_{\rm unit}} \propto \frac{\sqrt{P_{\rm out}(m)}}{P_{\rm unit}},. \tag{2}$$

The PA array's drain efficiency is

$$\begin{aligned}\eta_{array}(m) &= \eta_{\rm unit} \times \eta_{\rm comb}(m) \\ &\propto \eta_{\rm unit} \frac{\sqrt{P_{\rm out}(m)}}{P_{\rm unit}} \quad \text{(Class-B)}\end{aligned} \tag{3}$$

where $\eta_{\rm unit}$ is the drain efficiency of an ON PA unit-cell and remains constant across m due to the unchanging load impedance that it is presented with. *Hence, any isolating combiner, such as the n-way Wilkinson or the cascaded Wilkinson tree, that satisfies the conditions for linear $A_{\rm out}$ vs. m of the PA array is limited to a class-B like efficiency degradation under back-off.* The isolating combiner dissipates the excess power that the ON PA unit-cells generate (in the isolation resistors in the case of the Wilkinson) in order to maintain linear $A_{\rm out}$ vs. m.

On the other hand, a non-isolating combiner with certain characteristics can alter the output power of each ON PA

unit-cell through load modulation such that the excess power dissipated by the combiner to maintain linearity is lowered or even eliminated. This can result in an efficiency under back-off that is better than class-B. Note that the changing efficiency of the unit-cells with changing load impedance must be considered—this is discussed in Section IV. While the outphasing transmitter in [11] also leverages load modulation, the overall back-off characteristics are still worse than class-B due to the weak nature of the load modulation.

Switching-class PA unit-cells typically exhibit an inverse proportional relationship between output power and load resistance. Quasi-linear-class PAs driven into hard-saturation/voltage-limited regime can also exhibit the same property. This may be expressed as $P_{\rm unit}(m) \propto 1/R_{\rm in}(m)$ where $R_{\rm in}(m)$ is input resistance (assuming that the combiner presents a purely resistive impedance to the PA unit-cells) presented by the non-isolating power combiner to the ON PA unit-cells in Fig. 1. In other words, the effective source resistance of a switching PA is very small. The total output power of the PA array, assuming the combiner stays lossless with m ($\eta_{\rm comb}(m) = 1$ for all m), is given by $P_{\rm out}(m) = mP_{\rm unit}(m)$, and must be proportional to m^2 to achieve $A_{\rm out} \propto m$.

$$mP_{\rm unit}(m) \propto m^2 \Rightarrow \frac{m}{R_{\rm in}(m)} \propto m^2 \Rightarrow R_{\rm in}(m) \propto \frac{1}{m}. \quad (4)$$

Hence, the kind of load modulation that the non-isolating combiner must provide is an inverse variation with m of the real part and no imaginary part. Section III contains detailed discussions on how to build a compact and highly efficient non-isolating combiner with this kind of load modulation.

Here, and through the rest of the paper, we focus on AM-AM nonlinearity as AM-PM nonlinearity can be pre-distorted for in a digital polar architecture for instance with no significant impact on efficiency under backoff. Furthermore, particularly at mmWave frequencies, high resolution phase modulators are more readily implemented than high-amplitude-resolution power DACs. Finally, it is seen that as long as the imaginary part of the impedance presented to ON PAs by the combiner is small across m (simulations are presented in the Appendix), AM-PM distortion is small (results are shown in Section VI).

C. Supply-Switching for High Back-Off Efficiency

The PA unit-cells are equipped with supply switches to eliminate DC current consumption when they are turned off. This way, the DC power consumption of the array also backs off with the output power of the PA leading to an improved efficiency under back-off profile. Detailed discussions on the implementation of such unit-cells in the context of stacked CMOS switching-class mmWave PAs can be found in [25] and are summarized in Section V-B.

D. Input Splitter

In order to maintain input match with the constant envelope mmWave input source, the input impedance of the PA array must not vary with m. In this work, the burden of maintaining input match is borne by the OFF unit-cells (by switching in termination resistors, see Section V-B and [25]) and the power splitter is designed as a zero-degree splitter [26]–[28] to minimize area consumption within the layout constraints imposed by the PA array.

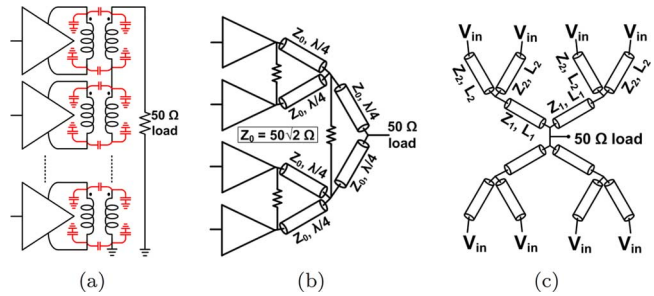


Fig. 2. Conventional power combining techniques: (a) transformer-based series combining, (b) Wilkinson combining, and (c) zero-degree combining.

III. Large-Scale Millimeter-Wave Power Combining

A. Limitations With Conventional Power Combiners

Large-scale, low-loss power combining on silicon is fraught with several challenges. Transformer-based series power combining [29] (Fig. 2(a)) is limited by the asymmetry that results from parasitic winding and inter-winding capacitances, causing non-constructive addition of individual PA voltages and stability challenges [24]. With Wilkinson power combiners, the maximum number of PA units n that can be combined in a single Wilkinson is restricted to two to four by the highest transmission-line characteristic impedance Z_0 that can be achieved in the back end of the line (BEOL), as the required $Z_0 = 50\sqrt{n}\ \Omega$. Realizing an on-chip transmission line with $Z_0 = 141.42\ \Omega$ for an eight-way Wilkinson combiner is impossible in a low-loss manner in scaled CMOS BEOLs while meeting electromigration constraints for watt-class power levels. Cascading 2:1 Wilkinsons (Fig. 2(b)) results in a severe increase in combiner loss. The zero-degree combiner [26]–[28] shown in Fig. 2(c) is essentially a current combining approach where the connecting lines are designed to perform the necessary impedance transformation. This has the advantage of not being restricted to the use of quarter-wavelength transmission lines of a fixed characteristic impedance. However, it is a multi-step structure and its efficiency is a function of the impedance transformation performed by each stage in the cascade.

B. Proposed Non-Isolating Lumped Quarter-Wave Combiner

In this work, a quarter-wave combiner (shown in Fig. 3) is pursued, which is essentially an n-way Wilkinson combiner without the isolation resistors. The isolation resistors are eliminated due to the load modulation requirement described earlier. To address the high Z_0 requirement and enable large scale power combining on-chip in one step, we replace the quarter-wave transmission lines of an n-way Wilkinson with lumped *C-L-C* π-section equivalents at the desired frequency of operation, since any reciprocal passive two-port network has an equivalent π-network at a given frequency. Each *C-L-C* π-section is realized as a single spiral inductor. To achieve the desired equivalent characteristic impedance Z_0 and behavior of a quarter-wave transmission line at the desired frequency ω_0, the

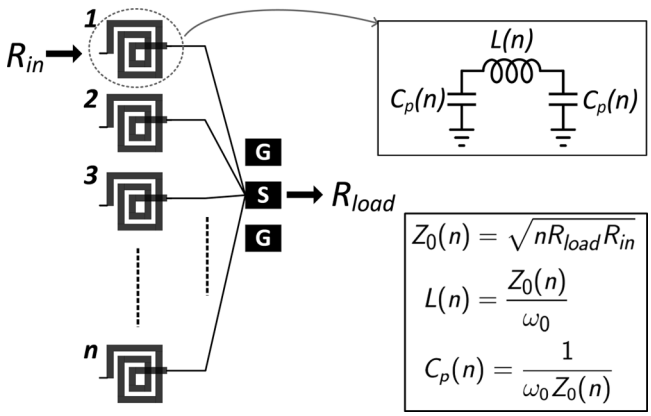


Fig. 3. An n-way spiral-based lumped quarter-wave combiner with design equations.

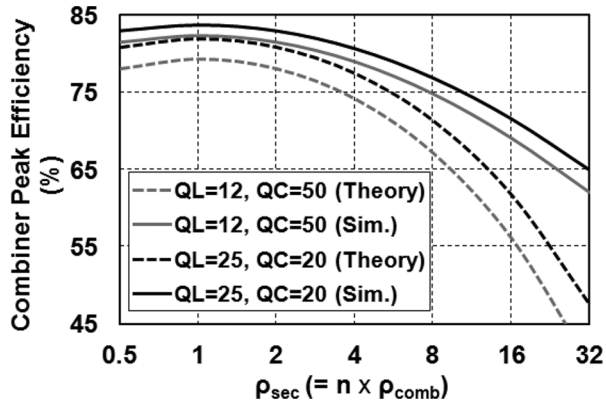


Fig. 4. Theoretical (from (5)) and simulated peak combiner efficiencies as a function of ideal impedance transformation ratio ρ_{sec} of each spiral section for two pairs of Q_L, Q_C of the spiral in an eight-way combiner at 45 GHz with $R_{\rm load} = 50\ \Omega$.

spiral must achieve an inductance of $L = Z_0/\omega_0$ and a parasitic capacitance of $C_p = 1/(Z_0\omega_0)$ on either side as seen in Fig. 3. In other words, the parasitic capacitances of each spiral are absorbed in the design as key components of the *C-L-C* π-sections. If $R_{\rm load}$ is the load impedance seen by the combiner and $R_{\rm in}$ is the desired input impedance then $L = \sqrt{nR_{\rm load}R_{\rm in}}/\omega_0$ and $C_p = 1/\omega_0\sqrt{nR_{\rm load}R_{\rm in}}$. For instance, an eight-way combiner designed at 45 GHz to drive a 50 Ω load and present a 50 Ω input impedance at each of its inputs requires $L = 500$ pH with $C_p = 25$ fF on either side giving an effective Z_0 of 141.42 Ω. A 500 pH spiral inductor with 25 fF (or less) parasitic capacitance on each side is easily achievable in the 45 nm SOI CMOS BEOL whereas a transmission line with the same Z_0 is very hard to realize in a low-loss manner as mentioned earlier. The key insight is that spirals are able to achieve higher equivalent characteristic impedances than transmission lines primarily due to their magnetic self-coupling. This self-coupling, absent in transmission lines, enables a greater inductance for a given parasitic capacitance budget. Loss is also reduced as spirals are able to use wider line widths than narrow high-Z_0 transmission lines to achieve the same characteristic impedance.

The maximum number of elements that can be combined in a single step using the quarter-wave lumped combiner for a given $R_{\rm load}$ and $R_{\rm in}$ is limited by the achievable self-resonant frequency (SRF) of spirals in the BEOL (16 in the case of the 45 nm SOI CMOS BEOL for $R_{\rm load} = R_{\rm in} = 50\ \Omega$ for which $Z_0 = 200\ \Omega$ at 45 GHz) and layout considerations for maintaining symmetry. In the watt-class PA array prototype, eight elements are combined for which the spirals have a $Z_0 = 141.42\ \Omega$ at 45 GHz. However, with better floor-planning techniques as many as 12 elements may be combined which requires a $Z_0 = 173.2\ \Omega$ at 45 GHz. While a lumped Wilkinson power divider has already been demonstrated in [30], the high equivalent characteristic impedance of spirals was not exploited to combine more than four elements.

The efficiency $\eta_{\rm comb}$ of the n-way lumped quarter-wave combiner driving $R_{\rm load}$ may be expressed as the following:

$$\eta_{\rm comb} \approx 1 - \left(\frac{1}{Q_L} + \frac{1}{Q_C}\right)\left(\sqrt{n\rho_{\rm comb}} + \frac{1}{\sqrt{n\rho_{\rm comb}}}\right) \quad (5)$$

where $\rho_{\rm comb}$, the ideal impedance transformation performed by the combiner, may be expressed as

$$\rho_{\rm comb} = \frac{R_{\rm load}}{R_{\rm in}} = n\left(\frac{R_{\rm load}}{Z_0}\right)^2. \quad (6)$$

Q_L is the inductive quality factor of the spiral and Q_C is the quality factor of its parasitic capacitances at ω_0. Equation (5) can also be written as the following:

$$\eta_{\rm comb} \approx 1 - \left(\frac{1}{Q_L} + \frac{1}{Q_C}\right)\left(\sqrt{\rho_{sec}} + \frac{1}{\sqrt{\rho_{sec}}}\right) \quad (7)$$

where $\rho_{sec} = n\rho_{\rm comb}$ and is the impedance transformation performed by each spiral π section in the combiner. Equations (5) and (7) are the result of perturbative analysis and assume that the currents and voltages in the ideal lossless combiner are unaffected by the presence of the resistance in series with the inductance and in parallel with the capacitances to model the loss of the spiral. It is seen that the efficiency of the combiner only depends on Q_L, Q_C and ρ_{sec}. The simulated and theoretical efficiencies of two eight-way combiners with $Q_L = 12, Q_C = 50$ and $Q_L = 25, Q_C = 20$ at 45 GHz are shown in Fig. 4. Higher section transformation ratios result in lower efficiencies with the peak efficiency occurring at $\rho_{sec} = 1$. Because of the perturbative analysis, (5) matches well with simulations for higher efficiency values and always gives a pessimistic estimate. In Section V-A, design parameters of two eight-way lumped quarter-wave combiners that are used in the implementation of the two PA array prototypes in this work are discussed. The first combiner has $\rho_{\rm comb} = 1$ ($\rho_{sec} = 8$), $Q_L = 25$, $Q_C = 20$ and an efficiency of 75% from full EM simulation as well as measurement of the test-structure. The second combiner has $\rho_{\rm comb} = 2$ ($\rho_{sec} = 16$), $Q_L = 12$ and $Q_C = 50$ and an efficiency of 65% from EM simulations. Both efficiency numbers are close to the predicted values shown in Fig. 4. A comparison of the lumped quarter-wave combiner's performance with conventional power combiners (three-level cascade of 2:1 Wilkinsons and a zero-degree combiner) is discussed in Section V-A.

This non-isolating combiner also exhibits the desired load modulation property for linear output amplitude ($A_{\rm out}$) versus m when used with ideal voltage-source-like switching PAs as

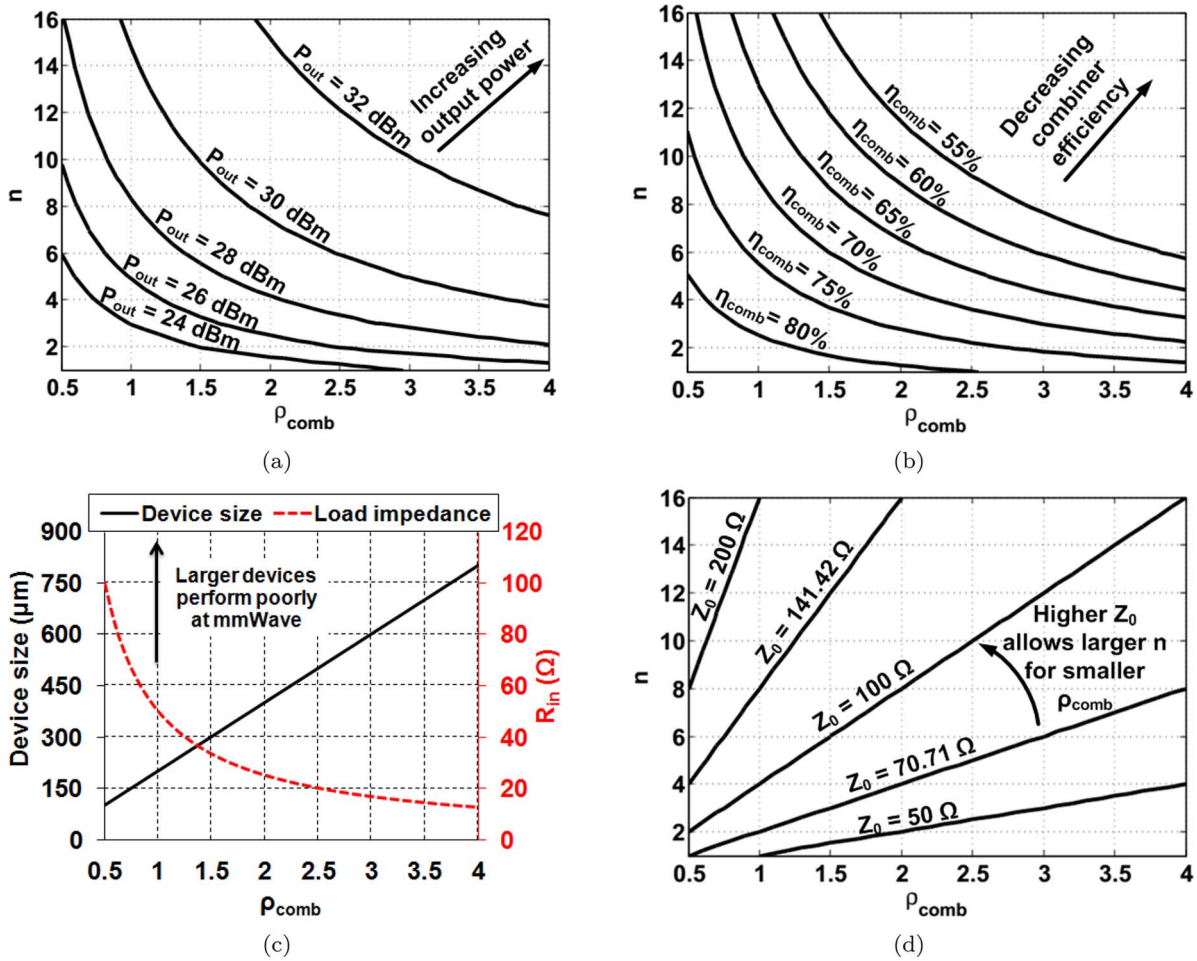


Fig. 5. (a) PA array output power and (b) combining efficiency as a function of the combiner's impedance transformation ratio $\rho_{\rm comb}$ and the number of elements combined n. (c) Device size and load impedance of each PA unit-cell as a function of $\rho_{\rm comb}$. (d) Effective characteristic impedance Z_0 of each spiral π section as a function of $\rho_{\rm comb}$ and n. The spirals in the combiner are assumed to have $Q_L = 25$ and $Q_C = 20$. $R_{\rm load} = 50\ \Omega$. A two-stage 45-nm SOI CMOS Q-band class-E-like PA design with a two-stacked driver stage and a four-stacked main PA presented in [9] is used as the unit-cell in this study.

discussed in Section II-B. We impose an additional constraint that an OFF unit-cell presents a short-circuit impedance to the combiner's input. This short-circuit is transformed by the lumped quarter-wave section to an open at the output of the combiner thus ensuring that no power is dissipated by OFF sections. Furthermore, the ON unit-cells see an impedance $R_{\rm in}(m) = Z_0^2/(mR_{\rm load})$ which is the desired load modulation effect $(R_{\rm in}(m) \propto 1/m)$.

C. Factors Affecting Choice of n and $\rho_{\rm comb}$

This section describes considerations for the design of a PA array utilizing the proposed quarter-wave lumped combiner to achieve a desired output power and efficiency. Based on the input impedance presented by the combiner, the PA unit-cell can be scaled and will deliver a saturated output power $P_{\rm unit}$ that is inversely proportional to $R_{\rm in}$, $P_{\rm unit} \propto 1/R_{\rm in}$. Note that this is a consequence of circuit scaling and not of switch-mode operation. Hence, the total output power is

$$P_{\rm out} = n \times \eta_{\rm comb} \times P_{\rm unit} \propto n \times \eta_{\rm comb} \times \frac{1}{R_{\rm in}} \tag{8}$$

$$\Rightarrow P_{\rm out} \propto \frac{n\eta_{\rm comb}\rho_{\rm comb}}{R_{\rm load}}. \tag{9}$$

Fig. 5(a) and (b) show the theoretical output power (from (9)) and combining efficiency (from (5)), as a function of $\rho_{\rm comb}$ and n, of a PA array that uses the proposed n-way lumped quarter-wave combiner. A two-stage 45-nm SOI CMOS Q-band class-E-like PA unit-cell with a two-stacked driver stage and a four-stacked main PA presented in [9] (also used in the watt-class PA array prototype) is used for this study to determine the constants of proportionality. It delivers a saturated $P_{\rm unit} =$ 20.3 dBm to a 50 Ω load with a PAE of 15.4%. The largest power device in the PA unit-cell has a width of 200 μm. The spirals in the combiner are assumed to have $Q_L = 25$ and $Q_C = 20$. The figures indicate that higher output powers and lower combiner efficiencies are associated with larger n and $\rho_{\rm comb}$. Lower n values require higher $\rho_{\rm comb}$ values for a given output power level. However, from Fig. 5(c), it can be seen that the device size used in the unit-cells scales linearly with $\rho_{\rm comb}$. Devices larger than 200 μm pose considerable layout challenges and typically suffer significant performance degradation at mmWave frequencies [9], [31]. This consideration sets the practical upper limit on $\rho_{\rm comb}$. Fig. 5(d) shows that a higher Z_0 is needed as n increases for a given $\rho_{\rm comb}$. The achievable Z_0 sets the practical upper limit on n for a given $\rho_{\rm comb}$, and the higher effective Z_0

achievable in the lumped quarter-wave combiner helps in this regard. For comparison, a conventional transmission-line-based n-way Wilkinson combiner would be limited to $n = 4$ and $P_{\rm out} = 25.2$ dBm using 200 μm devices for the unit-cells since on-chip low-loss transmission lines with $Z_0 > 100\ \Omega$ that satisfy electromigration constraints are impossible to achieve. However, the proposed combiner allows Z_0 as high as 200 Ω at 45 GHz which enables 16 elements to be combined yielding $P_{\rm out} = 30.2$ dBm for the same PA unit-cell device size ($P_{\rm out} = 27.8$ dBm with $n = 8$, $Z_0 = 141.42\ \Omega$ as implemented in the watt-class PA array prototype and $P_{\rm out} = 29.3$ dBm with $n = 12$, $Z_0 = 173.2\ \Omega$). The efficiency would also be higher for the proposed combiner as a narrow $Z_0 = 100\ \Omega$ line would have higher loss than the Q_L, Q_C values assumed here.

IV. DAC Linearity and Efficiency Under Backoff

The relationship between $A_{\rm out}$ and m deviates from the linear function due to non-idealities such as finite output conductance of the OFF PA unit-cells and deviation of the mmWave switching PA unit-cell from ideal voltage-source-like behavior. Each of these non-idealities are discussed in the following subsections along with guidelines on how to mitigate their effect. The differential nonlinearity (DNL) and integral nonlinearity (INL) (using the end-point fit definition) of the output amplitude of the PA array are used to determine the extent of nonlinearity. An eight-way combiner designed to have $R_{\rm in}(8) = 25\ \Omega$ for $R_{\rm load} = 50\ \Omega$ ($L = 353$ pH, $C_p = 35.4$ fF, $Z_0 = 100\ \Omega$ at 45 GHz) is chosen for this study.

1) Deviation of Class-E-Like PA Unit-Cells From Voltage-Source-Like Behavior: In Section II-B, it was stated that switching PAs typically exhibit an inverse linear relationship between output power and load impedance. However, the various non-idealities at mmWave frequencies (such as lack of square-wave drives leading to soft-switching, impracticality of harmonic shaping of voltages and currents due to low-Q filters) result in deviation from ideal switching characteristics leading to departure from the aforementioned relationship. The one-bit supply-switched Q-band 45nm SOI CMOS power DAC unit-cell (Fig. 14(a)) presented in [25] and used in the three-bit digital to mmWave PA array prototype is used to study the interaction of stacked switching-class mmWave PAs and their load impedance. It consists of a two-stacked class-E-like driver stage followed by a two-stacked class-E-like main amplifier (design details are summarized in Section V-B). Fig. 6(a) shows the simulated output power variation of the unit-cell when it is presented with the (real) input impedance of the ideal eight-way lumped quarter-wave combiner ($R_{\rm in}(m) = 200/m\ \Omega$). The deviation from the desired linear profile is due to the non-voltage-source-like behavior of the PA unit-cell. This deviation translates to a nonlinear $A_{\rm out}$ vs. m profile. The effect of this on the INL and DNL of the PA array is shown in Fig. 6(b). From these curves, it is evident that the non-ideal behavior of the unit-cells results in $A_{\rm out}$ always being higher than the desired ideal value. It is also interesting to note that a source resistance of 15 Ω models the behavior of the switching PA unit-cell almost exactly (Fig. 6(a)).

The presence of an equivalent source resistance implies that the output voltage swing will increase slightly as the load

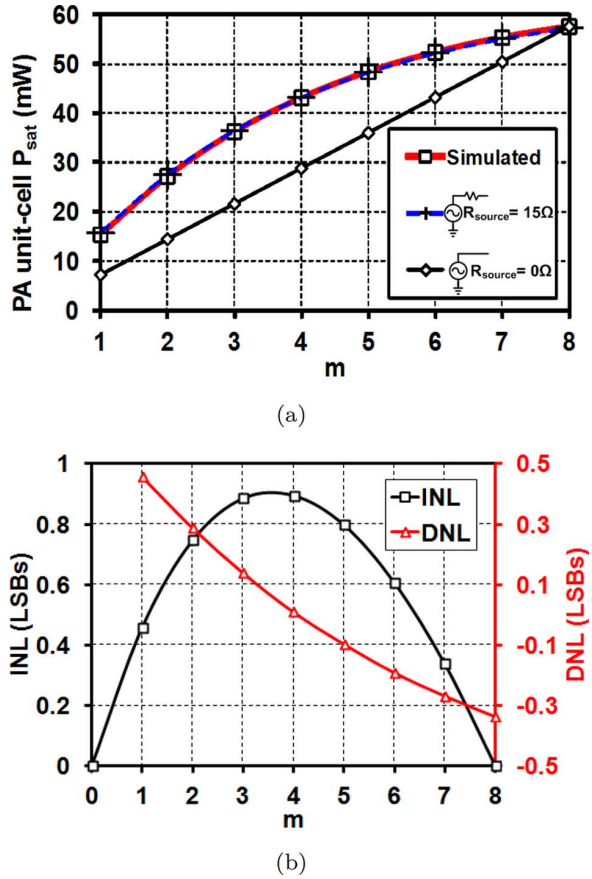
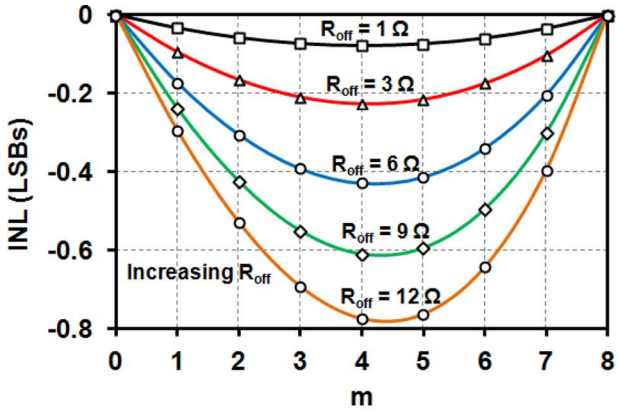


Fig. 6. (a) Output power variation of the PA unit-cell (simulated with PDK devices, modeled as an ideal voltage source and modeled as a voltage source with a 15 Ω source resistance) when presented with the input impedance of a lossless eight-way quarter-wave lumped combiner at 45 GHz. The parameters of the combiner are chosen such that it presents 25 Ω impedance to each PA unit-cell when $m = n = 8$ ($R_{\rm in}(m) = 200/m\ \Omega$). (b) The simulated INL and DNL of a PA array with the real PA unit-cell, lossless combiner and short-circuit OFF PA unit-cell impedance.

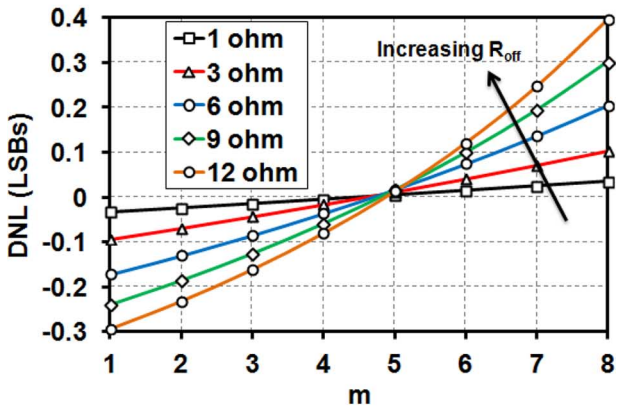
impedance increases. This increase is smaller for unit-cells designed to have a smaller equivalent source impedance. Nevertheless, the supply voltage of the PA unit-cells (or their input power) must be limited to the value that keeps all devices safe from breakdown for $m = 1$ case when the ON PA unit-cell is presented with the highest impedance.

2) Finite Output Conductance of OFF PA Unit-Cells: The load modulation property of the lumped quarter-wave combiner relies on the OFF PA unit-cells presenting perfect short-circuits at their outputs. A non-zero OFF PA unit-cell output resistance ($R_{\rm off}$) is transformed to a finite resistance in parallel with $R_{\rm load}$ and dissipates a portion of the power output of the ON unit-cells. This causes a degradation in the efficiency of the combiner which varies with m. Hence, from an efficiency stand-point, $R_{\rm off}$ must be chosen to be as small as possible. Non-zero $R_{\rm off}$ also modifies the variation of $R_{\rm in}(m)$. These factors cause the PA array to deviate from the linear $A_{\rm out}$ vs. m profile. Assuming a perfectly lossless combiner and ideal voltage-source behavior of the PA unit-cells, the output amplitude variation with m accounting only for the finite output conductance of the OFF PA unit-cells may be expressed as

$$A_{\rm out}(m) = \frac{m}{1 + \frac{(n-m)R_{\rm load}R_{\rm off}}{Z_0^2}} \sqrt{\frac{2R_{\rm load}}{n} P_{\rm unit}(n)}. \quad (10)$$



(a)



(b)

Fig. 7. Effect of finite OFF PA unit-cell output conductance $(1/R_{\rm off})$ on the INL and DNL of a PA array with the eight-way quarter-wave combiner assuming ideal voltage-source behavior of the PA unit-cell and lossless combiner at 45 GHz. The combiner parameters are chosen such that $R_{\rm in}(8) = 25\ \Omega$ with $R_{\rm load} = 50\ \Omega$.

Fig. 7(a) and (b) show the resulting effect on the INL and DNL respectively, of the PA array. Simulations are not depicted in Fig. 7(a) and (b) as they match the theory exactly as no approximations were involved in deriving the equation above. It is seen that for $R_{\rm off} < 3\ \Omega$, the INL and DNL are below 0.25 LSB. It must be noted that a non-zero $R_{\rm off}$ always results in negative INL values, i.e., $A_{\rm out}(m)$ is always smaller than the ideal value. Moreover, the amount by which it is smaller increases as $R_{\rm off}$ increases.

The opposing effects of the non-idealities of the PA unit-cell and non-zero $R_{\rm off}$ can be used to compensate for each other. *In fact, as is described in the Appendix, choosing* $R_{\rm off}$ *to be equal to the equivalent source resistance of the ON PA unit-cells (*15 Ω *in this case) should perfectly linearize the PA simply by superposition, as this non-isolating combiner satisfies the symmetry conditions of* (15), (18)*, and* (23). To accomplish this, $R_{\rm off}$ can be made programmable (not pursued in this work) by programming the bias voltage applied at the drain of transistor M_5 in Fig. 14(a). *This internal compensation of sub-block non-idealities comes at the price of efficiency under backoff*—the finite $R_{\rm off}$ is reduces the combiner's efficiency under back-off to compensate for the excess power that the PA unit-cells deliver.

To verify this, the effects of all the above non-idealities on the INL and DNL of the PA array are simulated and the results are summarized in Fig. 8(a) and (b). The real post-layout EM-simulated combiner with $R_{\rm in}(8) = 25\ \Omega$ for $R_{\rm load} = 50\ \Omega$ ($L = 353$ pH, $C_p = 35.4$ fF, $Z_0 = 100\ \Omega$ at 45 GHz) and used in the direct digital to mmWave power-DAC prototype is utilized. Different $R_{\rm off}$ values are achieved by changing the bias voltage at the drain of transistor M_5 in Fig. 14(a). It is seen that the maximum deviation from the ideal linear profile is due to the non-voltage-source-like behavior of the ON PA unit-cells. Finite $R_{\rm off} = 3\ \Omega$ of the OFF unit-cells (achieved in the power-DAC prototype) partially compensates for the non-ideal behavior of the ON PA unit-cells. Setting $R_{\rm off} = 15\ \Omega$ results in the best linearity of the PA array with simulated DNL and INL being less than 0.025 LSB and 0.03 LSB respectively demonstrating the internal compensation mechanism available.

Fig. 8(c) depicts the overall drain efficiency as a function of output power as m is varied. When $R_{\rm off} = 0\ \Omega$, the primary mechanism of efficiency degradation under backoff is the effect of load modulation on the efficiency of the ON PA unit-cells. As $R_{\rm off}$ is increased, the efficiency of the combiner under backoff degrades, degrading the overall drain efficiency. $R_{\rm off} = 3\Omega$ (achieved in the power-DAC prototype) results in a $DE_{-6\rm dB}/DE_{\rm peak} = 69.8\%$, very close to the measured performance described in Section VI, while $R_{\rm off} = 15\Omega$ (from linearity optimization) results in $DE_{-6\rm dB}/DE_{\rm peak} = 58.4\%$. The latter is still better than class-B-like backoff. *Hence, while PA unit-cell non-idealities do introduce a linearity vs. backoff efficiency trade-off in the proposed architecture, this trade-off is significantly relaxed when compared with conventional PAs.* Reducing the effective source impedance of the switching PAs, through the use of more scaled CMOS technology nodes for instance, would further relax this trade-off and reduce the efficiency-under-backoff penalty associated with achieving linearity.

V. Circuit Implementation Details

Two PA prototypes are fabricated in a 45 nm SOI CMOS process to verify our claims about the proposed combiner and linearizing power-DAC architecture. The first prototype, a 33–46 GHz watt-class PA array (shown in Fig. 9), demonstrates the utility of the lumped quarter-wave combiner as a highly efficient, large-scale power combiner. No digital controls are implemented in this prototype. Eight stacked-FET PA unit-cells are combined using the eight-way lumped quarter-wave combiner. The input power is delivered by means of an eight-way input splitter whose details are discussed in Section V-C. The second prototype is a three-bit digital to mmWave PA array (shown in Fig. 10) based on the architecture described in Section II. Eight supply switched stacked-FET PA unit-cells are power combined using the lumped quarter-wave combiner. Eight digital control lines $(b_1$–$b_8)$ determine the ON/OFF state of the unit-cells and thereby determine the PA array's output modulation. The lengths of these digital control lines are equalized to minimize skew in the digital control word input to the PA array during modulation.

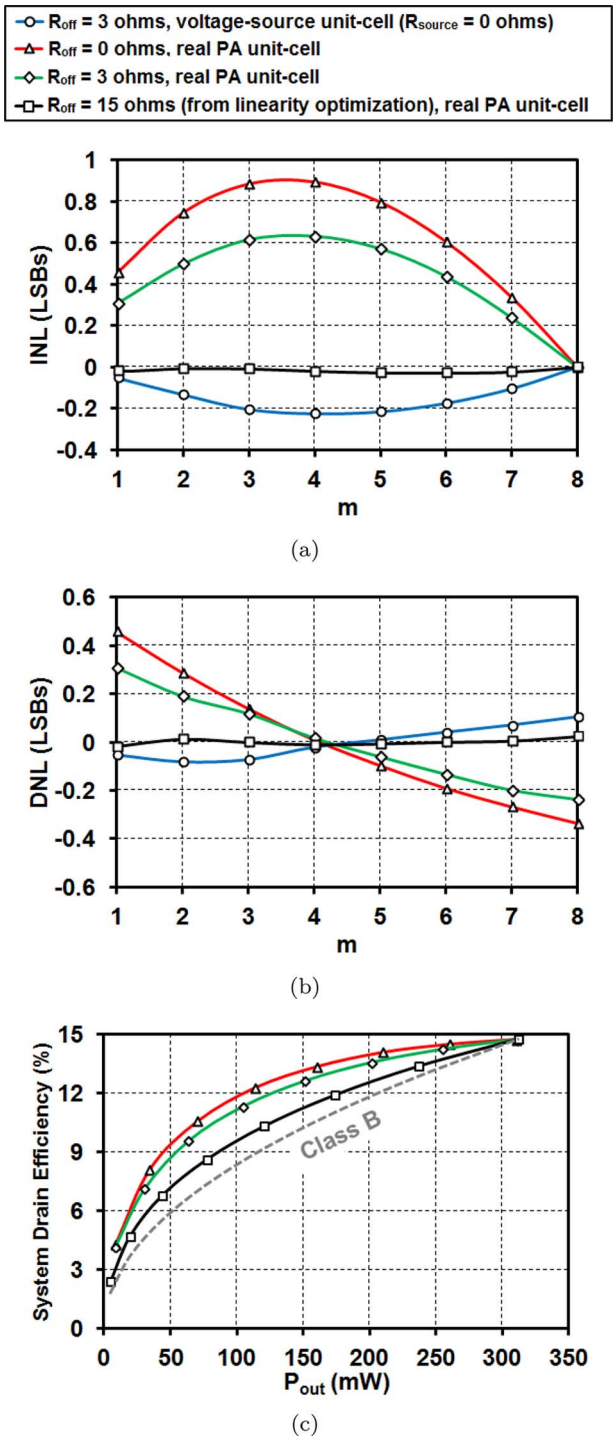


Fig. 8. Composite effect of the PA unit-cell non-idealities on the (a) INL and (b) DNL and (c) system drain efficiency of the PA array.

A. Combiner Design

Both prototypes use eight-way lumped quarter-wave combiners. However, the $\rho_{\rm comb}$ values and hence the design parameters of the combiners differ. In the watt-class PA array prototype, the combiner is designed to achieve $R_{\rm in}(8) = 50\ \Omega$ for $R_{\rm load} = 50\ \Omega$ ($\rho_{\rm comb} = 1$, $L = 500$ pH, $C_p = 25$ fF, $Z_0 = 141.42\ \Omega$ at 45 GHz). Each spiral's outer dimensions are 86 μm $\times$ 86 μm. Fig. 11(a) shows the schematic broadband model of the spiral. The basic lumped model of the spiral in [32]

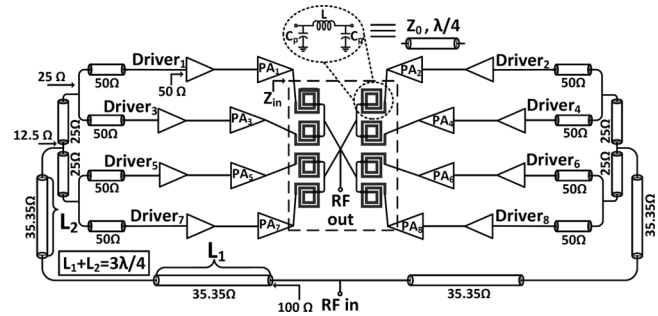


Fig. 9. Schematic of the 33–46 GHz watt-class PA array prototype.

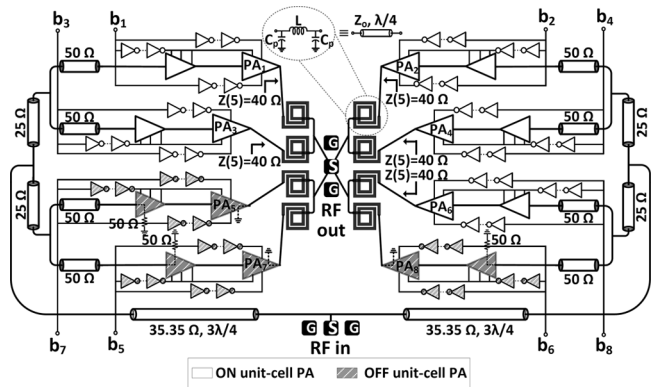


Fig. 10. Schematic of the three-bit digital to mmWave PA array prototype. The state of the array for $n = 8, m = 5, Z(8) = 25\ \Omega$ is shown for illustration.

is augmented with an $L-R$ ladder to model the skin-effect, and an additional series inductance in the substrate path to model the finite inductance of the return path through the substrate and surrounding ground plane. The spiral is simulated in IE3D, an EM simulator, and was implemented as a test structure for measurement. Fig. 11(b)–(e) compares measurement, EM-simulation, and broadband model based equivalent π-model components across frequency. A good agreement is seen, and $Q_L = 25$ and $Q_C = 20$ from EM simulations at 45 GHz. There is potential for asymmetry between the input ports of the combiner in the watt-class PA array prototype due to the coupling of magnetic fields between adjacent spirals. Fig. 12(b) shows the EM simulated input reflection coefficient $|\Gamma_{\rm in}|$ of all eight input ports of the combiner when all eight ports are identically excited. As expected, the outer 4 spirals which experience magnetic coupling from only one adjacent spiral have identical profiles whereas the inner four spirals which are coupled to two adjacent neighbors have a *slightly* different profile. The distance between adjacent spirals was chosen to be greater than 45 μm which significantly reduces the coupling and the maximum difference in $|\Gamma_{\rm in}|$. Two combiner test-structures (shown in Fig. 12(a)) are also fabricated in order to assess the combining efficiency and the extent of asymmetry. The test-structures had all but one input port (a different one in the two test structures) terminated with 50 Ω resistors on-chip. It is seen that the measurements of the two combiner breakouts are almost identical (Fig. 12(c)). The combiner efficiency is defined as the ratio of the available output power to the available input power and is evaluated as $8|S_{21}|^2$ where S_{21} is the measured forward transmission parameter of

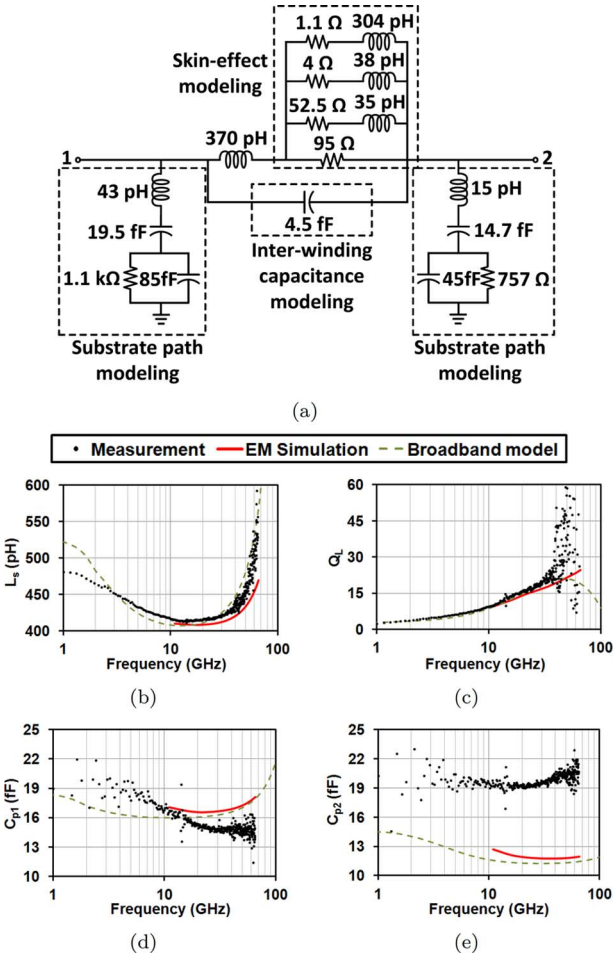


Fig. 11. (a) Broadband model for the spiral inductor in the eight-way quarter-wave lumped combiner used in the 45nm SOI CMOS watt-class PA array prototype. Measurement, EM simulation, and broadband model simulation results of the spiral test-structure showing the (b) spiral's inductance, (c) its inductive quality factor, and (d), (e) shunt capacitances of its equivalent π-model C_{p1}-R_{p1}-L_s-R_{Ls}-C_{p2}-R_{p2}).

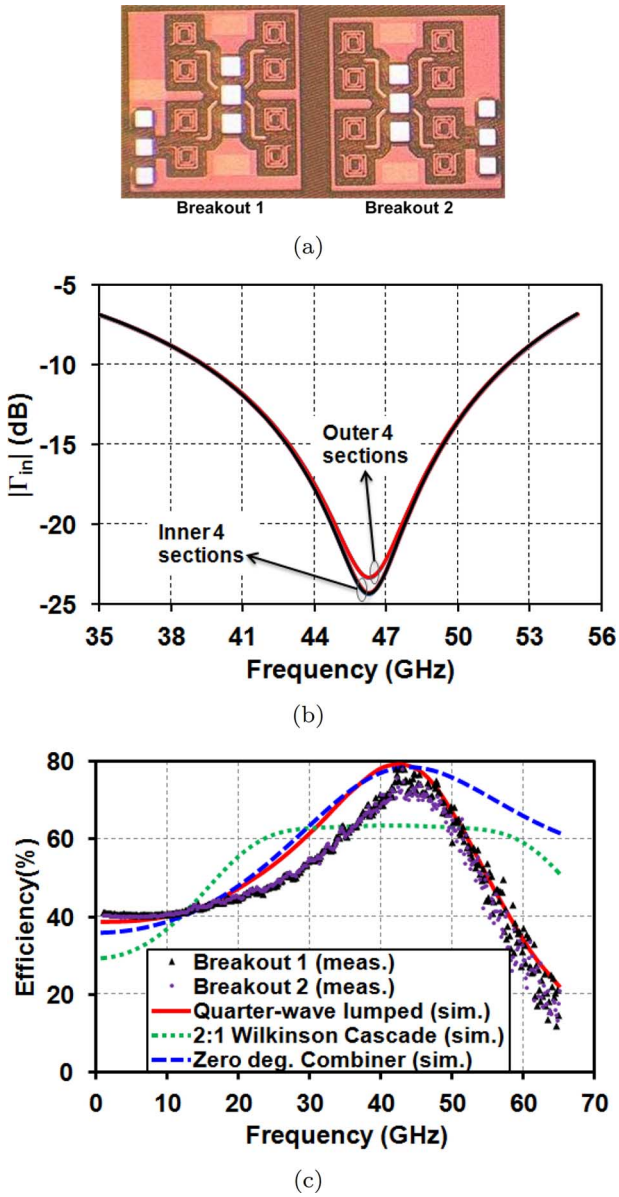


Fig. 12. (a) Chip photograph of the eight-way lumped quarter-wave combiner test-structures. (b) EM simulated input reflection coefficient of all eight input ports of the combiner when all ports are identically driven. (c) Comparison of the measured combining efficiency to EM simulations of the proposed eight-way lumped quarter-wave combiner as well as three-level cascade of 2:1 Wilkinsons and an optimum eight-way zero-degree combiner.

the test structure. A combiner efficiency of 75% at 45 GHz (78% at 48 GHz) and excellent agreement with EM simulations are seen in Fig. 12(c).

For comparison, eight-way combining via a three-level cascade of 2:1 Wilkinsons is simulated to achieve a combining efficiency of only 63%. The low efficiency of the Wilkinson combiner is a combination of two factors—multiple cascading stages, and the quarter wavelength restriction on the length of the transmission lines used. An optimum zero-degree combiner (Fig. 2(c)) subject to layout and impedance transformation restrictions is also shown to have a simulated efficiency of 78% at 45 GHz (Fig. 12(c)). The combiner's parameters are obtained by an exhaustive search of possible combinations of Z_1, Z_2, L_1, L_2 that present an input impedance of 50 Ω when the combiner is loaded with a load resistance of 50 Ω, while maximizing efficiency for typical transmission line attenuation constants in the 45 nm SOI CMOS BEOL. It is clear that an eight-way zero-degree combiner achieves no better performance than our proposed lumped quarter-wave combiner. It is also significantly harder to design since it requires multiple optimization iterations. Furthermore, while the zero-degree combiner satisfies (15), namely the symmetry condition described in the Appendix required for linear A_{out} vs. m, it fails to satisfy (23) which is required for the m ON PA unit cells to see identical load impedances. This makes the design of the PA unit-cells challenging. However, the quarter-wave lumped combiner satisfies the high level of symmetry dictated by (15), (18), and (23).

The combiner used in the three-bit digital to mmWave PA array prototype is designed to have $R_{\text{in}}(8) = 25\ \Omega$ for $R_{\text{load}} = 50\ \Omega$ ($\rho_{\text{comb}} = 2$, $L = 353$ pH, $C_p = 35.4$ fF, $Z_0 = 100\ \Omega$ at 45 GHz). This combiner has a peak efficiency of 65% and the spiral used has $Q_L = 12$ and $Q_C = 50$ from EM simulations. The lower peak efficiency is due to the higher transformation ratio and the lower Q_L of the spirals and is close to the theoretical prediction (Fig. 4). A design procedure identical to the one previously described was used.

B. Stacked-FET PA Unit-Cells

The PA unit-cell (Fig. 13) used in the watt-class PA array prototype is based on a two-stage design, where the driver is a two-stacked Class-E-like PA while the output stage is a four-stacked class-E-like PA. Both the stages are designed based on a loss-aware class-E design methodology [33] applied to the context of device stacking as discussed in detail in [5] and [9]. For long-term reliability, the maximum voltage swing across any two device terminals is limited to a peak value of $2 \times V_{dd} = 2.4$ V. The two-stacked and four-stacked PA breakouts were presented in [5] and the cascaded two-stage breakout was presented in [9]. The breakout of the PA unit-cell was measured to have a peak small-signal gain of 24.9 dB, saturated output power of 20.1 dBm at 47 GHz with peak drain efficiency and PAE of 15.6% and 15.4% respectively.

The one-bit mmWave CMOS power DAC (Fig. 14(a)) mentioned in Section IV-A is used as the unit-cell in the three-bit digital to mmWave PA array prototype. A broad outline of its operation and performance is presented here, and the reader is directed to [25] for additional details. It consists of a two-stacked class-E-like driver stage followed by a two-stacked class-E-like main amplifier. Modulation capability is incorporated into the PA by means of digitally controlled switches (all controlled by a single-bit b_n) driven by sized inverter chains. These switches ensure that an OFF PA consumes no DC power, preserves its input match and presents a short-circuit impedance to the combiner.

Various design trade-offs exist with respect to modulation speed, supply switch design and dynamic power dissipation, impact of digital path delays, and ground and supply bounce. The modulation speed is essentially limited by the bias-path RC time constants associated with nodes whose bias voltages are changed during turn ON/OFF. Smaller values of the biasing resistors result in fast settling, but can affect mmWave static performance by dissipating mmWave power. In the one-bit power DAC cell, the biasing resistors were designed to ensure ~200 ps rise/fall times while not noticeably degrading static performance. The supply-switch design also presents a trade-off—a larger supply-switch minimizes degradation of static drain efficiency and PAE but introduces parasitic capacitance that must be charged and discharged upon turn-ON/OFF, resulting in dynamic power dissipation and reduction of average drain efficiency and PAE under modulation. In the designed unit-cell, the supply-switch size was chosen to maximize average PAE while degrading static PAE by ~3% in simulation. The reader is directed to [25] for a detailed description of the various design trade-offs.

A breakout of the one-bit power DAC cell was measured to have a peak gain of 20 dB in small-signal and saturated output power of 18.2 dBm at 47 GHz and peak drain efficiency and PAE of 16.3% and 15.3% respectively. OOK modulation using a 2^7-1 PRBS was applied along with a 47 GHz carrier input at the class-E drive level. Modulation rates beyond 1 Gbps could not be applied owing to the limitation of the PRBS generator. Fig. 14(b) summarizes the measured large-signal average performance metrics for different modulation speeds. At 400 Mbps, an average output power of 15.7 dBm was measured, and an average drain efficiency of $\approx$ 10% is maintained. In Fig. 14(c), the time-domain waveform is shown for a modulation rate of 1 Gbps. The rise and fall times shown in Fig. 14(d) and (e), respectively, were measured to be $\sim$ 213 ps and $\sim$ 225 ps respectively with a measured extinction ratio of 32 dB. These indicate that the three-bit digital to mmWave PA array is capable of supporting GSps modulation rates.

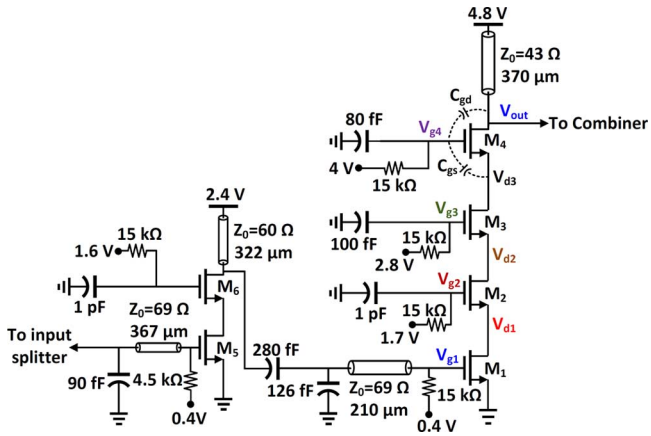


Fig. 13. Schematic of the two-stage 45 nm SOI CMOS stacked PA unit-cell used in the watt-class PA array prototype.

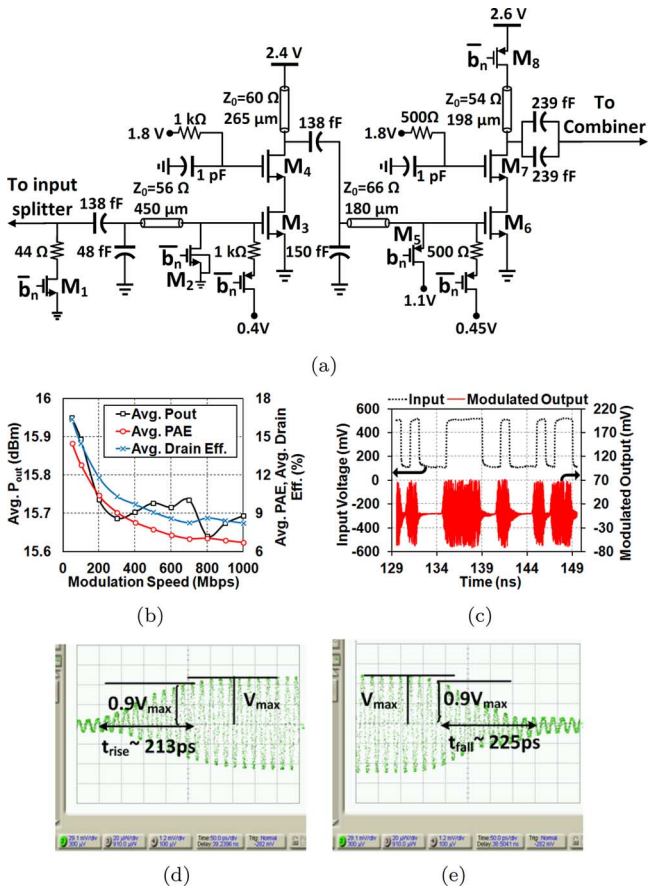


Fig. 14. (a) Schematic of the one-bit DAC PA unit-cell used in the three-bit digital to mmWave PA array prototype. (b) Measured one-bit DAC cell average large-signal metrics at 47 GHz with 2^7-1 PRBS OOK at different speeds. (c) Measured DAC cell time-domain output, (d) rise time and (e) fall time with 1 Gbps 2^7-1 PRBS OOK input and 47 GHz carrier (Setup losses have not been de-embedded).

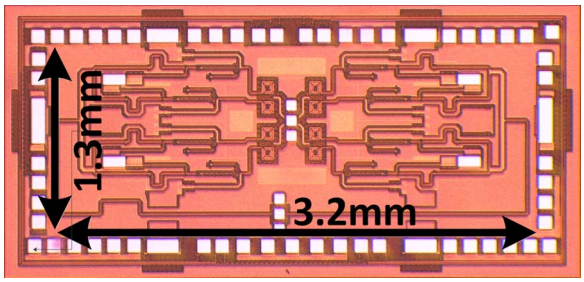


Fig. 15. Chip microphotograph of the 33–46 GHz watt-class PA array prototype. Chip dimensions are 3.2 mm × 1.3 mm without pads.

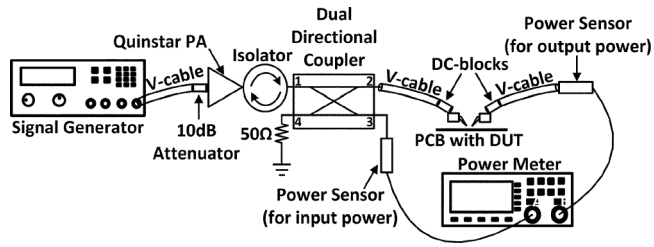


Fig. 16. Setup used for large-signal measurements of the watt-class PA array and the three-bit digital to mmWave PA array prototypes.

C. Power Splitter Design

The eight PA unit-cells in both prototypes receive their input power via an eight-way input power splitter. A three-stage design is implemented where the two stages closest to the PA unit-cell inputs are designed in a current-splitting fashion and the last stage performs the necessary impedance transformation using $3\lambda/4$ lines. The current-splitting technique, similar to the zero-degree combiner, eschews the quarter-wave lines of a cascaded Wilkinson splitter for shorter lines only limited by layout considerations. This results in a compact structure which achieves a simulated efficiency of 37%. The input pad is slightly offset from the center to ensure that the prototypes can be measured in a probed configuration. The $3\lambda/4$ line on that side is meandered to ensure equal line lengths on both sides and negligible amplitude/phase imbalance.

VI. PA Prototype Measurement Results

The 3.2 mm × 1.3 mm watt-class PA array prototype (Fig. 15) is probed in a chip-on-board configuration. The simulated and measured small-signal S-parameters are shown in Fig. 17(a). A peak S_{21} of 19 dB is measured in small-signal at 50 GHz. Considering the efficiency of the combiner (75% or 1.25 dB loss), efficiency of the input splitter (37% or 4.3 dB loss) and small-signal gain of the PA unit-cells (25 dB), the expected small-signal gain of the PA array is $25 - 1.25 - 4.3 = 19.45$ dB which is consistent with measurement (19 dB). Fig. 16 shows the setup that is used for measurement. The measured efficiency and saturated output power across frequency are shown in Fig. 17(b). The PA maintains 1 dB-flatness in saturated output power (26–27 dBm) from 33–46 GHz while the measured PAE varies between 8.8% to 10.7% in this range. It is interesting to note that the PA array achieves wider-bandwidth performance than the PA unit-cells themselves (when they are loaded with a 50 Ω load impedance [9]) since the eight-way lumped quarter-wave combiner's input impedance tracks the optimal load impedance required by the PA unit-cells over nearly the entire Q-band. Measurement below 33 GHz is limited by the experimental setup. The output power level of 27 dBm is quite close to the expected power level (27.8 dBm) from eight-way combining of the unit-cells using the proposed combiner with $\rho_{\text{comb}} = 1$ as described in Section III-C. The PAE at 43 GHz (10.4%) is close to the expected PAE ($\approx 15\% \times 75\% = 11.25\%$) based on the unit-cell and combiner efficiencies. The measured large-signal performance at 37 GHz, 42.5 GHz and 46 GHz are summarized in Fig. 17(c). Table I compares the measured performance to state-of-the-art mmWave PAs. The implemented PA achieves the highest output power (27.2 dBm) amongst reported CMOS mmWave PAs and a very high ITRS figure-of-merit. The PA reported in [4] uses ideal off-chip DC feed inductors as well as ideal external 3 dB differential combining. *When this is factored in, our implemented PA achieves approximately* 5 *dB* (3×) *higher output power than any other CMOS mmWave PA*. The implemented PA array also achieves the highest fractional bandwidth (33%). When compared with the state-of-the-art SiGe mmWave PA [34], we see that aggressive device stacking and power combining has enabled comparable performance despite the higher supply voltage of 0.13 μm SiGe. GaAs mmWave PAs [35] achieve higher output power but device stacking has narrowed the gap. Furthermore, scaled SOI CMOS enables digital-/mixed-signal intensive SoCs exploiting integration complexity for efficiency enhancement and linearization. A preliminary probed RF stress test is performed where the watt-class PA array is operated at the P_{sat} drive level for approximately 12 hours at 44 GHz. The observed variations in output power, drain efficiency and PAE are small ($<$ 0.5 dB, 1.4% and 1.4% respectively, Fig. 17(d)). Drift in the setup (Quinstar driver PA, power sensors etc.), minor probe movements and DUT self heating due to imperfect conduction of heat away from the IC may be contributing factors. The main purpose is to show the benefits of device stacking in distributing the voltage swing among the stacked devices and the absence of immediate breakdown effects despite the high supply voltages used.

The fabricated three-bit digital to mmWave PA array prototype is shown in Fig. 18 and has an active area of 3.2 mm × 1.3 mm. Small-signal S-parameter measurements shown in Fig. 19 indicate that input and output match are maintained across the digital control settings. The measured large-signal P_{out} vs. P_{in} profile of the PA array measured at 42.5 GHz can be seen in Fig. 20(a) across m. A P_{sat} of 23.4 dBm is achieved when all PAs are ON. The measured saturated output voltage (Fig. 20(b)) displays the expected linear profile with *m* demonstrating its utility as a three-bit mmWave power DAC. The DNL and INL of the prototype are shown in Fig. 22. The DNL never exceeds 0.5 LSB and the INL is always within 1 LSB. The INL and DNL values and shape as a function of m match the expected profile from Fig. 8(a) and (b) for $R_{\text{off}} = 3\ \Omega$ fairly closely. The simulated phase-shift as a function of digital control word is shown in Fig. 20(b). The AM-PM nonlinearity is very small (maximum phase difference of 0.355°

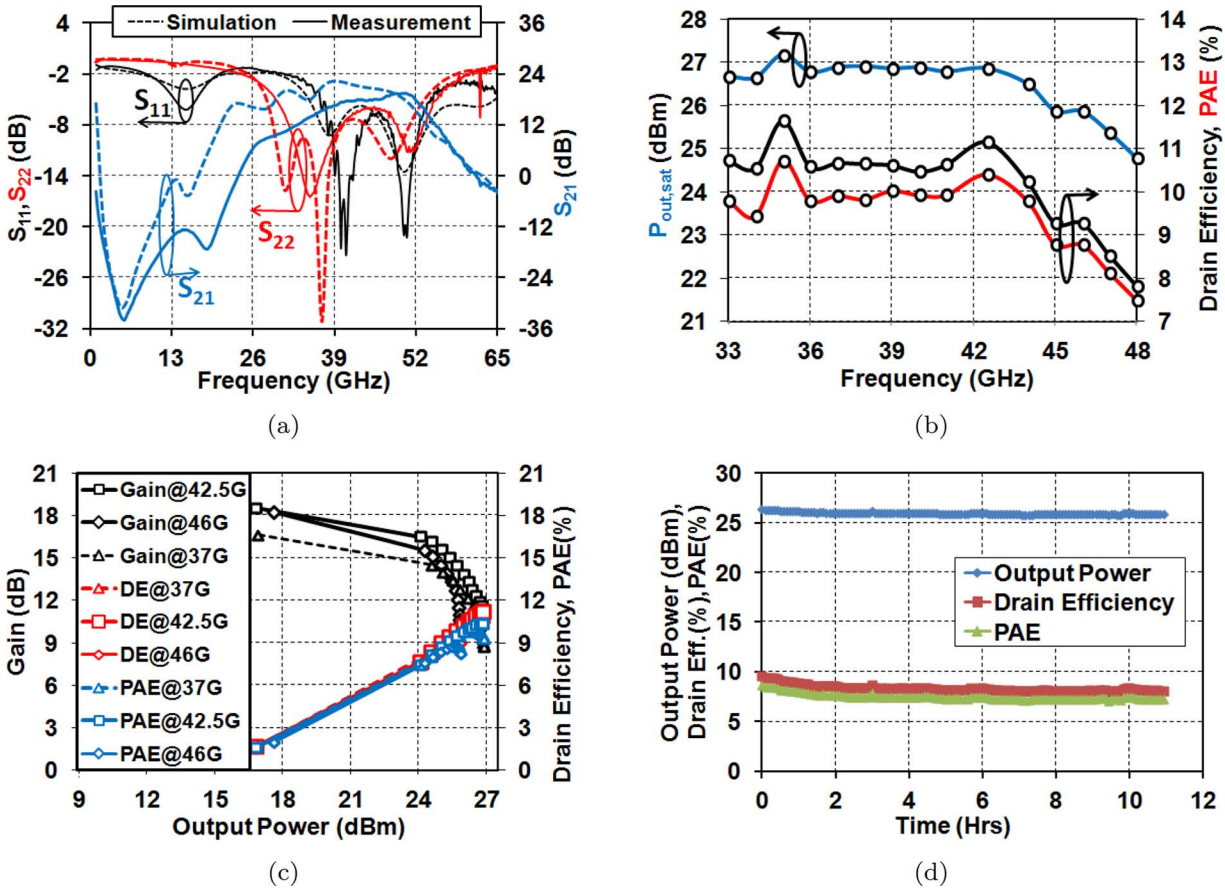


Fig. 17. (a) Simulated and measured small-signal S-parameters of the watt-class power-combined PA array. Measured results showing (b) large-signal saturated output power, peak PAE and drain efficiency at peak PAE across frequency. (c) Gain, PAE and drain efficiency across output power levels for three frequencies. (d) Results of a preliminary probed stress test performed on the PA for 12 hours.

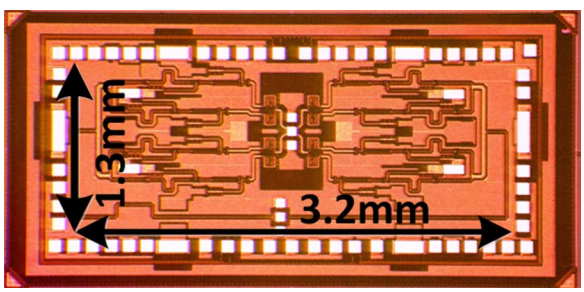


Fig. 18. Chip photograph of the Q-band three-bit digital to mmWave PA array prototype.

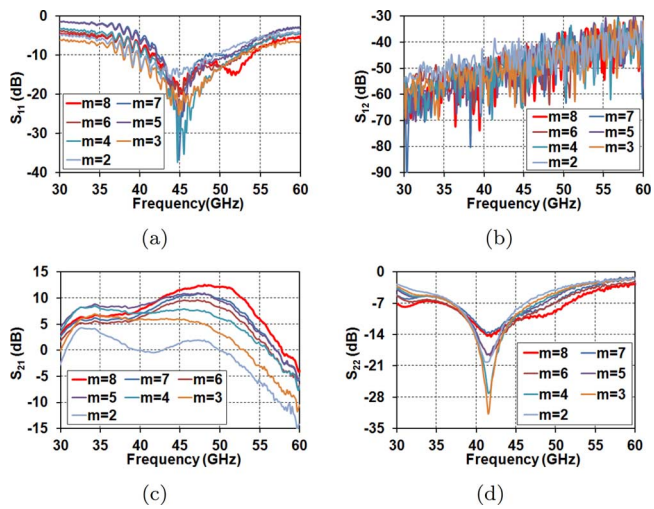


Fig. 19. Measured small-signal S-parameters vs. digital control setting of the three-bit digital to mmWave PA array prototype.

between the outputs at $m = 1$ and $m = 8$). Fig. 21 shows drain efficiency and PAE as a function of output power at 42.5 GHz across digital control settings. Our measurements show a 2.25× improvement in drain efficiency and a 1.75× improvement in PAE at 6 dB back-off over the baseline case where all PAs are always kept ON. $DE_{-6\text{dB}}/DE_{\text{peak}} = 70.7\%$ (close to the expected value for $R_{\text{off}} = 3\ \Omega$ as discussed in Section IV) and $PAE_{-6\text{dB}}/PAE_{\text{peak}} = 67.7\%$. The peak PAE (6.7%) and output power (23.4 dBm) are lower than simulated (14% and 24.5 dBm) due to lower PAE in the unit cell in measurement vis-a-vis simulation and frequency mismatch between the PAs and the combiner. The PAE and gain under back-off (lower values of m) are also expected to be higher in an SoC transmitter implementation, either through elimination of the input 50 Ω terminations presented by OFF PAs (which degrade PAE and gain under back-off) through co-design with the preceding driver stage or through the addition of another driver stage within each supply-switched unit-cell. Table I compares this

TABLE I
COMPARISON WITH STATE-OF-THE-ART MMWAVE PAS WITH $P_{sat} > 20$ dBm OR EMPLOYING EFFICIENCY ENHANCING ARCHITECTURES

Work	[18]	[6]	[23]	[11]	[8]	[36]	[4]	**This work**	**This work**	[34]	[35]
Technology	40nm CMOS	45nm SOI CMOS	40nm CMOS	40nm CMOS	45nm CMOS SOI	45nm SOI CMOS	40nm CMOS	**45nm SOI CMOS**	**45nm SOI CMOS**	0.13μm SiGe	120nm GaAs pHEMT
Supply (V)	0.9	5	1.2	1	2.5	4	5.1	**4.8**	**2.6**	4/2.4	6
Freq.(GHz)	80	41	60	60	42	45	45	**33-46**[2]	**42.5**	42	43.5
$\Delta f/f_0$ (%)	19.5	22	11.6	11.6	N/R[1]	13.3	15	**33**	**32**	11.9	7.5
Gain$_{max}$(dB)	18.1	8.9	29	N/A	7	7.4	>18	**19.4**	**15**	18.5	23
$P_{sat,max}$ (dBm)	20.9	21.6	22.6	15.6	18	21.3	24.3	**27.2**	**23.4**	28.4	35.4
DE$_{max}$ (%)	N/R	N/R	N/R	23[6]	33	24	21.3	**11.7**	**8.2**	N/R	N/R
$\frac{\text{DE @ 6dB back-off}}{\text{Peak DE}}$ (%)	N/R	N/R	N/R	28.5[6]	72.7	52.1	N/R	**42.7**	**70.7**	N/R	N/R
PAE$_{max}$ (%)	22.3	25.1	7	N/A	23	16	14.6	**10.7**	**6.7**	28.4	21
$\frac{\text{PAE @ 6dB back-off}}{\text{Peak PAE}}$ (%)	32.7	60	35.7	N/A	73.9	56.2	N/R	**42**	**67.7**	N/R	23.8
ITRS FOM[4]	70.5	56.8	75.6	N/A	51.1	53.8	67	**67.8**	**58.8**	73.9	84.4
Area (mm^2)	0.19	0.3	2.16	0.33	0.64	1.15	7.67	**4.16**	**4.16**	5.55	15.9
Architecture	4-way diff. power combined	4-stacked PA	8-way diff. power combined	Out-phasing	Doherty 2-stacked PAs	4-stacked 8 bit I/Q power-DAC	4-stacked 2-bit power-DAC	**4-stacked 8-way Power Combined**	**Proposed 3-bit mmWave Power DAC**	16-way power combined	16-way power combined
Fully Integrated?	Yes	Yes	Yes	Yes	Yes	Yes	No[3,5]	**Yes**	**Yes**	Yes	Yes
Integration Complexity	PA only	PA only	PA only	modulator + PA	PA only	modulator + PA	modulator + PA	**PA only**	**Direct digital to mmWave**	PA only	PA only

[1]Large-signal performance across frequency is not reported. [2]Measurement below 33GHz is limited by equipment. [3]Assumes 3dB external differential-to-single-ended converter. [4]Defined as P_{sat}(dBm) + Gain(dB) + 20 $\log_{10}$(Freq.(GHz)) + 10 $\log_{10}$(PAE). [5] Does not have an on-chip choke inductor (biased using external bias-Ts). [6]Entire system metrics (for a fair comparison) inferred from supplied graph assuming power consumption of I/Q mixer remains constant.

work with state-of-the-art CMOS mmWave PAs, some of which employ efficiency enhancing architectures. This PA achieves one of the lowest degradation in PAE under 6 dB back-off while having the highest saturated output power among PAs using such architectures. While not reflected in this table, the AM-AM and AM-PM linearity of this PA are also noteworthy.

VII. CONCLUSION

A state-of-the-art ultra-wideband watt-level CMOS PA at mmWave frequencies has been demonstrated. The PA uses a low-loss eight-way lumped quarter-wave combiner and class-E-like stacked PA unit-cells to achieve watt-class output power over nearly the entire Q-band. This is a step towards enabling large-scale deployment of low-cost, long-distance CMOS Q-band communication links. A novel architecture employing large-scale power combining, dynamic load modulation, and supply-switching has also been demonstrated and results in a high-power highly linear three-bit digital to mmWave PA array prototype with high efficiency under back-off.

APPENDIX

Consider an n-way passive and reciprocal combiner whose first n ports are inputs and the $(n+1)^{th}$ port is the output which drives an impedance Z_{load}. The combiner is driven by n identical PA unit-cells. $m(\leq n)$ PA unit-cells are ON and are modeled as a voltage source V_s in series with a source impedance Z_{on}. The OFF PA unit-cells are simply modeled as an impedance Z_{off} to ground. In order for the network including these impedances to remain the same irrespective of the value of m, the following condition must be satisfied:

$$Z_{\text{on}} = Z_{\text{off}}. \tag{11}$$

Under this condition, only the excitation changes with m and the currents and voltages of the network for all values of m may be determined by superposition. We define $Y = [y_{ij}]$ to be the complex Y-parameter matrix of this combiner together with the output impedances of the ON and OFF PA unit-cells. The combiner output may be determined as:

$$I_{n+1} = [y_{(n+1)1} + \cdots + y_{(n+1)m}]V_s + y_{(n+1)(n+1)}V_{n+1} \tag{12}$$

$$\frac{-V_{n+1}}{Z_{\text{load}}} = [y_{(n+1)1} + \cdots + y_{(n+1)m}]V_s + y_{(n+1)(n+1)}V_{n+1} \tag{13}$$

$$V_{n+1} = -\frac{\overbrace{[y_{(n+1)1} + \cdots + y_{(n+1)m}]}^{m \text{ terms}}V_s}{Z_{\text{load}}^{-1} + y_{(n+1)(n+1)}}. \tag{14}$$

If $V_{n+1} \propto m$ is desired then it follows that

$$y_{(n+1)1} = y_{(n+1)2} = \cdots = y_{(n+1)n} = a. \tag{15}$$

In addition to linearity with m, it is also desirable that each ON PA unit-cell sees the same input impedance. For this to be true, for a given m, the input currents of all the ON sections

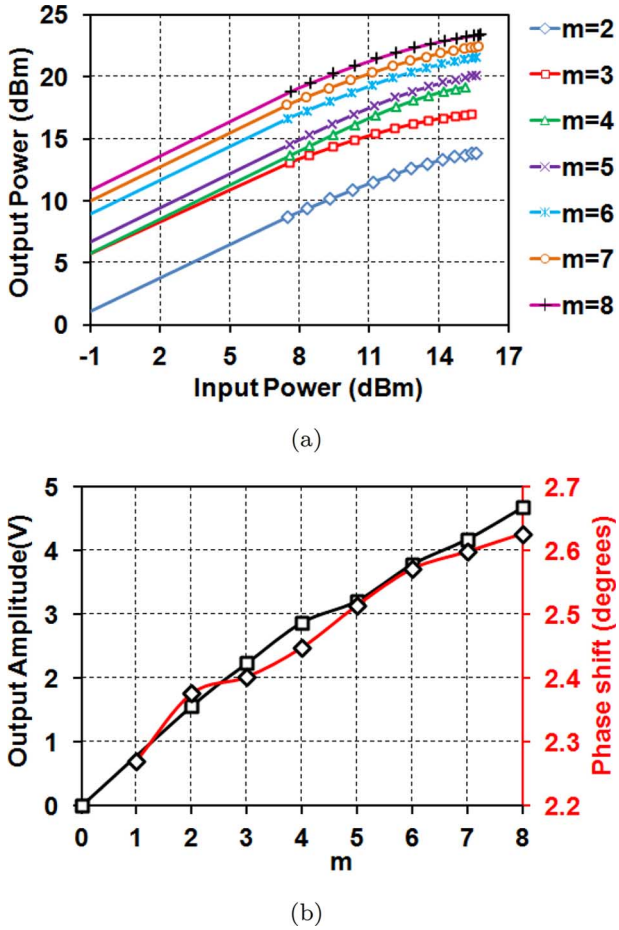


Fig. 20. (a) Measured output power versus input power and (b) measured saturated output voltage and simulated phase shift for different digital control settings (i.e., different number of PAs on) at 42.5 GHz for the three-bit digital to mmWave PA array prototype.

must be equal. Consider the case of $m = 2$ when the j^{th} and k^{th} PA unit-cells are ON. The output currents of these unit-cells (input currents to the combiner) are

$$I_j = (y_{jj} + y_{jk})V_s + aV_{n+1} \tag{16}$$

$$I_k = (y_{kk} + y_{kj})V_s + aV_{n+1}. \tag{17}$$

Since we desire $I_j = I_k$ and $y_{jk} = y_{kj}$ from reciprocity,

$$y_{jj} = y_{kk} = b \text{ where } j \neq k \text{ and } j, k \in 1, 2, \ldots n. \tag{18}$$

Now consider $m = 3$ when the j^{th}, k^{th} and l^{th} PA unit-cells are ON. The output currents of these unit-cells are

$$I_j = (b + y_{jk} + y_{jl})V_s + aV_{n+1}, \tag{19}$$

$$I_k = (y_{kj} + b + y_{kl})V_s + aV_{n+1}, \tag{20}$$

$$I_l = (y_{lj} + y_{lk} + b)V_s + aV_{n+1}. \tag{21}$$

Imposing the $I_j = I_k$ condition yields the following:

$$(b + y_{jk} + y_{jl})V_s + aV_{n+1} = (y_{kj} + b + y_{kl})V_s + aV_{n+1} \tag{22}$$

$$\Rightarrow y_{jl} = y_{kl} = c \quad \text{where } j \neq k \neq l \text{ and } j, k, l \in 1, 2, \ldots n. \tag{23}$$

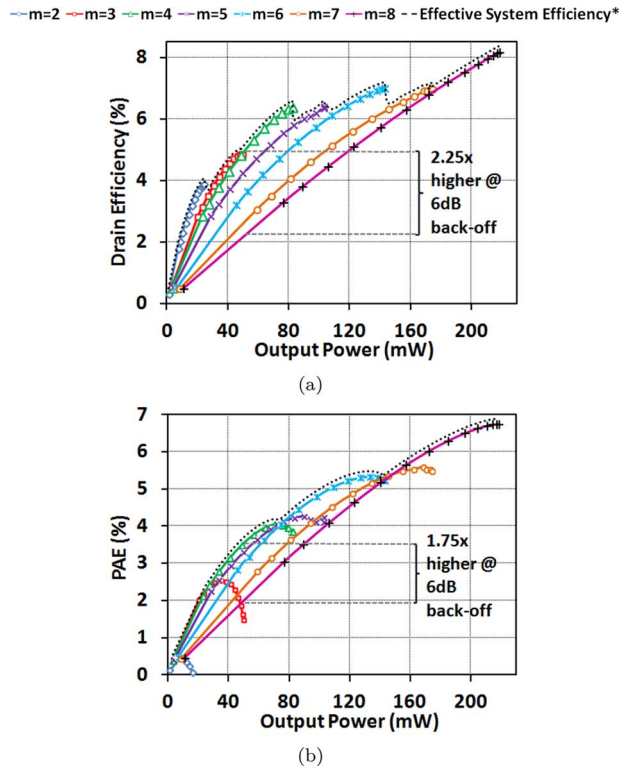


Fig. 21. (a) Drain Efficiency vs. P_{out} and (b) PAE vs. P_{out} for different digital control settings (i.e., different ms) at 42.5 GHz for the three-bit digital to mmWave PA array prototype. *Curves are slightly offset for clarity.

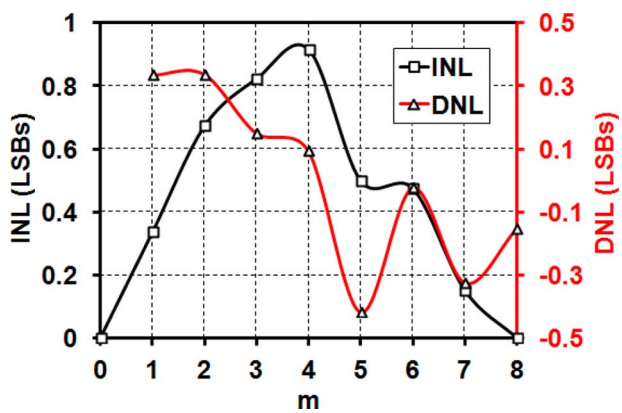
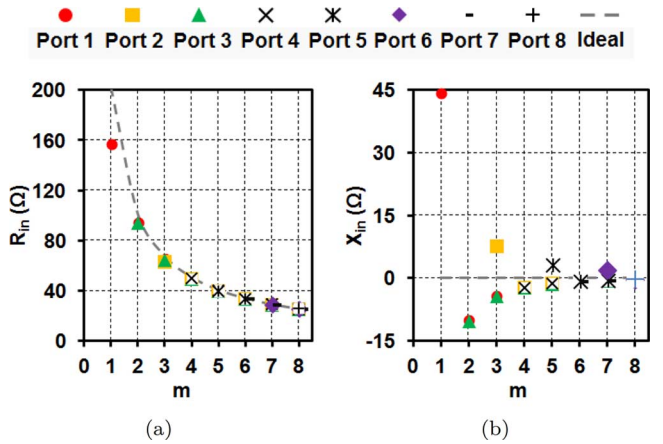


Fig. 22. Measured DNL and INL of the three-bit digital to mmWave PA array prototype at 42.5 GHz.

From (15), (18), and (23) the general Y-parameter matrix structure for an n-way passive, reciprocal combiner along with the source impedances of the PA unit-cells that satisfies linearity with m as well as equal load impedance seen by all ON unit-cells for each m is the following:

$$Y = \left[\begin{array}{ccccc|c} b & & & & & a \\ & b & & \mathbf{C} & & a \\ & & b & & & a \\ & \mathbf{C} & & \ddots & & \vdots \\ & & & & b & a \\ \hline a & a & a & \cdots & a & y_{(n+1)(n+1)} \end{array}\right]. \tag{24}$$



(a) (b)

Fig. 23. (a) Series input resistance and (b) reactance across m of the EM simulated eight-way combiner seen by each ON PA unit-cell in the three-bit digital to mmWave PA array prototype.

The Y-parameters of an ideal n-way quarter-wave lumped combiner at the operating frequency ω_0 driven by PA unit-cells with equal ON and OFF output impedances (Z_s) has this matrix structure, with $a = -1/jZ_0$, $b = 0$, $c = 0$ and $y_{(n+1)(n+1)} = nZ_s/Z_0^2$.

The eight lumped quarter-wave sections in the combiners used in the two prototypes are joined pairwise and each pair is connected to the output pad by means of an intermediary microstrip. Care must be taken to ensure that these routing lines are as short as possible to minimize the impedance transformation that they perform and the resulting asymmetry in the ON PA unit-cell load impedances for each m. For the combiner used in the three-bit digital to mmWave PA array prototype, from simulations, when all unit-cells are ON, each of the four aforementioned microstrip lines transforms a $4 \times 50\ \Omega$ load in parallel with 30 fF/4 pad capacitance to $167.25\ \Omega \| 37.8$ fF. Hence, each lumped quarter-wave section sees $334.5\ \Omega \| 18.9$ fF instead of an ideal value of 400 Ω. The input impedance of the EM simulated combiner used in the three-bit digital to mmWave PA array prototype seen by each ON PA unit-cell across m is very close to the ideal variation and the difference in the impedance between various ON ports is negligibly small as shown in Fig. 23(a) and (b). This indicates that the connecting lines used in this design do not violate the symmetry dictated by (23) to a large extent since their lengths are minimized and their characteristic impedances optimized to minimize their effect. Such optimization is not possible in the zero-degree combiner since all the connecting lines play a vital role in the impedance transformation being performed.

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