A Silicon-based, All-Passive, 60GHz, 4-Element, Phased-Array Beamformer Featuring a Differential, Reflection-Type Phase Shifter

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Abstract—*This paper presents an all-passive, 4-element, phased-array beamformer based on a differential, reflection-type phase shifter (RTPS) operating in the 60GHz band. The RTPS consists of a differential, vertically-coupled, coupled-line hybrid and variable, parallel-LC, resonant, reflective loads, both of which enable low-loss millimeter-wave operation. The design considerations for a silicon-based implementation of all the beamformer elements are discussed in detail. In particular, the influence of the different RTPS components on its insertion loss is analyzed. The beamformer IC and a breakout of the RTPS are implemented using CMOS-only features of IBM's 8HP 0.13μm SiGe BiCMOS process, and employ areas of 2.1mm^2 and 0.33mm^2, respectively, without probe pads. Differential s-parameter measurements at 60GHz show a phase-shift range greater than 150^o, insertion losses of 4-6.2dB in the RTPS and 14-16dB in the beamformer, and an isolation better than 35dB between adjacent beamformer channels. Measurements across temperature and process variations are also presented.*

1. Introduction

The 60GHz Industrial, Scientific and Medical (ISM) frequency band has aroused tremendous interest in the recent past due to the large available bandwidth that may be exploited for Gb/s wireless communications [1]-[4]. Beamforming is expected to be a critical feature in 60GHz transceivers for three main reasons. Firstly, beam steering allows to establish alternate multipath links when the line-of-sight (LoS) link is obstructed. Secondly, the link-budget requirements are difficult to meet, especially in CMOS implementations that achieve comparatively lower transmit-power levels. Finally, the directionality of the link mitigates the effect of interferences that result from undesired multipath.

Phased arrays, also known as electronically-steered arrays (ESAs), have been investigated for many decades, mainly for military and space applications [5]. On the other hand, silicon-integrated phased-arrays and beamformers started to emerge only the in last few years and present a different set of challenges and opporunities. For instance, a silicon implementation imposes design limitations to passive components due to metallization design rules, as well as performance limitations due to substrate and conductor losses. Nevertheless, the economics of silicon will benefit comercial

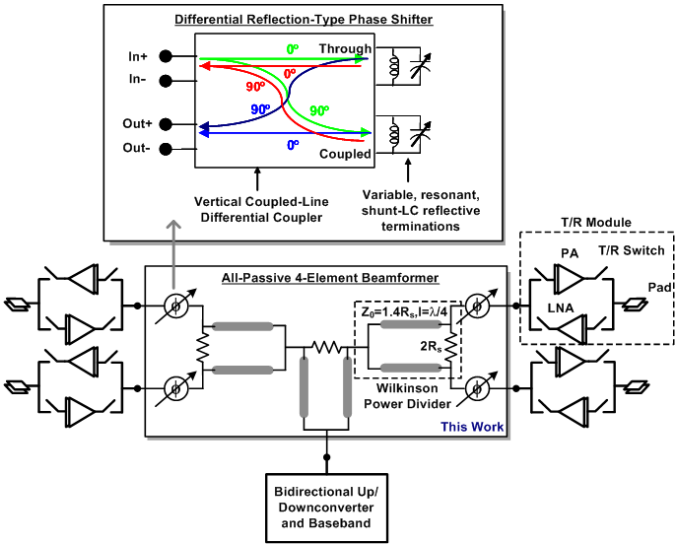

Fig. 1. A 60GHz phased-array transceiver architecture based on the proposed, bidirectional, phased-array beamformer, and the proposed differential RTPS

applications of integrated beamforming solutions. The first integrated millimeter-wave phased arrays were meant for radar applications [6]-[8] and silicon-based beamforming solutions for 60GHz wireless connectivity applications have started to emerge rapidly. RF-path phase shift [9]-[11], LO-path phase shift [12], and IF-path phase shift [13] architectures have been explored. Moreover, recent results show that the package-level integration of individual silicon beamforming modules with small number of elements is a feasible alternative for modular and low-cost 60GHz beam-steered solutions [14].

This work addresses the challenges of a millimiter-wave, RF-path, phased-array implementation in silicon and presents a 4-element beamformer operating in the 60GHz band. Its all-passive nature is useful for high-dynamic-range spatial-interference cancellation in phased-array receivers. In addition, the all-passive nature also results in bi-directionality, which renders the beamformer suitable for transceiver architectures that share the beamformer across transmit and receive sections (Fig. 1). The beamformer features a differential, reflection-type phase shifter (RTPS) and differential, Wilkinson power combiners. The RTPS consists of a differential, vertically-coupled, coupled-line hybrid and variable, parallel-LC, resonant, reflective loads, both of which enable low-loss millimeter-wave

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operation. Design considerations for the proposed coupler and loads are discussed, including an analysis of their influence on the insertion loss. The presented design guidelines are well supported by measurements of a prototype phase shifter and beamformer.

The paper is organized as follows. Section II presents the design details of the RTPS and beamformer. Section III presents the measurement results, and Section IV concludes the paper.

2. All-Passive Beamformer Design

1. Architecture

Fig. 1 depicts the architecture of the 60GHz, all-passive, 4-element, phased-array beamformer. All blocks are differential implementations. Each channel employs reflection-type phase shifters [15] that can provide 180^o of variable phase shift. Flipping of the differential signals results in a fixed 180^o degree shift that enables 360^o of variable phase shift and complete beam-steering coverage. This sign inversion can be achieved in the front-end LNA/PA of each channel [7]. The power combining of the 4 channels of the beamformer is achieved through a cascade of two stages of 2:1 Wilkinson combiners [16].

An RTPS, depicted in Fig. 1, consists of a -3dB, quadrature hybrid with the *through* and *coupled* ports terminated with variable, reflective (i.e., purely reactive) loads and the *input* and *isolated* ports as the bidirectional input/output ports. The phase shift of an RTPS is given by

$$\angle S_{21} = -90^o - 2\tan^{-1}\frac{X}{R_s}, \quad (1)$$

where X is the reactance of the reflective loads and R_s is the reference impedance. The loss of the RTPS is given by

$$|S_{21}| = 2|S_{hyb}| + |\Gamma|, \quad (2)$$

where $|S_{hyb}|$ is the loss of the hybrid in dB (not counting the -3dB power split) from the *input/isolated* ports to the *through/coupled* ports assuming a symmetric response, and $|\Gamma|$ is the reflection coefficient of the non-ideal (i.e., lossy) load reactance.

2. Coupled-Line Hybrid Design

Fig. 2(a) depicts the schematic diagram of a -3dB, quadrature, coupled-line hybrid. Two coupled lines function as a -3dB quadrature hybrid if the length of the lines is a quarter-wavelength in both even and odd modes, and the impedances of the modes are given by the expressions in Fig. 2(a). c is the coupling factor of the hybrid, and is 0.7 for -3dB coupling. For -3dB coupling and a differential reference impedance of 100Ω, $Z_{0,even}$ and $Z_{0,dd}$ are 240Ω and 42Ω respectively.

Coupled transmission lines may be implemented in two ways - edge coupling or vertical/broadside coupling. In [17], the authors have reported quadrature Lange couplers operating at 60GHz and 77GHz using edge-coupled microstrips in the Back-End-Of-the-Line (BEOL) of IBM's 8HP process. However, a challenge with edge-coupled lines is the simultaneous

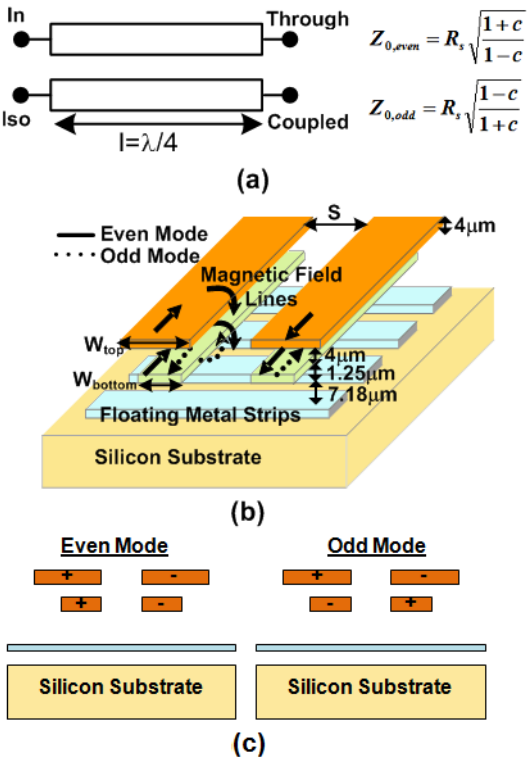

Fig. 2. (a) Circuit diagram of a -3dB, quadrature, coupled-line hybrid. c=0.7 for -3dB coupling.(b) An integrated implementation using vertically-coupled, coplanar striplines with shielding metal strips. The Back-End-Of-the-Line (BEOL) dimensions correspond to IBM's 8HP 0.13μm BiCMOS process. (c) Current polarities in the even and odd modes are depicted on a cross-sectional view for clarity.

achievement of high coupling values (e.g., -3dB coupling) and the required even- and odd-mode characteristic impedances for satisfactory input and output matching in the presence of BEOL design rules [17], [18]. As a result, in [17], the authors abandon the thick, top metal layer for the thinner, penultimate layer at the expense of insertion loss. Secondly, differential quadrature couplers are difficult to implement using planar, edge-coupled transmission lines.

In this paper, an asymmetric, vertically-coupled, coplanar-stripline (CPS) structure is employed (Fig. 2(b)). Vertically-coupled CPS lines are implemented in the top and penultimate layers of IBM8HP's BEOL, called AM and LY respectively. Vertically-coupled lines have been investigated in the past [18]-[21], and analytical results for vertically-coupled CPS lines have been derived recently [21]. However, the implementation of vertically-coupled transmission lines in a silicon-based process results in unique design challenges. The presence of a conductive substrate requires the implementation of floating metal strips underneath the coupled lines in the first metal layer to isolate the lines from the substrate and reduce loss [22]. These shielding strips result in asymmetry between the top and bottom lines. Therefore, in this paper, an asymmetric structure is proposed with unequal widths for the top and bottom CPS lines.

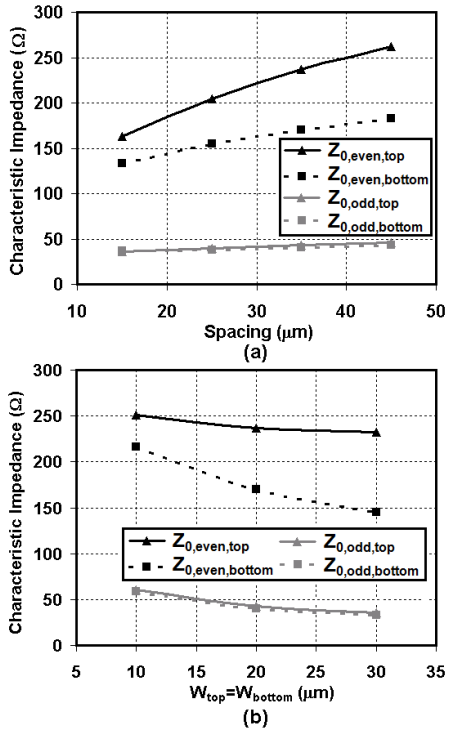

Fig. 3. Simulated characteristic impedances of the top (AM) and bottom (LY) coplanar striplines in the even and odd modes. (a) W_{top}=W_{bottom}=20μm, and the spacing S is varied. (b) S=35μm and $W_{top} = W_{bottom}$ is varied.

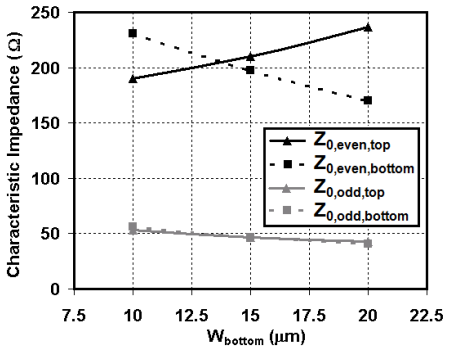

Fig. 4. Simulated characteristic impedances of the top (AM) and bottom (LY) coplanar striplines in the even and odd modes. $W_{top} = 20\mu m, S = 35\mu m$ and W_{bottom} is varied.

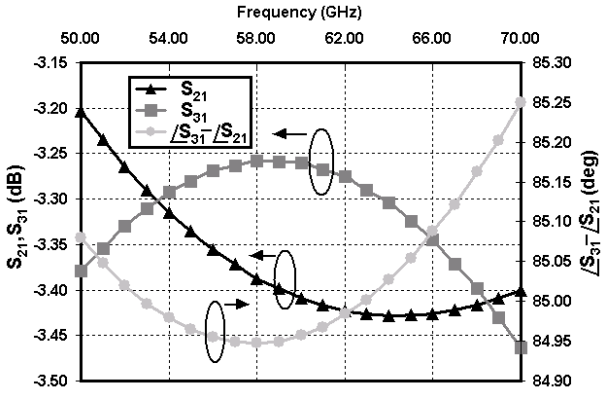

Fig. 5. Simulated insertion losses from the *input* port (#1) to the *through* (#2) and *coupled* (#3) ports, and phase difference between the *through* and *coupled* ports.

Fig. 3 depicts the characteristic impedances of the top (AM) and bottom (LY) CPS lines in the even and odd modes as the widths and spacings of the two CPS lines are varied. Current polarities in the even and odd modes are depicted in Figs. 2(b) and 2(c). The characteristic impedances are obtained through electromagnetic simulations in IE3D, a Method-of-Moments-based field solver [23]. In the even mode, the currents in both CPS lines are parallel, and the magnetic fields in the center of the structure add constructively, boosting the inductance per unit length. The vertical capacitance between the top and bottom CPS lines is virtually non-existent as the voltages along the lines are identical. As a result, a large even-mode characteristic impedance is seen. Furthermore, this characteristic impedance increases with an increase in the spacing due to an increase in the inductance per unit length (Fig. 3(a)), but is only a weak function of the conductor width (Fig. 3(b)). However, the even-mode characteristic impedance of the bottom CPS does show more dependence on the width due to capacitive parasitics to the floating strips. Consequently, the even-mode impedance of the bottom CPS is lower than that of the top CPS.

In the odd mode, the magnetic fields in the center cancel. As a result, the magnetic field is mainly confined between the top and bottom CPS lines, where their contributions add constructively. There is also a significant parallel-plate capacitance between the top and bottom CPS lines. In effect, the coupled CPS lines behave as two differential parallel-plate waveguides. Due to the small inductance and the large parallel-plate capacitance, the characteristic impedances of the two CPS lines in the odd mode are lower. Furthermore, they show a strong, decreasing dependence on the conductor width (Fig. 3(a)) and only a weak dependence on the spacing (Fig. 3(b)). The simulated attenuation constants of the coupled CPS lines in the even and odd modes are 0.4 and 1.1 dB/mm, respectively, for a spacing of S=35μm. The attenuation constant is higher in the odd mode. This can be attributed to current crowding at the bottom of the top conductor and the top of the bottom conductor due to the proximity effect.

Since the even-mode impedances are largely a function of the spacing and the odd-mode impedances are largely a function of the width, they can be set to their desired values independently. Even and odd mode impedances of 240Ω and 42Ω respectively, dictate width and spacing of approximately 20μm and 35μm, respectively. A challenge that remains is the lower impedance of the bottom (LY) CPS in the even-mode. To equalize the even-mode impedances, an asymmetric, vertically-coupled, CPS structure is employed with unequal widths for the top and bottom CPS lines. Fig. 4 depicts the even- and odd-mode impedances as W_{bottom} is varied. In the

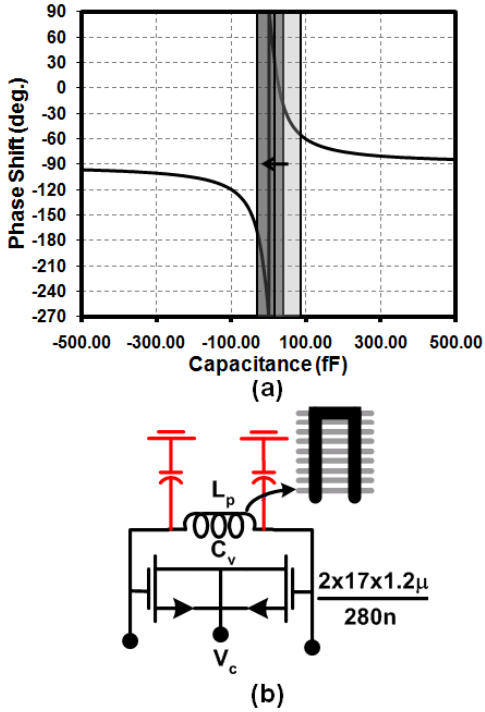

Fig. 6. (a) Theoretical RTPS phase shift as a function of the effective capacitance of the reflective terminations from (1). (b) Variable, resonant, shunt-LC reflective termination.

even mode, as the width of the bottom conductor is reduced, the characteristic impedance of the bottom CPS increases due to a reduced capacitance per unit length. The characteristic impedance of the top CPS decreases as the regions that extend beyond the bottom CPS experience capacitive parasitics to the substrate. A width of 15μm for the bottom CPS results in equal even- and odd-mode impedances of approximately 200Ω and 46Ω, respectively, which are close to the desired values.

Approximately 500μm of length is required to achieve a quarter-wavelength in the even and odd modes. The coupled CPS lines are bent to conserve chip area. Fig. 5 shows the simulated insertion losses from the input port to the through and coupled ports, as well as the phase difference between the through and coupled ports. The phase difference is close to 90^o, and the simulated insertion losses are below 3.5dB between 50GHz and 70GHz.

3. Tunable Reflective Terminations

The variable reactance required for the tunable, reflective terminations is commonly implemented using varactors. Fig. 6(a) depicts the phase shift achieved by the RTPS from (1) as a function of the effective capacitance of the reflective termination, assuming a reference impedance of 100Ω. It is seen that maximum phase variation occurs around an effective capacitance of 0. If an inductor is shunted across the varactor (Fig. 6(b)), the effective capacitance is given by

$$C_{eff} = C_v - \frac{1}{\omega^2 L_p}, \tag{3}$$

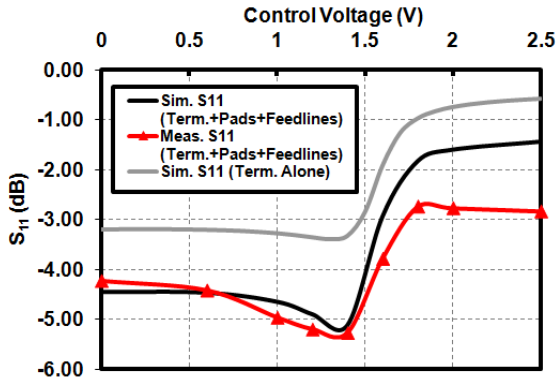

Fig. 7. Simulated and measured reflection coefficients of a breakout of the reflective termination as a function of the varactor control voltage.

where C_{eff} is the effective capacitance, C_v is the capacitance of the varactor, ω is the frequency of operation and L_p is the shunt inductance. As can be seen in Fig. 6(a), if L_p is chosen to resonate with the mid-value of the varactor's range, C_{eff} falls in the region of maximum phase change.

A total effective-capacitance variation of 50fF centered around 0 is required for 180^o phase variation. The usage of varactors with high tuning ratio enables the usage of small varactors to achieve this variation. For example, a tuning ratio of 3.5 enables the usage of a varactor with 20-70fF capacitance range, while a tuning ratio of 2 needs the deployment of a 50-100fF varactor. The benefit of using small varactors is that the shunt inductance needed to resonate with the mid-range capacitance is higher. As a result, for a constant inductor quality factor (Q), the loss that results from the parallel resistance of the inductor is lowered. However, varactors with high tuning range require the use of large channel length, which in turn decreases Q and increases loss. As a result, an optimal point exists in the design of the reflective termination.

At design time, accurate varactor models that realistically reflect the varactor Q did not exist in the process design kit. For the reflective termination, a 20-70fF varactor was employed using MOS varactors with the dimensions given in Fig. 6(b). The 156pH inductor needed to resonate with the mid-range capacitance was implemented as a short-circuit-terminated CPS. The CPS conductors are implemented in the top metal layer with floating strips in the first metal layer. Fig. 7 summarizes the simulated and measured reflection coefficients of a breakout of the reflective termination, along with test pads and feed lines. Since accurate varactor models were not available, a parasitic series gate resistance of 2.7Ω was added at design time to each varactor. The addition of this series resistance results in quality factors of 9 and 33 in the on and off states respectively. The resultant simulations agree reasonably with the measurements (Fig. 7). It should be noted that in the off state, the measured reflection coefficient exhibits 1.5dB more loss than the simulations. This indicates that a constant series gate resistance that is independent of the control voltage is insufficient to model the loss of the varactors

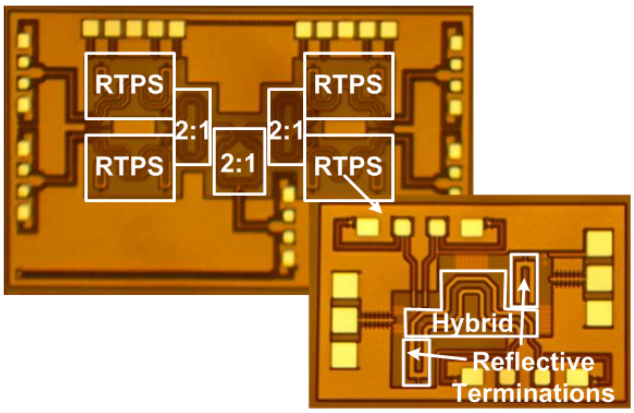

Fig. 8. Chip microphotograph of the 4-element beamformer and the RTPS breakout.

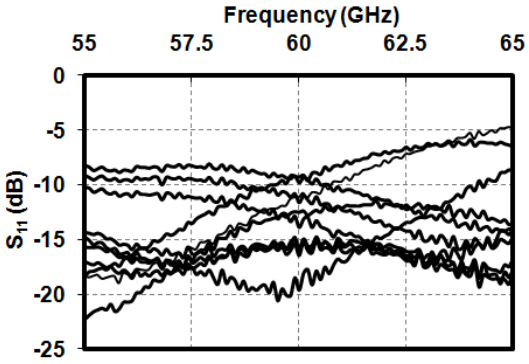

Fig. 9. Measured input reflection coefficient of the RTPS for different varactor control settings ranging from 0V to 2.5V.

at 60GHz, especially in the off state. The on-state quality factor of 9 is roughly consistent with previously reported numbers at 60GHz in a 0.13μm CMOS process [24]. In the absence of the pads and feed-lines, the reflective termination, including the added parasitic series gate resistance, adds a simulated 0.5-3.5dB of loss to the RTPS at 60GHz (Fig. 7).

Higher-order reflective terminations for silicon-based reflection-type phase shifters have been investigated in the past [25]-[27], [30]. These higher-order terminations have primarily relied on LC circuits in series or π configurations, or combinations of the two. The shunt LC termination is more suitable for millimeter-wave realizations as the parasitic capacitances of the inductor can be readily absorbed into the design by modifying the inductance value.

The prototypes described in this paper employ analog varactor control voltages. When deployed in a practical system, digital-to-analog converters (DACs) will be required for each RTPS to support digital phase-control bits. In Section 3-A, the number of practical phase-control bits that can be supported is determined based on across-wafer process-variation measurements. Analog varactors are sensitive to noise on the bias lines, which translates to phase noise at the output of the phase shifter. During practical deployment, the varactors in Fig. 6(b) can decomposed into binary-weighted, DAC-like varactor banks, with each varactor driven by a digital control bit that always places the varactor at the on- or off-edge of its tuning curve, where there is no sensitivity to bias noise.

4. *Wilkinson Power Combiners*

The power combining of the 4 channels of the beamformer is achieved through a cascade of two stages of 2:1, differential, Wilkinson power combiners. Each Wilkinson power combiner consists of two, parallel, quarter-wavelength transmission lines with characteristic impedances of $1.4R_s$ and an isolation resistor of value $2R_s$ (Fig. 1). The quarter-wavelength transmission lines are implemented using a CPS in the top metal layer with a width of 15μm, spacing of 35μm, and floating metal strips in the first metal layer, achieving the requisite differential characteristic impedance of approximately 1.4×100Ω=140Ω. The required length of each CPS is approximately 500μm, and they are bent to conserve chip area. The bent dimensions are 515μm×328μm. The simulated, single-channel insertion loss of the 4-channel power combiner is approximately 1dB at 60GHz, aside from the ideal 6dB power-split.

3. Measurement Results

The 4-element beamformer and RTPS breakouts are implemented using IBM's 0.13μm SiGe 8HP BiCMOS process. Fig. 8 shows the chip microphotographs. The beamformer and RTPS breakouts occupy areas of 2.1mm^2 and 0.33mm^2, respectively, not including probe pads. All of the measurement results presented in this section are differential and were obtained through full, 4-port, S-parameter measurements with probe-based SOLT calibration.

1. *RTPS Measurement Results*

Figs. 9, 10(a) and 10(b) depict the input reflection coefficient, insertion loss and phase response of the RTPS across frequency for different varactor control voltage (V_c) values respectively. Fig. 10(c) depicts the measured insertion phase at 60GHz across V_c values. Measurements on a breakout of the input and output pads and the feed lines reveal an insertion loss of approximately 3dB at the frequency range of interest. The measured insertion loss of the input and output pads and feed lines are subtracted to yield the insertion loss of the RTPS alone in Fig. 10(a). It should be noted that the pads employ shunt transmission-line stubs to resonate out the pad capacitance [31]. As a result, the input and output pads and feedlines are *electrically transparent* over the considered bandwidth [31], enabling a de-embedding of their insertion loss through simple subtraction. After de-embedding, the RTPS insertion loss is approximately 4-6.2dB at 60GHz. The simulated 60GHz insertion loss, without pads and feed lines, ranges from 2-5dB, as shown in Fig. 10(a). For a V_c value of 0V, when the varactor is in the on-state, the simulated and measured insertion losses agree within approximately 1dB. However, for a V_c value of 2.5V, the discrepancy is about 2dB. This increased discrepancy agrees with the observation made in Section II-C that the constant parasitic gate resistance of

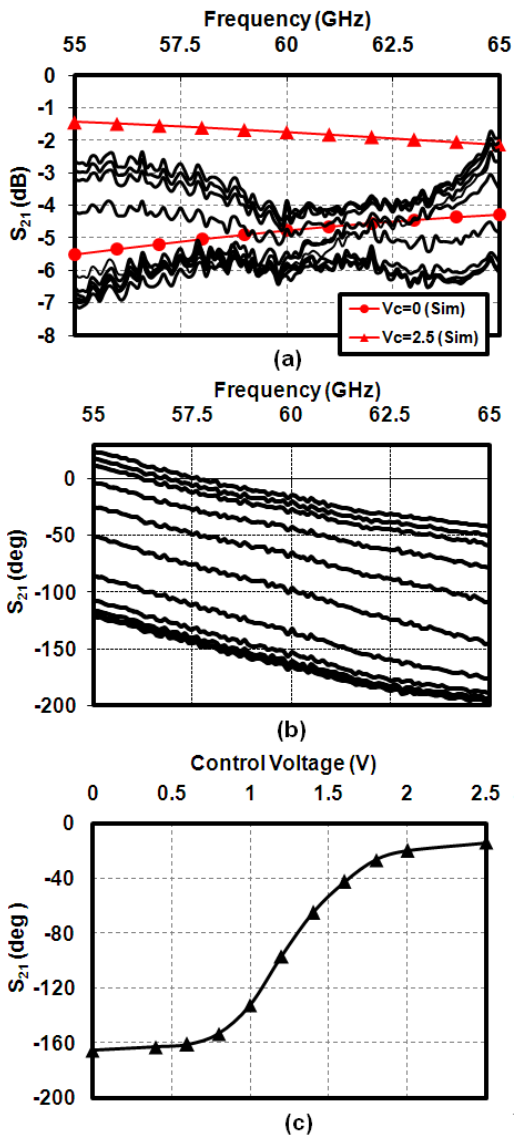

Fig. 10. (a) Measured and simulated insertion loss of the RTPS across frequency for different varactor control settings ranging from 0V to 2.5V. Note that the insertion loss of the pads and feed lines, measured from a separate breakout, have been subtracted out to yield the insertion loss of the RTPS alone. (b) Measured insertion phase of the RTPS across frequency for different varactor control settings ranging from 0V to 2.5V. (c) Measured insertion phase at 60GHz across varactor control settings.

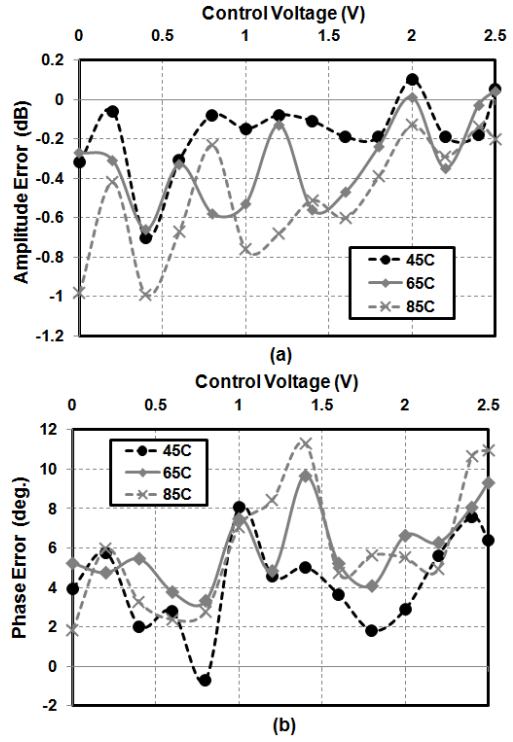

Fig. 11. Measured RTPS (a) amplitude error and (b) phase error at 60GHz across different varactor control settings for different temperatures. The errors are referenced to the performance at 25^{o}C.

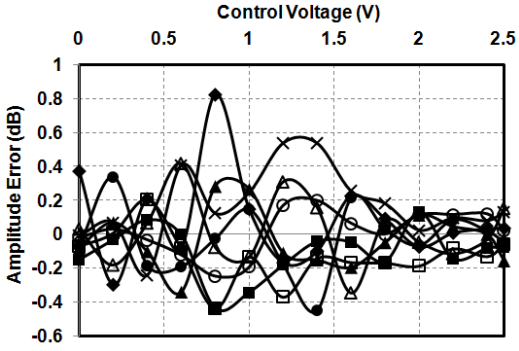

Fig. 12. Measured RTPS amplitude error at 60GHz across different varactor control settings for 8 different samples on the same wafer. The amplitude error is computed as the error between the insertion loss of each sample and the mean across all samples.

2.7 Ω that was added in simulation underestimates the loss of the varactor in the off-state.

The simulated phase-shift range at 60GHz is 177^o, while the measured range is 151^o. This reduction of about 15% is attributed to unaccounted parasitic capacitance in the varactor connections. Nevertheless, the phase-shift-range changes by less than 8^o across the 55 to 65GHz frequency band, which is in good agreement with simulations.

Fig. 11 depicts the measured RTPS amplitude and phase errors at 60GHz across varactor control settings at different temperatures. The errors are referenced to the performance at 25^{o}C. The RTPS is seen to be robust to temparature variations. The maximum change in insertion phase between operating temperatures of 25^{o}C and 85^{o}C happens at a control voltage of 1.4V, and is equal to 11.3^o. Fig. 12 depicts the measured RTPS amplitude error at 60GHz across different varactor settings for 8 different samples on the same wafer. The amplitude error is computed as the error between the insertion loss of each sample and the mean across all samples. Fig. 13 depicts the measured RTPS phase-shift error of the 8 samples at 60GHz for different varactor settings, with the error once again referenced to the mean across the 8 samples.

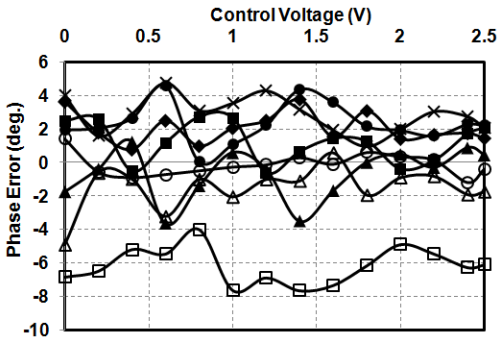

Fig. 13. Measured RTPS phase-shift error at 60GHz across different varactor control settings for 8 different samples on the same wafer. The phase error is computed in relation to the mean phase across the samples.

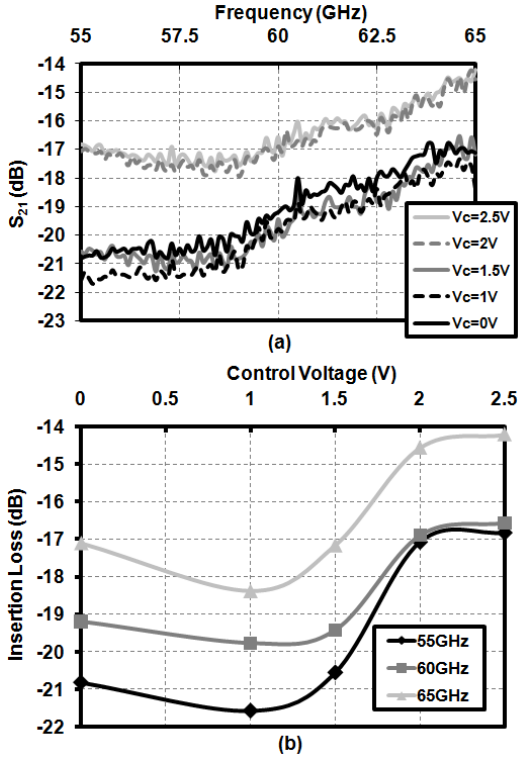

Fig. 14. Insertion loss of a single beamformer channel (a) versus frequency for different control voltage values (b) versus control voltage for the same channel for different frequencies. No de-embedding of pads and feed lines is performed.

The maximum amplitude and phase-shift errors are 0.8dB and -8^o, respectively, indicating that the RTPS is robust to across-wafer process variations. The worst-case standard deviation of the phase-shift for the 8 samples is approximately 4^o. This indicates that the RTPS can be controlled by a DAC with 4-5 bits of resolution for the standard deviation of quantization phase error to be equal to the standard deviation of phase error due to across-wafer process variations [1].

[1]This assumes that quantization noise is uniformly distributed between $\pm\frac{LSB}{2}$, where LSB is the Least Significant Bit.

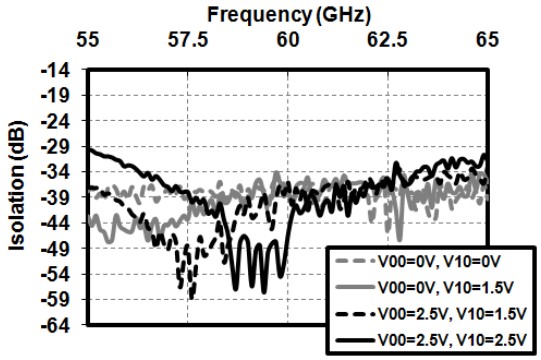

Fig. 15. Isolation between adjacent beamformer channels (designated 00 and 10) for different control voltage values.

Table I contains a survey of reported silicon-based phase shifters, and compares them to this work.

2. *4-Element Beamformer Measurement Results*

The insertion loss and phase from the input to the outputs of the 4 channels of the beamformer are first measured individually. When this measurement is performed for a channel, all other channels are left un-terminated due to wafer-probing restrictions. Simulations verify that the insertion loss and phase between the input and the channel of interest do not change significantly if the other channels are left un-terminated due to the inherent architectural isolation between the channels and the substantial insertion loss between the input and each output. As expected, the phase-shift range on each channel is the same as measured for the RTPS. Fig. 14(a) shows the insertion loss for a single beamformer channel across frequency for different control voltage values. Fig. 14(b) shows the insertion loss of the same channel versus control voltage for different frequencies. Since the feedlines of the beamformer are slightly different from those in the RTPS and a separate breakout of the beamformer feedlines was not available, no de-embedding of pads and feed lines is performed. Aside from the ideal 6dB power split across the 4 channels and an assumed 3dB of loss in the feedlines, there is 7.5-10.5dB of loss from the input to each channel output at 60GHz. Hence, each Wilkinson power combiner adds approximately 2dB of loss at 60GHz.

The isolation between adjacent channels, with the input port and other channel outputs left un-terminated, is measured and displayed in Fig. 15 for different control-voltage values. It can be seen that the isolation is better than 35dB at 60GHz and 29dB in the 55-65GHz frequency range. The isolation quality may be attributed to the differential design, and the usage of shielding metal strips underneath the various transmission lines to isolate them from the substrate.

4. Summary and Conclusion

This work has presented a 60GHz beamformer design which is original in its combination of differential, silicon-based, and all-passive characteristics. In contrast to recently reported 60GHz RF-path beamforming solutions [9]-[10], which feature

TABLE I
SURVEY OF SILICON-BASED PHASE-SHIFTER DESIGNS.

Work	Architecture	Freq. (GHz)	Tech.	Loss (dB)	Phase Shift (^{o})	Area (mm^2)	Power (mW)
[25]	RTPS with active loads (Single-Ended)	2.4	0.18μm CMOS	4.6-11	105	2.5	1.8
[26]	RTPS with active circulator (Single-Ended)	2.4	0.18μm CMOS	0-5	120	0.36	111
[27]	RTPS (Single-Ended)	24	0.18μm CMOS	10.1-12.5	360	0.33	0
[28]	Switched π-networks (Single-ended)	34	0.13μm SiGe (CMOS-only)	11.5-13.7	360	0.12	0
[28]	Switched π-networks (Differential)	34	0.13μm SiGe (CMOS-only)	8.8-11.2	360	0.18	0
[29]	Varactor-loaded transmission line (Differential)	60	65nm CMOS	6.3-12.5	156	0.2	0
[30]	RTPS (Single-Ended)	60	0.13μm SiGe (CMOS-only)	4.2-7.5	180	0.18	0
[30]	Vector Interpolator (Differential)	60	0.13μm SiGe	2	360	0.64	32.4
This work	**RTPS (Differential)**	**60**	0.13μm SiGe (CMOS-only)	**4-6.2**	**156**	**0.33**	**0**

limited discrete phase states, the proposed beamformer offers continuous phase shift. A vertically coupled, coupled-line hybrid design compatible with a silicon-process BEOL has also been introduced. The differential RTPS employed in the beamformer, based on the proposed coupled-line hybrid, achieves state-of-the-art performance, showing comparable phase-shift range and lower insertion loss in comparison to other passive silicon-based implementations operating at 60GHz.

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