A 4-Channel 24-27 GHz UWB Phased Array Transmitter in 0.13μm CMOS for Vehicular Radar

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***Abstract*— The Variable-Phase Ring Oscillator (VPRO) and Phase-Locked Loop (PLL) architecture for integrated phased arrays enables the elimination of mixers, power splitters/combiners and phase shifters and hence allows for compact and power-efficient implementations. This paper extends the architecture to Ultra-wideband (UWB) applications through architectural and circuit innovations. The implementation of a wideband VPRO enables the generation of UWB signals through the PLL which are inherently phase-shifted to accomplish beam-steering. The VPRO operates at half of the desired frequency range, and a squarer is interposed between the VPRO and the power amplifier of each channel. This doubles the bandwidth and the inter-channel phase shift and enables the architecture to cover the $\pm 180^{o}$ phase-shift range required for full beam-steering coverage. In addition, a waveform-adaptive, tunable-narrowband design paradigm is introduced that greatly simplifies the design of UWB RF blocks. A fully-integrated, 4-channel, 24-27 GHz, phased-array transmitter, useful for vehicular radar applications, is implemented in 0.13μm CMOS to validate these claims.**

***Index Terms*— Phased arrays, radar, CMOS integrated circuits, power amplifiers.**

I. Introduction

Both FCC and ETSI have opened a large bandwidth around 24 GHz for use towards UWB vehicular radar applications. The deployment of a number of UWB radar sensors on the car perimeter, intended for driver assistance functions such as blind-spot detection, parking assistance and pre-crash detection, is envisioned by the automotive industry. Efforts have been made towards the integration of these sensors on SiGe processes [1], and CMOS is even more attractive from a cost perspective.

Spatial selectivity, specifically beam-steering, is important in vehicular radar as reflections from undesired directions are suppressed, thus reducing the rate of false alarms. Phased arrays are particularly attractive as they allow for electronic beam-steering, thus eliminating the need for moving mechanical fixtures. In addition, for transmitters, a phased-array architecture alleviates the power requirement of each channel.

The Variable Phase Ring Oscillator (VPRO) and Phase-Locked Loop (PLL) architecture for integrated phased arrays, first presented in [2], eliminates common phased-array building blocks such as mixers, power splitters/combiners and phase shifters, allowing for compact and low-power implementations. This paper extends the architecture to UWB applications through architectural and circuit innovations and presents the first CMOS UWB phased array transmitter in the K-band.

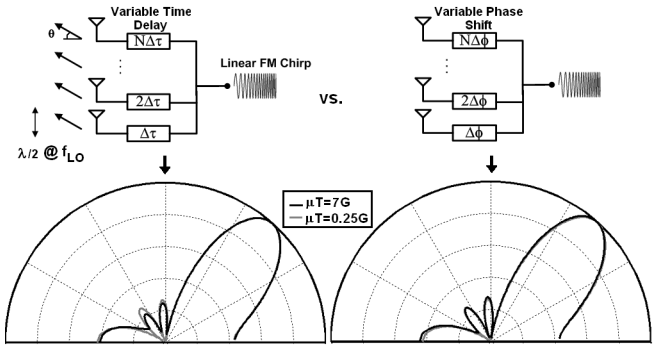

Fig. 1. Comparison of the spatial selectivity of timed and phased arrays for the linear FM chirp signal. Different signal bandwidths are considered.

II. Phased Arrays versus Timed Arrays

A phased array transmitter achieves spatial selectivity by imposing a successive time delay between the signals transmitted from the different channels. The transmitted signals add coherently only in the direction in which the successive time delay is compensated by the path delay of the signals in free space that results due to the spacing between the antennas. In narrowband phased arrays, the variable delay element that is required for each signal path can be approximated with a variable phase shifter. However, when the bandwidth of the signal is large, this approximation is no longer valid and a true-time-delay implementation is necessary [3]. Such implementations may be called *Timed Arrays*.

To examine the range of bandwidths in which the phased-array approximation is valid, consider the linear, frequency-modulated (FM) chirp signal that is commonly used in radar applications. The chirp has a frequency that increases linearly with time and a functional form given by $S_{chirp}(t) = \sin(2\pi f_{LO} t + \frac{1}{2}\mu t^2)$ for $|t| < \frac{T}{2}$ and 0 otherwise, where f_{LO} is the center frequency, T is the duration of the chirp pulse and μ is the rate of increase of the chirp frequency with time. μT represents the frequency range of the chirp and is closely related to the signal bandwidth. In radar applications, at the receiver side, the received signal is usually passed through a matched filter. Hence, to compute the spatial selectivity (or for

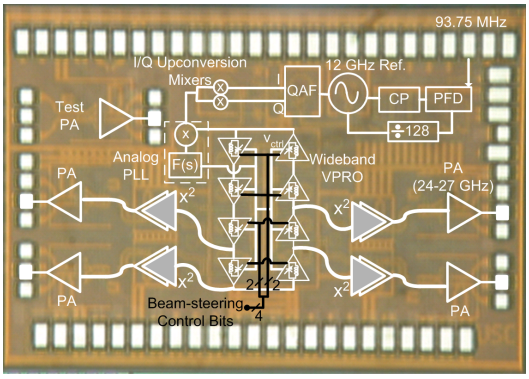

Fig. 2. Ultra-wideband VPRO-PLL transmitter phased array architecture and chip microphotograph.

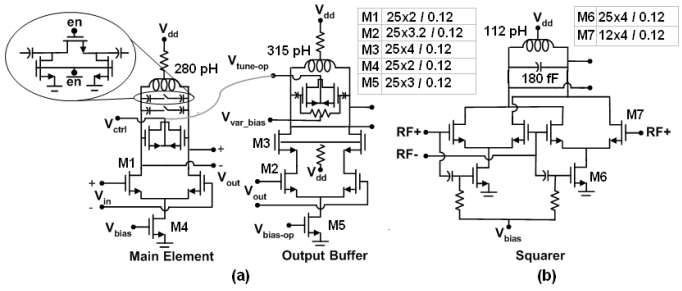

Fig. 3. Circuit diagram of (a) each element of wideband VPRO and (b) the squarer.

that matter, range resolution), the autocorrelation of the chirp, $R(t)$, is of interest.

Fig. 1 depicts phased- and timed-array transmitters based on the linear FM chirp signal. When true-time-delay blocks are used for each signal path, the received signal in a particular direction θ after the matched filter can be written as $S_{RX}(\theta,t) = \sum_{i=1}^{N} R\left(t - i\Delta\tau - \frac{(N-i)\sin\theta}{2f_{LO}}\right)$. Note that the antenna spacing is assumed to half-wavelength at f_{LO}. The array factor, representing the strength of the received signal in a particular direction, may then be defined as $AF(\theta) = \max_t S_{rx}(\theta,t)$.

Fig. 1 shows the array pattern for a timed-array on the left hand side for 45^o steering. f_{LO} =25.5 GHz, T=1 ns, and different bandwidths are considered. On the right, the array pattern is shown when wideband variable phase-shifters are used in place of the true-time-delay blocks. It is seen that for the FCC vehicular radar band (7 GHz around 25.5 GHz), a phased-array implementation is adequate and no deterioration in the array pattern is seen. Indeed, it is the signal's *fractional bandwidth*, defined as the ratio of the bandwidth to the center frequency, that determines the need for timed arrays; for instance, a 7 GHz signal from 3 to 10 GHz would require true-time-delay blocks due to its high fractional bandwidth.

III. The UWB VPRO-PLL Transmitter Architecture

Fig. 2 depicts the UWB VPRO-PLL integrated phased array architecture. The reference path consists of an on-chip 12 GHz reference oscillator which is locked to an off-chip, low-frequency reference in a divide-by-128 digital PLL. I and Q components of this reference are generated by a Quadrature all-pass filter (QAF) and are mixed with baseband I and Q inputs to generate the modulated reference signal. The wideband VPRO, which generates the phase-shifted signals for each antenna path, is locked to this modulated UWB reference signal through an analog, high-frequency PLL with sufficient loop bandwidth for the VPRO to track the UWB reference. Since the VPRO functions at half of the desired output frequency range, a squarer, designed as a self-mixer (Fig. 3(b)), is interposed between each VPRO output and the corresponding power amplifier (PA). This section provides additional details with respect to the design of these blocks.

A. Wideband VPRO

The VPRO, first introduced in [2], is a tuned ring oscillator with a phase-shifter introduced into the loop. Since the total phase shift in the loop must add up to 0^o, the phase-shifter's extra phase shift must be compensated by the tuned ring elements. The VPRO oscillates off the center-frequency of the tuned loads so that each tuned element sustains a phase shift across itself to compensate for the extra phase-shifter. Thus, an electronically-controllable phase progression is set up across the VPRO nodes, which is the requirement for beam-steering.

An LC tuned load can sustain a phase shift that ranges from -90^o to +90^o. However, in a tuned ring oscillator, this range would be practically limited to -60^o to +60^o as large phase shifts reduce the impedance of each tuned load and hence deteriorate start-up. The VPRO is therefore operated at half of the desired output frequency range; doubling the frequency through squaring also doubles the inter-element phase shift. If each tuned load provides -45^o to +45^o of phase shift, squaring increases the range to -90^o to +90^o. A simple sign-inversion of the differential signals, accomplished in the PAs, increases the range further to -180^o to +180^o, the complete range required for beam-steering.

Fig. 2 contains the block diagram of the wideband VPRO and Fig. 3(a) depicts the circuit diagram of each element. For symmetry purposes, the extra phase-shifter is implemented as 4 additional tuned stages. Each stage is equipped with 2-bit, binary-weighted switched capacitors so that the top- and bottom-four elements may be detuned to accomplish phase-shifting and hence beam-steering. This, coupled with the 1-bit sign inversion capability incorporated in the PAs, allows the 4-channel array to achieve 3-bits of beam-steering resolution. Each tuned element is also equipped with varactors for PLL frequency control, with the size of the varactors chosen to maximize the Quality Factor (Q) and the $\frac{C_{max}}{C_{min}}$ capacitor tuning ratio [4]. Although the VPRO needs 1.5 GHz of tuning

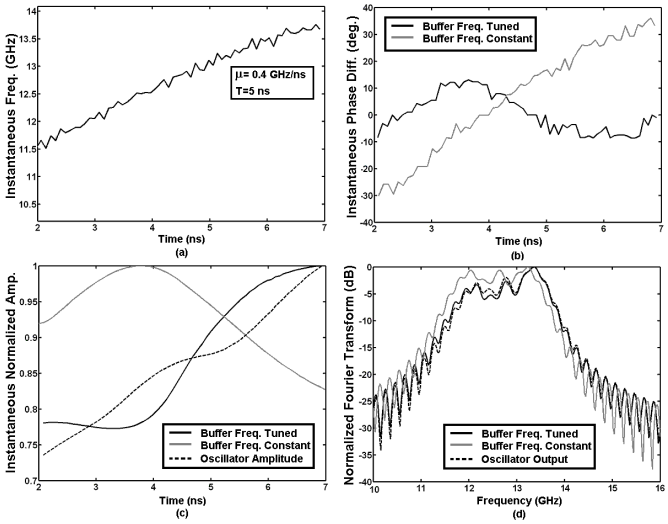

Fig. 4. SpectreRF simulation of the VPRO and its output buffers when the control voltage is ramped up linearly with time to generate a chirp. The (a) instantaneous frequency, (b) instantaneous phase difference between the VPRO node outputs and the buffer outputs, (c) instantaneous amplitude of the VPRO node outputs and buffer outputs and (d) frequency response of the VPRO node outputs and buffer outputs are shown for two cases - the buffers' frequency control is connected to that of the VPRO/held constant.

bandwidth for 24-27 GHz system operation, the bandwidth is increased beyond 2 GHz to provide margin and ensure a linear tuning characteristic in the desired range. This amount of tuning bandwidth is significant, given that a large portion of the capacitance budget is used toward phase-shifting.

B. Waveform-Adaptive Tunable-Narrowband Design Approach

The design of UWB RF blocks is challenging as a large number of passive elements is usually needed to match ports to a desired impedance and achieve a wideband transfer function. An alternative is to design narrowband blocks with low Q, as the bandwidth of an RLC tuned load is inversely proportional to its Q. However, this comes with the penalty of high loss levels and low gain, or, alternatively, a larger current consumption to main the same gain and power levels.

In this paper, we propose a new UWB design paradigm that takes advantage of the known shape and characteristics of the waveform(s) being used. The UWB VPRO-PLL architecture generates UWB signals that are phase- or frequency-modulated (such as the linear FM chirp for radar), and the control voltage of the VPRO is a measure of the signal's instantaneous frequency. Therefore, the tuned blocks that follow the VPRO, such as the output buffers, squarers and PAs, may be designed to be high-Q, *tunable-narrowband* systems, whose center frequency is also controlled by the control voltage. In other words, the transfer function of the RF chain *tracks* the instantaneous frequency of the signal, achieving wideband performance while being instantaneously narrowband in nature.

Fig. 3 shows the frequency control of the buffer V_{tune_op}

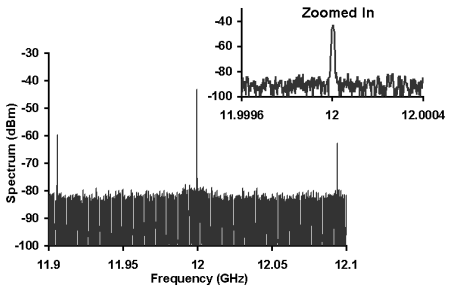

Fig. 5. Measured spectrum of the 12 GHz on-chip reference under lock.

(achieved through varactors) being connected to the control voltage of the VPRO. Fig. 4 depicts the result of a SpectreRF simulation of the VPRO and its buffers when the control voltage is linearly ramped with time to produce a chirp. Fig. 4(a) shows that a linear ramp in the control voltage results in a linearly increasing instantaneous frequency while Fig. 4(b)-(d) show how the tuning of the buffers along with the VPRO leads to tracking of amplitudes and phases between the buffer outputs and VPRO node outputs, thus minimizing the distortion between the two in the frequency response. When the buffers are not tracked, significant distortion is introduced between VPRO node outputs and the buffer outputs. This is important as the radar receiver would use an identical VPRO to correlate with the incoming signal, and distortion in the transmitter and receiver front-end circuits reduces the SNR benefit achieved through matched filtering.

In the prototype presented in this paper, only the buffers were designed to track the VPRO frequency, since the squarers and PAs were capable of supporting the desired bandwidth without a significant gain or power penalty. If a larger bandwidth is desired, the squarers and PAs may also be designed as tunable-narrowband systems.

C. Reference Chain and Analog PLL Design

The on-chip 12 GHz reference is implemented as a cross-coupled LC oscillator utilizing only pMOS transistors, due to the high nMOS flicker-noise corner. It is locked in a divide-by-128, digital PLL that utilizes static frequency dividers, a standard, tri-state, phase-frequency detector and a charge pump. The Quadrature all-pass filter employs a single-stage RC-CR network while the analog PLL that locks the VPRO to the modulated reference uses a three-stage mixer as its phase detector and a first-order RC loop filter. The tracking range of the analog PLL governs the bandwidth of the chirp waveform that may be generated, while the loop bandwidth governs μ, the rate of the chirp.

IV. Measurement Results

This section summarizes the measurement results of the fully-integrated, 4-channel, 24-27 GHz, CMOS phased array transmitter prototype. Fig. 2 depicts the microphotograph of the chip, which was implemented in a 0.13 μm CMOS process

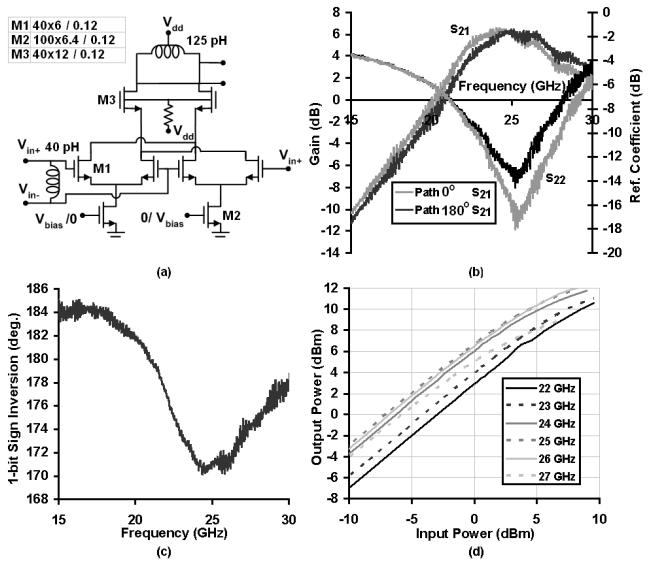

Fig. 6. (a) PA circuit diagram (b) Measured small signal parameters for $0/180^o$ paths (c) 1-bit sign inversion (d) Measured large signal performance.

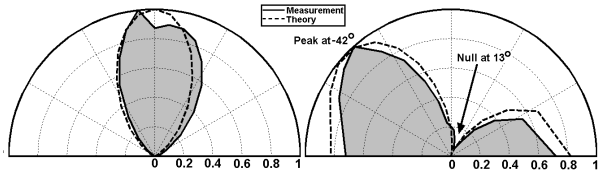

Fig. 7. Measured 2-element narrowband array patterns at 24.75 GHz.

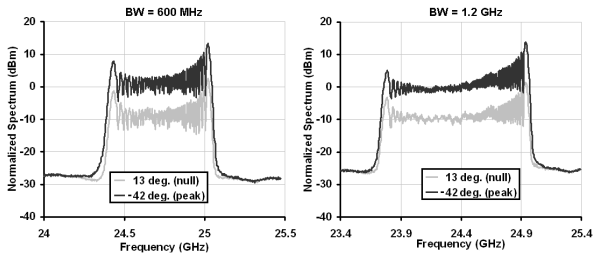

Fig. 8. Measured spectrum of the transmitted UWB FM beam along the expected peak and null directions when the beam is steered to -42^o. Two elements are active and two different signal bandwidths are considered.

with 8 metal layers and no special analog options, such as a thick upper metal layer or MIM capacitors. The chip occupies 2.7 mm x 1.8 mm of die area and draws approximately 750 mA from a 1.5 V supply when all channels are enabled.

Fig. 5 shows the spectrum of the 12 GHz on-chip reference when locked to an external 93.75 MHz reference in the divide-by-128 digital PLL.

The circuit diagram of the PA of each channel is presented in Fig. 6(a). To achieve 1-bit sign inversion, two differential pairs with inverted inputs are used. Each pair may be enabled through its tail transistor, and the drains of both are tied to each other. A cascode pair is used to enhance reverse isolation and both ports are matched to a differential impedance of 100 Ω through lumped inductors. Fig. 6(b)-(d) present the measured PA performance. Wideband performance between 24 GHz and 27 GHz is seen for small- and large-signal drive and 1-bit sign inversion is achieved. Each PA draws 88 mA from a 1.5 V supply during linear operation and achieves a saturated output power in excess of 12.1 dBm at 26 GHz, corresponding to a peak drain efficiency greater than 13%.

In order to experimentally validate the beam-steering capability of the prototype, narrowband array patterns are measured at 24.75 GHz with two elements active, assuming half-wavelength antenna separation. The propagation of the transmitted beam in free-space is emulated using external, variable delay elements. Fig. 7 shows the results of these measurements for two different settings. To assess UWB beam-steering functionality, wideband FM waveforms of varying bandwidths are generated by direct FM modulation of the VPRO control voltage with a 5 MHz sinusoid of varying amplitude. Once again, two channels are enabled and the transmitted beam in different directions is measured. Fig. 8 shows the measured normalized spectrum when the beam is steered to -42^o (corresponding to the second narrowband pattern in Fig. 7) for two different signal bandwidths along the expected peak and null directions. Indeed, the power spectral density (PSD) in the null direction is suppressed by approximately 10 dB when compared to the peak direction.

V. Conclusion

A fully-integrated, UWB, 4-channel, K-band, CMOS, phased-array transmitter is demonstrated. The transmitter targets vehicular radar applications, and utilizes the VPRO-PLL architecture, which is extended to UWB capability through architectural and circuit innovations. A waveform-adaptive, tunable-narrowband design paradigm is introduced that simplifies the design of UWB RF blocks. The architecture can be extended to support pulsed-sinusoidal UWB waveforms through the implementation of a fast, pulse-shaping switch before or after the PAs. Such architectural innovations that result in area- and power-efficient imlpementations, coupled with the frequency-handling capability of modern CMOS processes, can make the deployment of fully-integrated, high-performance, low-cost, UWB vehicular radar sensors a reality.

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