## 6.7 A Fully Integrated 24GHz 4-Channel Phased-Array Transceiver in 0.13µm CMOS Based on a Variable-Phase Ring Oscillator and PLL Architecture

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Phased arrays are a special class of multiple antenna systems that allow for electronic beam-steering through the introduction or compensation of time delays in the signal paths of different antennas. The amount of additional time delay that is introduced/compensated in each successive signal path determines the angle of radiation/incidence at which the electromagnetic signals add up coherently. In addition to spatial selectivity, the SNR of an $N$-channel phased-array receiver is enhanced by $10\log_{10}(N)$ decibels compared to that of a single-channel receiver [1]. Phased-array transmitters represent a high-efficiency spatial power-combining scheme and relax the PA output power requirements of each channel [2]. The complete integration of phased-array transceivers in a CMOS process offers tremendous possibilities for low-cost high-speed wireless communication systems and radar.

In narrowband phased arrays, the required time delay is often approximated with a phase shift to ease the implementation. In CMOS implementations, RF phase shifting and power combining, prior to the mixing action, is challenging due to the loss of on-chip passive components. Alternately, phase shifting may be accomplished in the LO path [1-3], where the loss of the phase shifters is moved out of the RF path. Multi-phase oscillators have been used to produce the necessary LO phases [1, 2]. However, the interconnect structure required to distribute these LO phases consumes significant chip area. The LO phases can also be realized locally through phase interpolation of a quadrature oscillator to reduce the size of the LO distribution structure [3].

In this paper, a fully integrated phased-array transceiver architecture is introduced that eliminates all the RF phase shifters, distribution networks, power combiners, and RF mixers. The phased-array transceiver is based on a variable-phase ring oscillator in a PLL (VPRO-PLL). In the transmit mode, the VPRO-PLL modulates the baseband information and provides the appropriately phase-shifted modulated signal to each antenna element. In the receive mode, the incoming RF signals for all channels are phase shifted, downconverted, and coherently combined inside the VPRO-PLL. Figure 6.7.1 shows the compact implementation of a 4-channel phased-array transceiver prototype at 24GHz based on the VPRO-PLL concept. The chip is implemented in a 0.13µm CMOS process with 8 metal layers and occupies an area of 2.35×2.15mm$^2$.

The 4-stage VPRO consists of tuned amplifiers connected in a ring configuration with an additional phase shifter. The additional phase shift is distributed evenly among all 4 VPRO stages to satisfy the loop boundary condition in such a way that the total phase shift in the ring is zero. Hence, a linear phase progression is established across the VPRO stages, which is the requirement to electronically steer the beam in narrowband phased arrays. The VPRO oscillation frequency is set to the desired value through the PLL.

In the transmit mode, the baseband information is fed into the PLL through the control voltage, $V_{ctrl}$ (Fig. 6.7.2). The baseband signal is frequency modulated around the VPRO oscillation frequency. The output signal of each VPRO stage is the frequency-modulated signal with a controllable phase shift relative to the adjacent stage. Each VPRO stage drives a 24GHz on-chip power amplifier for each antenna element without requiring any power distribution network.

In the receive mode, each 24GHz on-chip LNA injects its received signal into the tuned resonator of the corresponding VPRO stage in the current domain (Fig. 6.7.2). In the absence of these input signals, the PLL is locked to a reference frequency and $V_{ctrl}$ is fixed. The incoming modulated signals pull the VPRO frequency. In an attempt to maintain lock, the value of $V_{ctrl}$ in the PLL is modified to follow the modulation [4]. It can be shown that, within the PLL loop bandwidth, the strength of this downconverted signal at $V_{ctrl}$ is $\frac{\omega\varepsilon}{2QK_{VCO}}\left|\frac{\sin N\frac{\Delta\theta-\Delta\phi}{2}}{N\sin\frac{\Delta\theta-\Delta\phi}{2}}\right|$, where $\omega$ is the PLL oscillation frequency without any injection, $Q$ is the VPRO resonator quality factor, $K_{VCO}$ is the VCO gain, $\varepsilon$ is the ratio of the injected signal amplitude to the undisturbed oscillation amplitude, and $\Delta\phi$ and $\Delta\theta$ are the phase progressions of the VPRO and the received signals, respectively. The strength of the downconverted signal at $V_{ctrl}$ exhibits the very same spatial selectivity as a conventional phased-array receiver does. It should be emphasized that the phase-shifting, power combining, and downconversion are done through the combined VPRO-PLL action without any explicit blocks.

Each 24GHz differential LNA is a 2-stage, inductively degenerated design, where cascode configuration is used to improve the reverse isolation and stability (Fig. 6.7.3). The input and output of both stages are matched to 100Ω differential impedances. The 24GHz on-chip PA is a single-stage pseudo-differential-pair with cascode transistors. A PA driver feeds the VPRO signal to the appropriate PA. All the on-chip high-frequency signal routing is accomplished through differential substrate-shielded coplanar striplines [5] with characteristic impedance of 100Ω. A stand-alone PA has a measured small-signal power gain of 11dB at 22GHz and a saturated output power in excess of 12.9dBm with a peak drain efficiency greater than 18.8% (Fig. 6.7.4). The center frequency of all tuned blocks can be adjusted through NMOS varactors.

The VPRO stages are implemented as differential pairs with $LC$ resonant loads using NMOS varactors. The design and layout of the VPRO should be symmetric to guarantee a linear phase progression between adjacent elements. In this implementation, the phase shifter is realized as 4 tuned differential pairs identical to the VPRO stages. The varactor control voltages of these additional stages are tied together and control the phase of the VPRO. Each VPRO stage can sustain a maximum phase shift of ±60°. Although not realized in this prototype, the extra phase shift, necessary for extreme steering angles, can be obtained by flipping the differential connections. It can be shown that the proposed VPRO phased-array architecture is less sensitive to component mismatches by an order of magnitude compared to other phased arrays that do not use phase shifters such as those using coupled oscillators. The VPRO is locked in a charge-pump-based PLL where the dividers are implemented using static D-flip flops (Fig. 6.7.5).

Transmit and receive array patterns are measured to test the phased-array functionality. Power splitters and variable phase shifters are used to emulate the propagation of a plane wave in space. Transmit and receive array patterns for the same angles are measured to be similar. Fig. 6.7.6 shows the measured 4-channel transmit patterns and 2-channel receive patterns for a few angles of radiation/incidence when the antenna separation is half-wavelength at 24GHz. A close match between the measured and ideal array patterns is observed. The phased array in the receive mode achieves a total gain of 42dB and theoretically improves the receiver SNR by 6dB. In the transmit mode, the array EIRP is enhanced to 24.9dB. Figure 6.7.7 summarizes the measured performance of the chip.

*References*:

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[2] A. Natarajan, A. Komijani, and A. Hajimiri, "A 24GHz Phased Array Transmitter in 0.18µm CMOS," *ISSCC Dig. Tech. Papers*, pp. 212-213, Feb., 2005.

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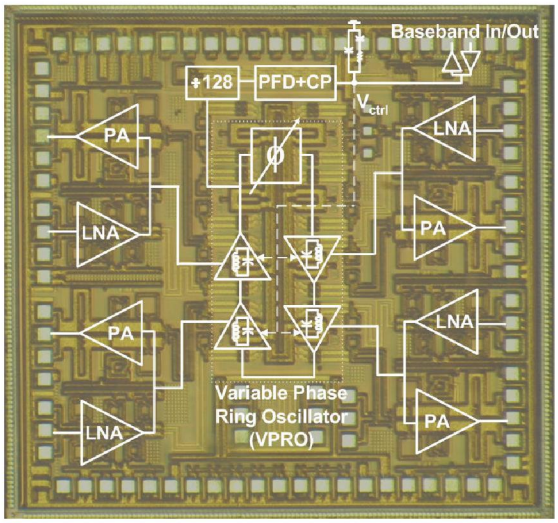


Figure 6.7.1: Simplified block diagram and chip micrograph of the 4-channel phased-array transceiver.

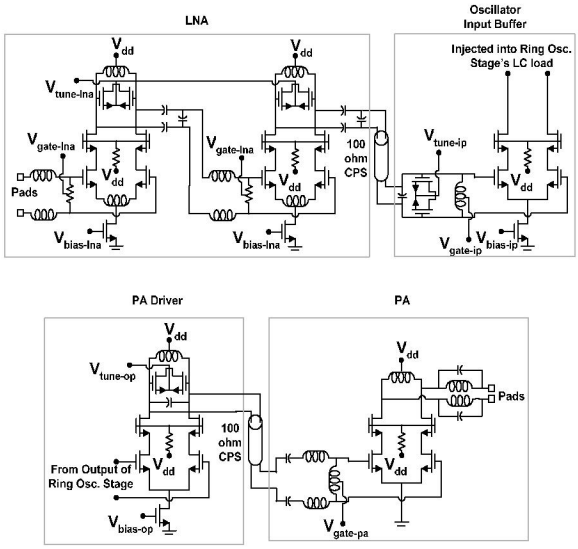


Figure 6.7.3: Schematics of the LNA, PA and VPRO buffers.

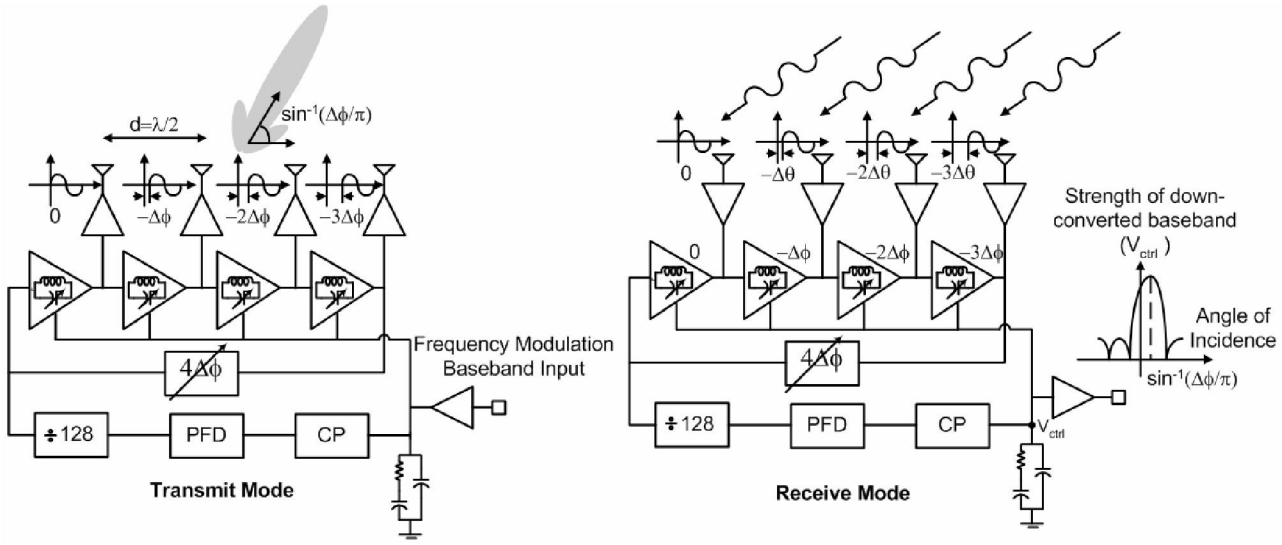


Figure 6.7.2: Principle of operation of the VPRO-PLL phased-array architecture –receive and transmit modes.

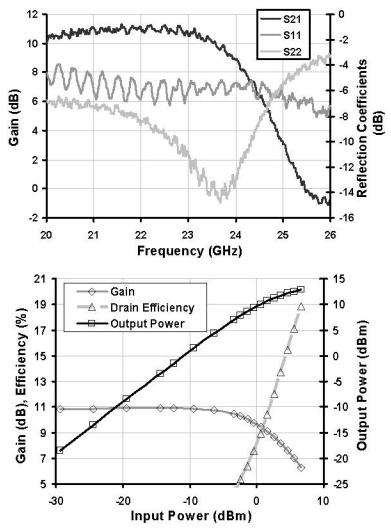


Figure 6.7.4: Measured power amplifier small-signal S-parameters and large-signal performance at 22.25GHz.

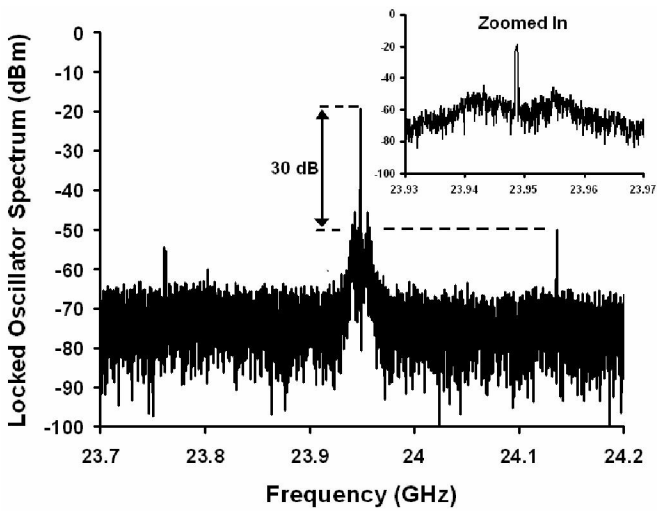


Figure 6.7.5: Measured spectrum of the locked VPRO.

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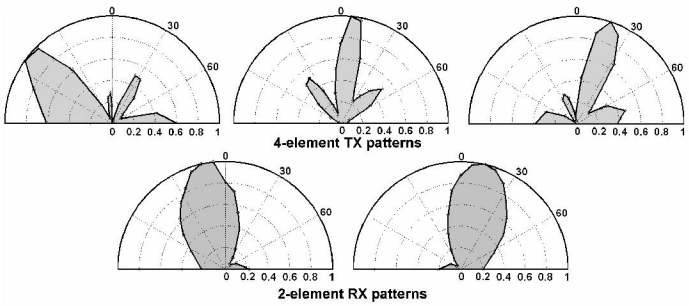


Figure 6.7.6: Measured array patterns for half-wavelength antenna separation.

**Phased Array Specification**

| | |
|---|---|
| Number of channels | 4 |
| Frequency of Operation | 24GHz |

**Transmitter Performance**

| | |
|---|---|
| Maximum PA Output Power | >12.9dBm |
| 4-element EIRP | >24.9dBm |
| Peak PA Drain Efficiency | >18.8% |
| PA Power Consumption per element | 78mA @1.5V |
| PA Driver Power Consumption per element | 13mA @1.5V |

**Receiver Performance**

| | |
|---|---|
| Receiver Gain | 30dB |
| Total Array Gain | 42dB |
| SNR Improvement | 12dB |
| LNA Power Consumption per element | 25mA @1.5V |
| VPRO Input Buffer Power Consumption per element | 2.5mA @1.5V |

**LO Path Performance**

| | |
|---|---|
| VPRO Power Consumption per element | 7.5mA @1.5V |
| Digital Dividers Power Consumption | 85mA @1.5V |
| PFD + Charge Pump Power Consumption | 16mA @1.5V |

**Implementation**

| | |
|---|---|
| Process Technology | 0.13µm CMOS |
| Chip Size | 2.35mm x 2.15mm |

Figure 6.7.7: Measured performance summary.

 