Design of All-Passive Higher-Order CMOS N-Path Filters

Negar Reiskarimian and Harish Krishnaswamy
Department of Electrical Engineering, Columbia University, New York, NY, 10027, USA

***Abstract*— In this paper, a methodology for designing all-passive higher-order N-path filters is described. The methodology extends known filter synthesis techniques for LC filters to N-path filters through the use of lumped quarter-wave transmission-line (t-line) equivalents that enable series-LC-like N-path structures. The quarter-wave t-line equivalents also isolate N-path filters from each other, allowing N-path sections to be cascaded to realize filters of arbitrary order. A tunable, nominally 6th-order, high-Q N-path bandpass filter based on this methodology has been implemented in 65nm CMOS. The filter has an insertion loss of 4.7-6.2dB, a tuning range of about 35% from 600MHz to 850MHz, and bandwidth that ranges from 9-15MHz, resulting in a Q that ranges from 40-90. The filter achieves an out-of-band (OOB) rejection of 30-50 dB, input-referred in-band (IB) and OOB 1dB compression point of 0dBm and +14dBm, and input-referred IB and OOB IIP3 of +7 and +17.5dBm respectively. The clock path DC power consumption at 700MHz is 75mW from a 1.2V supply.**

***Index Terms*— Tuned circuits, Band-pass filters.**

I. Introduction

Filters play a crucial role in radio transceivers, and are used for front-end band-selection and intermediary channel-selection in receivers and as output filters in transmitters. Perhaps the most significant challenge facing reconfigurable/software-defined radios is the realization of highly-linear, high-Q tunable filters.

N-path filters have recently re-emerged as a promising solution to realize highly-linear, high-Q tunable on-chip filters. However, the original topology [1] only results in a second-order filtering profile which may not be sufficient for many applications. Recent research efforts to realize higher-order N-path filter responses have relied on the incorporation of active circuitry in the filter topology [2], [3]. To achieve a 4th order response, the authors of [2] use the difference of two slightly-shifted 2nd order filters, with the frequency shifts accomplished using an N-path Gm-C technique. It should be noted that this is not a scalable solution to achieve arbitrary order. The authors of [3] have developed a methodology to design active N-path filters employing gyrators in the signal path.

This paper presents a design methodology using only passive elements to synthesize N-path filters of arbitrary order and type. The methodology extends known filter synthesis techniques for LC filters to N-path implementations. A study of various loss mechanisms is presented, and the methodology is verified through the implementation and measurement of a 600-850MHz, nominally 6th-order, high-Q N-path filter in 65nm CMOS.

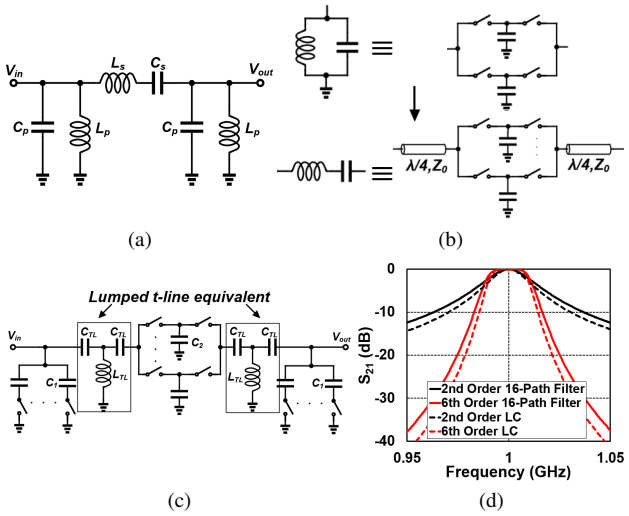
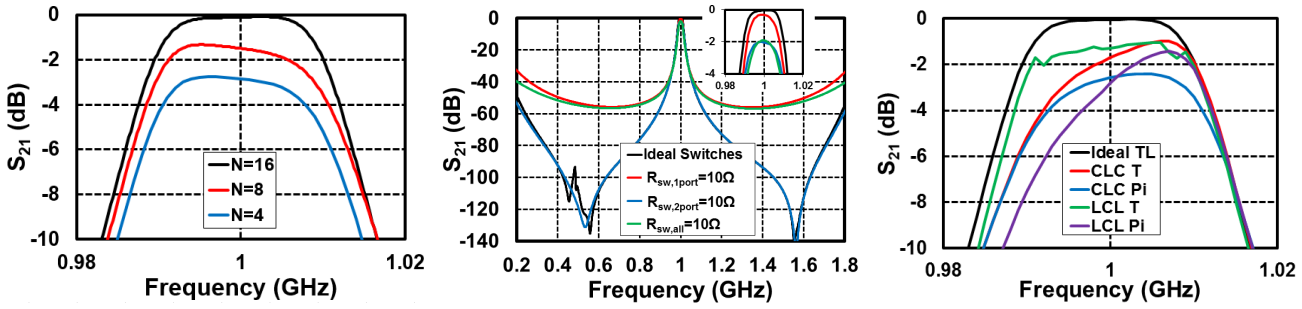


Fig. 1. (a) 6th-order LC filter. (b) Shunt-LC to series-LC transformation of a two-port N-path filter using quarter-wave t-lines. (c) Proposed architecture of an all-passive 6th-order (in general, arbitrary order) N-path filter with CLC T-type quarter-wave t-line equivalents. (d) Simulated comparison of 1GHz 2nd- and 6th-order 20MHz bandwidth Butterworth LC and N-path filters with ideal switches and passive components.

II. Filter Design Methodology

It is known that filters of any desired type (Butterworth, Chebyshev etc.) and any desired order can be achieved by cascading shunt and series LC sections (Fig. 1(a)). However, two fundamental challenges exist in extending this design methodology to N-path filters. Firstly, the conventional N-path bandpass filter discussed in [4] has a transfer function that is equivalent to a shunt LC section close to its center frequency. However, no N-path filter structure has been reported that is equivalent to a series LC section. *Intuitively, a series-LC-like N-path filter would require switching a series inductor (with switches on both sides of the series inductor), and an impractically-large (and consequently lossy) inductor value would be required for typical passband bandwidths.* A second challenge is that N-path filters cannot be simply cascaded due to their linear periodic time-variant (LPTV) nature. *Cascading N-path filters would result in interaction (charge sharing) between the switched capacitors, and significant deviation*



(a) (b) (c)

Fig. 2. Simulation of different loss factors on the performance of the 1GHz all-passive Butterworth 6th-order N-path filter designed for 20MHz bandwidth (in each figure only the effect of one loss source has been taken into account and other parameters are ideal): (a) effect of finite number of paths, (b) switch resistance, and (c) lumped t-line equivalent implementation on the loss and filter shape.

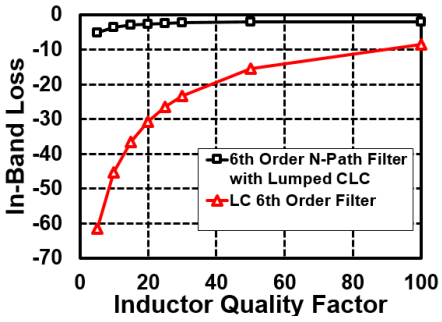


Fig. 3. Comparison of IB loss versus quality factor of the utilized inductors in the 1GHz 6th-order Butterworth 20MHz bandwidth LC and all-passive N-path filter.

from the expected response.

Our proposed methodology uses quarter-wave t-lines on either side to transform a shunt-LC-like response to a series LC section (Fig. 1(b)). While the original N-path filter that was been proposed in [1] uses two sets of mixers (switches) to translate a low-frequency filter profile to a bandpass center frequency, in recent implementations, one set of switches has been eliminated, resulting in merging of the input and the output node. In other words, a single-port filter configuration is realized with lower clock path DC power consumption and better noise performance [4]. In order to isolate the input and the output nodes, we revert to the two-port shunt-LC-like N-path filter and transform it to series-LC behavior using quarter-wave t-lines (Fig. 1(b)). The required shunt-LC sections of the original LC filter are still realized using the one-port configuration (Fig. 1(c)).

A complete LPTV analysis of the proposed filter topology is beyond the scope of this paper, but it is interesting to note that the quarter-wave t-lines also eliminate the interaction between the N-path filters. *Consequently, each N-path filter can be independently designed to emulate the LC section that it is replacing.*

The use of quarter-wave t-lines will limit the tuning range. As will be seen later in the paper, the quarter-wave t-lines are implemented as lumped-LC two-port equivalents. The Cs of the two-port equivalents are realized as switched-capacitor banks, which allow partial reconfiguration of the operating frequency. Indeed, tuning both L and C is required to maintain characteristic impedance while tuning the quarter-wave frequency. Nevertheless, tuning C alone allows 600-850MHz operation in our prototype, or a tuning range of 35%, which is sufficient to cover the LTE low bands for instance.

A single-port 4-path system and its equivalent RLC tank were analyzed in [4]. Ignoring switch resistance, a similar derivation for a two-port N-path filter with a capacitance of C_2 in each path results in an RLC tank with the following R_{2port}, L_{2port} and C_{2port} values:

$$R_{2port} = \frac{4R_sR_lN^2(1-\cos(\frac{\pi}{N}))}{4\pi^2R_l - N(R_s+R_l)(1-\cos(\frac{\pi}{N}))}, \quad (1)$$

$$C_{2port} = \frac{N((R_l||R_{2port})+R_s)}{4\pi(f_{r_{SC}}+f_{r_{LC}})(R_l||R_{2port})R_s}, \quad (2)$$

$$L_{2port} \approx \frac{1}{C_{2port}(2\pi f_s)^2}. \quad (3)$$

Here, R_s and R_l are the real source and load impedances, and f_s is the clock frequency. $f_{r_{SC}}$ is equal to $\frac{1}{2\pi R_sC_2}$ and $f_{r_{LC}}$ is equal to $\frac{1}{2\pi R_lC_2}$.

Let us assume that the bandpass higher-order LC filter to be emulated has component values L_s, C_s, L_p and C_p as in Fig. 1(a)). Using (2) and a generalization of equation (19) in [4] to N paths, and assuming R_0 is the reference impedance, the value of C_1 and C_2 can be computed as:

$$C_1 = \frac{2C_pR_{1port}}{N(R_{1port}+R_0)}, \quad (4)$$

$$C_2 = \frac{4(R_0+R_{2port})}{NC_s(Z_0.2\pi f)^2((R_0||R_{2port})+R_0)}. \quad (5)$$

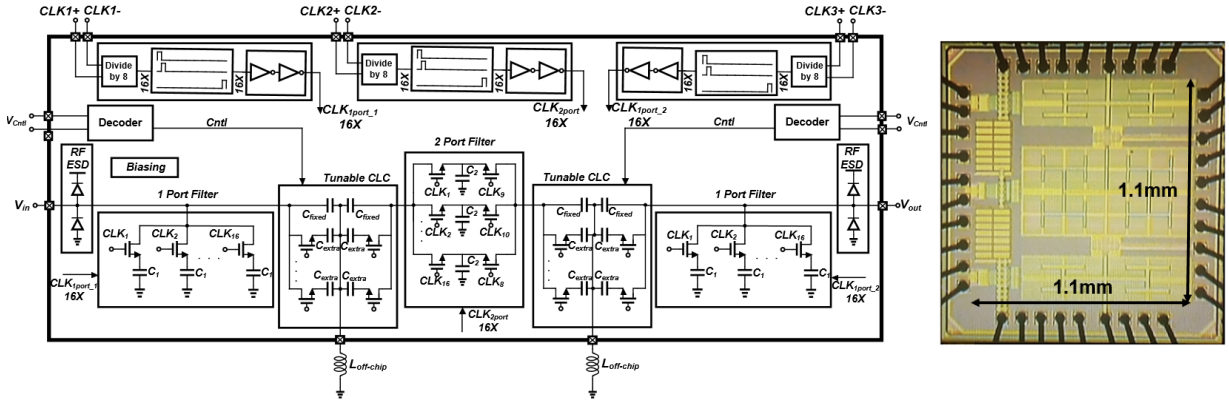


Fig. 4. Block diagram, schematic and chip microphotograph of the 65nm CMOS 600-850MHz all-passive 6th-order N-path filter.

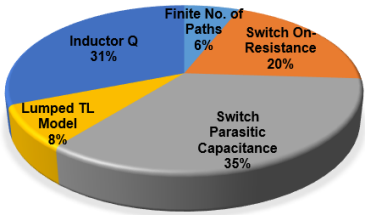


Fig. 5. Pie chart showing the distribution of loss for the 65nm CMOS all-passive Butterworth 6th-order 1GHz N-path filter (16 paths, $R_{sw,1port}$=10Ω, $R_{sw,2port}$=4Ω, Q_L=15 and using a lumped CLC T-type t-line equivalent).

Fig. 1(d) depicts a comparison between simulations of ideal 2nd- and 6th-order Butterworth LC filters designed for 1GHz center frequency and 20MHz bandwidth, and 2nd-order 16-path and all-passive higher-order 16-path filters with ideal switches and passive components. An extremely close match is seen, validating the methodology.

The implementation of quarter-wave t-lines at RF frequencies on chip is extremely area-hungry and lossy. Consequently, the quarter-wave t-lines may be replaced with two-port lumped T- or Pi-sections that are equivalent at the quarter-wave frequency. Four possible two-port lumped sections exist: CLC T-type, CLC Pi-type, LCL T-type and LCL Pi-type. The L and C values needed are independent of the nature of the section and are given by:

$$L_{TL} = \frac{Z_0}{2\pi f}, C_{TL} = \frac{1}{Z_0 \times 2\pi f}, \quad (6)$$

where f is the quarter-wave frequency. For ease of implementation, fewer number of inductors is preferable. To this end, CLC networks are advantageous (such as the CLC T-type network in Fig. 1(c)). The four possible networks differ from each other (and from a true quarter-wave t-line) in their response at harmonics of the operating frequency, and therefore can be expected to impact the filter performance given its LPTV nature. This is examined in the following section.

III. Design Trade-Offs and Loss Factors

The various factors that impact the performance of the proposed N-path filter include: finite number of paths, switch on-resistance, switch parasitic capacitance, the lumped LC t-line equivalents and the loss associated with the inductors in the lumped equivalents. The loss introduced by the finite number of paths ranges from negligible for 16 paths to ≈3dB for 4 paths for the 6th-order example in Fig. 2(a). Higher number of paths leads to more complexity and power consumption in the clock path. Switch on-resistance in the shunt one-port N-path filters affects filter OOB rejection but does not impact IB loss, while on-resistance in impedance-transformed two-port N-path filter has the opposite impact (Fig. 2(b)). Increasing switch size in the N-path filters increases clock path power consumption as well as the detrimental impact of switch parasitic capacitance. In Fig. 2(c), the impact of the lumped t-line equivalent network type is investigated. It is seen that the CLC T-type equivalent results in the best filter shape and loss. The impact of finite inductor quality factor (Q_L) is studied in Fig. 3 and is compared to the equivalent LC filter. Note that the CLC T-type sections only perform low-Q impedance transformation in the proposed N-path filter and do not store substantial energy. Consequently, the impact of finite inductor Q is small, especially when compared with the equivalent LC filter.

Fig. 5 shows the loss distribution when the filter is implemented in 65nm CMOS technology. For the example considered, 55% of the loss comes from switch on-resistance and parasitic capacitance which improve with CMOS technology scaling.

IV. Implementation and Measurement Results

The block diagram, schematic and chip microphotograph of the implemented filter are illustrated in Fig 4. The chip has been fabricated in 65nm CMOS

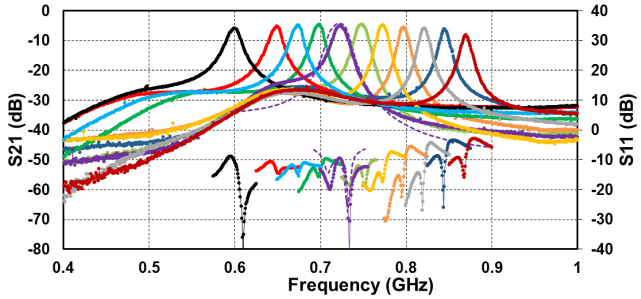


Fig. 6. Measured S21 and S11 for different clock frequencies in conjunction with reconfiguration of the CLC T-type networks. A comparison between measurement (solid) and simulations (dashed) is also shown for one frequency.

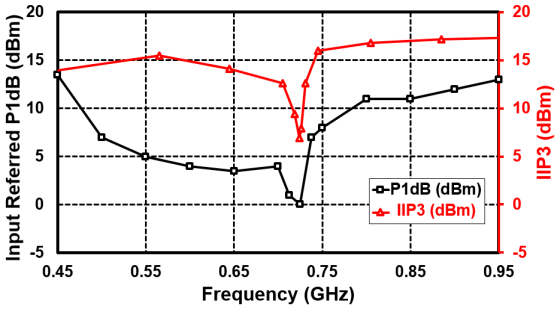


Fig. 7. Measured input referred P1dB and IIP3 for the filter tuned at a center frequency of 725MHz (for IIP3 f_{tone1} is shown on the X axis and $f_{tone2}=2f_{tone1}-f_c$).

technology with an active area of 1.2mm^2 and mounted in a QFN24 package. Each filter is implemented using 16 paths and separate clock generation has been utilized to ensure maximum symmetry in routing. The switch sizing is consistent with Fig. 5. The CLC sections are implemented using switched-capacitor banks to increase the tuning range and off-chip air-core 8.1nH inductors (0908SQ from Coilcraft, typical Q=100).

The measured S_{21} and S_{11} of the filter are shown in Fig. 6 and are compared to post-layout simulation results at one frequency. The filter can be tuned from 600-850MHz in conjunction with reconfiguration of the CLC T-type networks, with a bandwidth that ranges from 9-15MHz and a Q that ranges from 40 to 90. The IB loss is measured to be 4.7-6.2dB in this range with an OOB rejection of 30-50dB. IB and OOB P1dB of 0dBm and +14dBm are measured and plotted versus frequency in Fig. 7 for the filter tuned at 725MHz. Measured IB and OOB IIP3 are +7 and +17.5 respectively. The measured IB NF is 8.5dB (Fig. 8). The chip draws 75mW at 700MHz from a 1.2V supply.

A comparison between this work and previous N-path filters is shown in table I. The proposed filter exhibits sharper filtering and increased OOB rejection when compared with the conventional 2nd-order N-path filter

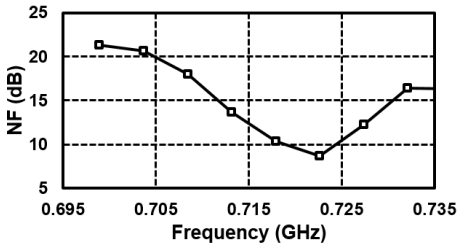


Fig. 8. Measured NF while clocking the filter at 725MHz.

[4] at the expense of increased IB loss, which is a trade-off that is typical for passive LC-based filters as well, and increased clock-path power consumption and reduced tuning range. The proposed filter is useful for applications where sharp filtering and moderate tunability is required, such as frequency-channelized receivers, perhaps preceded by a highly-linear front-end low-noise amplifier.

TABLE I
COMPARISON TABLE

	This work	[4]	[2]	[3]
CMOS Tech. (nm)	65nm	65nm	65nm	65nm
Filter Order	6	2	4	6
BW (MHz)	9-15	35	20	8
Freq. Range (GHz)	0.6-0.85	0.1-1	0.4-1.2	0.1-1.2
IB P1dB (dBm)	0	2	N/R	-23
OOB P1dB (dBm)	14	N/R	N/R	N/R
IB IIP3 (dBm)	7	>14	9	-12
OOB IIP3 (dBm)	17.5	N/R	29	26
NF (dB)	8.6	3-5	10	2.8
Gain (dB)	-4.7 to -6.2	-2	3.5	25
OOB rejection (dB)	30-50	15	55	59
Power consumption (mW)	75@700MHz	2-20	12.8-21.4	18-57.4

V. CONCLUSION

A design methodology for synthesizing all-passive higher-order N-path filters is introduced and demonstrated with a 6th-order 65nm CMOS prototype. Topics for future research include design methodologies that enable even wider frequency tuning and techniques for linearity enhancement of N-path filters.

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