Matching the power density and potentials of biological systems: a 3.1-nW, 130-mV, 0.023-mm^3 pulsed 33-GHz radio transmitter in 32-nm SOI CMOS

Jaebin Choi, Eyal Aklimi, Jared Roseman, David Tsai, Harish Krishnaswamy, Kenneth L. Shepard

Department of Electrical Engineering, Columbia University, New York, NY, USA

***Abstract* — A 3.1 nJ/bit pulsed millimeter-wave transmitter, 300µm by 300µm by 250µm in size, designed in 32-nm SOI CMOS, operates on an electric potential of 130mV and 3.1nW of dc power. These achieved power levels and potentials are comparable to those present across cellular and intracellular membranes. Far-field data transmission at 33 GHz is achieved by supply-switching an LC-oscillator with a duty cycle of 10^{-6}. The time interval between pulses carries information on the amount of power harvested by the radio, supporting a data rate of ~1bps. The inductor of the oscillator also acts as an electrically small (~λ/30) on-chip antenna, enabling the extremely small form factor.**

***Index Terms* — Implantable biological devices, low-power electronics, microwave antennas, millimeter wave communication, switched capacitor circuits.**

I. Introduction

Solid-state systems and biological systems have many complementary capabilities. For example, solid-state systems are uniquely capable of coupling to the radio-frequency electromagnetic spectrum for the transfer of information, while biological systems have capabilities for specific molecular recognition and the exploitation of biochemical energy sources. Nevertheless, biological systems and solid-state systems are characterized by fundamentally different physical characteristics, power densities, and operating voltages, which create many challenges in mating these functions, most evidently in the area of implanted medical devices [1].

From a physical form-factor perspective, solid-state systems tend to be hard and flat and biological systems round and pliable. One way to resolve this discrepancy is to make macro-scale electronics flexible [2]; the other is to miniaturize the solid-state to the point at which it is "small" compared to the relevant structure in the biological system to which it is interfaced. This work addresses the limits of the latter by scaling a radio transmitter to the size of the vacuoles of large monads, such as *Thiomargarita namibiensis* (Fig. 1b). These vacuoles, with diameters up to 500 µm, are reported to have metabolic rates on the nW scale [3], most of which support a proton motive force (PMF) that can be harnessed to power a system across the membrane.

The "nanoradio" transmitter developed here, designed to achieve the input voltage and power requirements to enable the exploitation of a PMF energy source, consumes 3.1 nW in a nearly cubic 300µm-by-300µm-by-250-µm form factor (Fig. 1c) in 32-nm SOI CMOS. These lower power levels are achieved through extreme-duty-cycling (10^{-6}) of an LC millimeter-wave (mmWave) oscillator, in which the inductor is repurposed as an electrically small (~λ/30) electromagnetic (EM) radiator. Power is integrated for about a second to provide the energy for an approximately 1-µsec-wide 33-GHz pulse by gating of the oscillator power supply. The large amount of capacitance required for energy storage (over 14 nF on the chip) is achieved through deep-trench capacitors extending 3.6 µm into the substrate. A switched-capacitor voltage multiplier boosts a 100-190 mV input voltage to over 300 mV to provide for oscillator startup, achieving a continuous-wave (CW) equivalent isotropically radiated power (EIRP) of -50 dBm and reading distance of 18 cm at 10 dB SNR. The interval between pulses is inversely proportional to the energy stored, meaning that the time interval between pulses carries information on the amount of power harvested by the radio. This information is encoded in the radio pulse stream at a bit rate of approximately 1 bps.

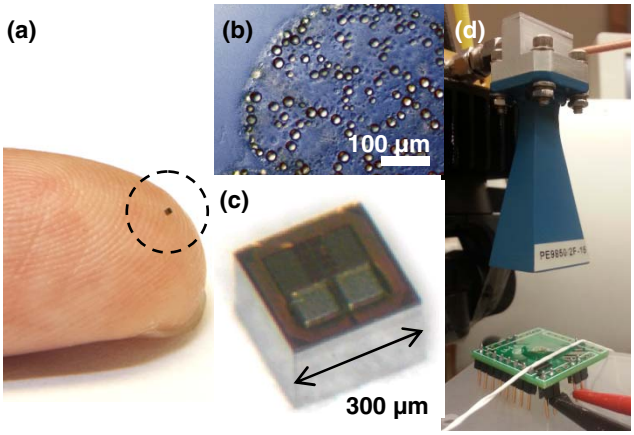

Fig. 1. (a) Nanoradio on fingertip; (b) *Thiomargarita namibiensis* at the same scale with (c) Die photo; (d) Horn receiver antenna at 10 cm transmission distance.

978-1-4799-3286-3/14/$31.00 ©2014 IEEE

II. Carrier Frequency Optimization

To improve radiation efficiency and load matching, RFID chips across a wide frequency spectrum to-date preferably exploit off-chip antennae which are much larger than the associated ICs, increasing overall system size to millimeter- or centimeter-scale [4,5]. Our motivation to make the nanoradio a cellular-scale implantable device leads us to limit any one dimension of system size to 300 µm including the antenna. The use of an on-chip integrated antenna circumvents the problem of antenna-chip alignment at such size scales but is inevitably accompanied by low efficiencies caused by losses in the metallization layers and silicon substrate [6]. We find that a 300-µm-diameter square loop antenna shows optimal low-power startup conditions at 33GHz, bringing the transmitter into the mmWave regime.

Recent work in mmWave communication has commonly relied on high dc power in order to maximize transmission distance and data rate [7]. This is due to the diminishing maximum available gain of devices at high frequencies, which is only overcome with larger bias currents. In this application where the maximum available power is bounded by biological constraints, we seek to maximize the amount of far field radiation energy generated per unit dc power. To achieve this, we choose a carrier frequency that allows minimal power consumption while meeting the startup condition of the LC oscillator.

Two factors contribute to the ratio of power received at the receiving antenna to power input to the transmitting antenna (the transmission gain, T) — the radiation efficiency of the transmitting antenna and the transmission loss as governed by the Friis transmission equation. Fig. 2 shows the simulated T (as determined by the product of these two factors, shown as a function of frequency) for the antenna used in the nanoradio. The increase in transmission loss with frequency is nearly completely compensated by the increase in radiation efficiency of the transmitting antenna with frequency.

Given the relative independence of T on frequency, the choice of carrier frequency is determined by the startup condition of the LC oscillator: $g_m > 2 \cdot R_{shunt}^{-1}$, where R_{shunt} is the shunt resistance of the inductor and g_m is the transconductance of the transistors M1 and M2 (Fig. 3g). When on, M1 and M2 are biased in weak inversion to consume minimal current, making g_m proportional to the drain current I_{bias} [8]. Fig. 2 shows that the value of g_m required for startup reaches a minimum at approximately 33 GHz. At this frequency, we find $I_{bias} \approx 500$ µA, approximately 10 times less bias current than would be required at an operating frequency of 2.45GHz, typical for many RFID tags, while resulting in equivalent T. Nanoradio transmitters are implemented with nominal oscillation frequencies (f_{osc}) of 29 GHz and 33GHz by varying the sizes of M1 and M2.

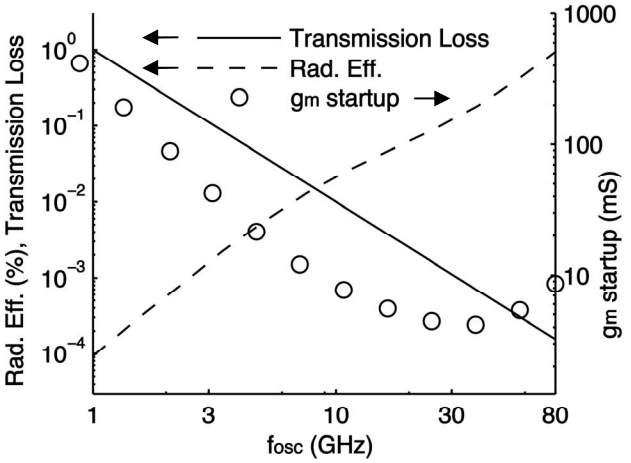

Fig. 2. Frequency response of the 300µm-wide loop antenna used in the nanoradio. Startup g_m required for oscillation startup ($2 \cdot R_{shunt}^{-1}$) reaches a minimum in the mid-30-GHz region. Simulated with IE3D.

III. Implementation

A. Ultra-subthreshold Switched Capacitor Voltage Multiplier. Operating transistors at 130 mV (~ 5.7 kT/q) results in I_{on}/I_{off} ratios of only 40. The switches of a voltage multiplier operating at this I_{on}/I_{off} ratio will be challenged by series resistance to produce the required multiplication and will do so at low efficiency. In addition, output impedances for the converters will be unacceptably large, resulting in large transient output voltage droops. Three stages of voltage boosting, all with current-starved gates, are employed to provide successively better switch function at each stage.

The entire system is controlled by an always-on ~ 1 Hz oscillator (Fig. 3a), based on a gate-leakage timer followed by a Schmitt trigger [9]. The 130-mV saw-tooth output of the timer is input into two independent buffer

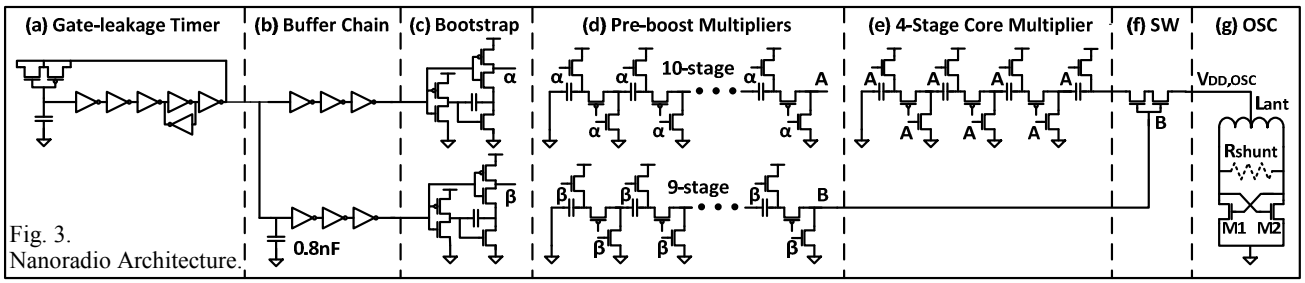

Fig. 3. Nanoradio Architecture.

chains, one of which is delayed by the addition of a 0.8 pF capacitance. These two time-offset 130-mV square waves emerging from these chains each feed into bootstrapped drivers, producing output swings up to 250 mV. The bootstrapped output (α) and the delayed bootstrapped output (β) drive "pre-boost" voltage multipliers with ten and nine capacitors, respectively. The pre-boost output (A) from the ten-stage multiplier has a 850-mV swing and drives the switches of the four-stage core multiplier (Fig. 3e), producing a more-than-300-mV supply for the oscillator. The pre-boost output (B) from the nine-stage multiplier, which has a 900-mV swing and is delayed approximately 10 µsec from A, opens the switch (SW) between the capacitor tank of the core multiplier and the LC oscillator, biasing the cross-coupled pair above the startup condition of ~ 500µA current (I_{osc}) into the antenna for 1-3 µsec until the capacitance of the core multiplier is sufficiently discharged.

This process repeats itself at each falling edge of the gate-leakage timer. The ratio of oscillator on-time to timer clock period is approximately 10^{-6}. To deliver a total of 0.15 nJ to the oscillator in a single pulse requires 3.09 nJ

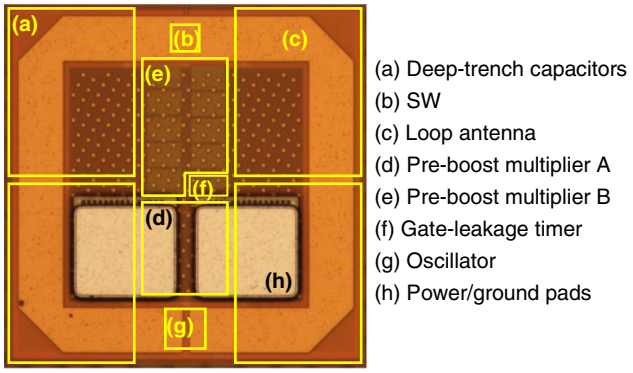

Fig. 4. Die photo with circuit positions noted.

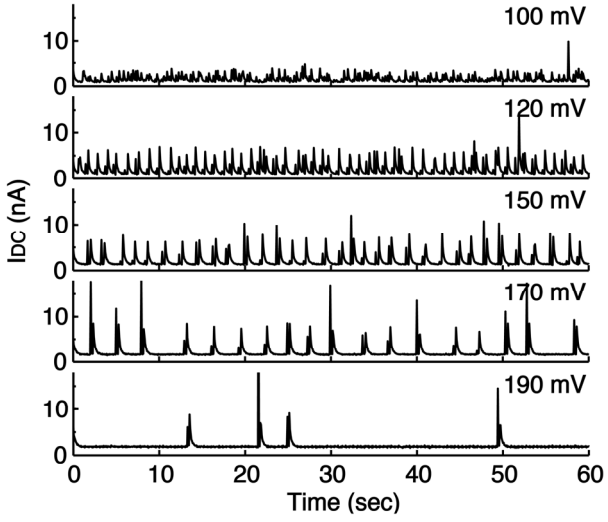

Fig. 5. Timer behavior with respect to changes in V_{DD}.

be drawn from the input supply for an overall efficiency of 4.9%. Ultra-subthreshold operation of the timing circuit produced an as-designed yield of 25% for these parts as a result of random variability in 32-nm CMOS.

B. Layout. To exploit a limited chip area of 300µm-by-300µm, a single-turn loop antenna (shown in the die photo of Figs. 1c and 4c) acts as both the far-field radiator and the inductor of the LC oscillator. Similarly, mmWave operation is achieved with the capacitance of the LC tank provided only by the device capacitance of the cross-coupled transistors (Fig. 3g). An nMOS-only oscillator is implemented as it improves the power generation efficiency of the oscillator due to the higher speed of nMOS transistors. The nMOS cross-coupled transistor pair is laid out using techniques to reduce terminal parasitics to increase drain efficiency [10].

The layout (Fig. 4) takes full advantage of the chip area bounded by the antenna perimeter. Deep-trench capacitors with nearly 200-times higher capacitance density (250fF/µm^2) than metal-metal capacitors occupy much of the area under the loop inductor, providing 13.7 nF for the four-stage voltage multiplier. The center contains the metal-metal capacitors of the nine-stage pre-boost multiplier, which is kept as distant as possible from adjacent metals to minimize parasitic coupling. Other on-chip components including the bootstrap drivers and gate-leakage timer are symmetrically placed in the center of the chip in order to produce an unskewed antenna radiation pattern. Two 90-µm-by-90-µm pads are also symmetrically placed on-chip, inside the loop antenna, for the input power supply.

IV. Measured Results

Fig. 5 shows the measured timer characteristics as a function of V_{DD} as measured indirectly through supply current of the full chip. This clock frequency (f_{timer}) reaches 1 Hz at a V_{DD} of 130 mV and inversely scales with voltage with a rate of ~1Hz/20mV. Oscillation is observed over the range of input supplies from 100 to 190 mV.

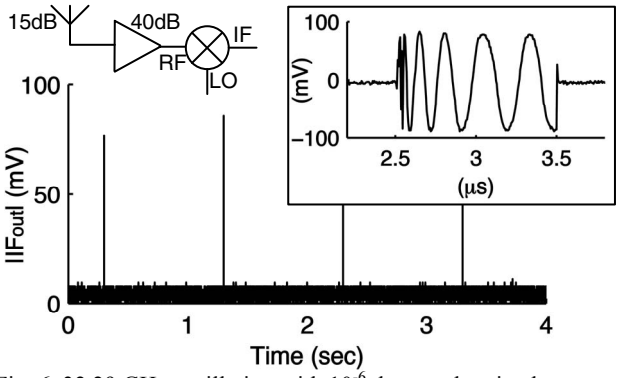

Fig. 6. 32.29 GHz oscillation with 10^{-6} duty cycle mixed to baseband using circuit shown.

The chip's RF transmission characteristics are studied with a 15-dB horn receiver antenna 10 cm away as shown in Fig. 1d. Fig. 6 shows the duty-cycled signal measured as an IF signal after down-converting to ~ 3 MHz by mixing with a 32.39-GHz carrier. The inset of Fig. 6 shows a detailed view of a transmission pulse, showing that the LC oscillator transient reaches steady-state within the 1-µs pulse width. The antenna oscillator startup behavior in relation to bias voltage is characterized in Fig. 7, for modules designed for both 29 and 33 GHz f_{osc} operation. CW EIRP of -49.89 dBm and -56.4 dBm are achieved at oscillator startup voltages ($V_{DD,osc}$) of 0.284 V and 0.327 V for the 29-GHz and 33-GHz designs, respectively. Low CW EIRP values are caused by the small dc power consumption of the oscillator and extremely small size of the antenna, which compromise the gain and radiation efficiency.

Ultra-subthreshold operation of the switched capacitor circuitry results in particularly large functionality variation in f_{timer} and power consumption (Fig. 8). f_{osc} shows less variation, facilitating a faster frequency sweep in search of the carrier frequency. Among the 80 dice, a total of 19 pulsed with an expected clock frequency of ~ 1 Hz. This is in accordance with Monte Carlo simulations including device mismatch and chip-to-chip variability.

Table 1 compares the performance of the nanoradio with an RFID operating at 45 GHz [5]. The energy consumed per transmitted bit is comparable between the two designs (~ 3 nJ/b), while the nanoradio uses only ~7% of the area (not including the antenna) and dc power of more than three orders of magnitude smaller. Table 1 compares the designs using (bit-energy × area)$^{-1}$ as a figure-of-merit (FOM).

TABLE I
NANORADIO TRANSMITTER SPECIFICATIONS

	Nanoradio	Pellerano [5]*
Carrier frequency	33GHz	45GHz
System area	0.3×0.3 mm^2 (antenna included)	1.3×0.95 mm^2 (without antenna)
Reading distance (for equivalent 13dB SNR)	12.7 cm**	1.3 cm*** (10^{-3} BER)
dc input power	3.1 nW	> 19 µW
Bit rate	1 bps	5 kbps
Energy cost per bit	~ 3.1 nJ	> 3.8 nJ
FOM ((bit-energy × area)$^{-1}$)	3.6 nJ^{-1}mm^{-2}	< 0.2 nJ^{-1}mm^{-2}

*Values obtained/calculated based on input power of 2 dBm.
**Measured with 15dB receiver antenna gain.
***Calculated for 3dB receiver antenna gain.

ACKNOWLEDGEMENT

This work was supported in part by the Keck Foundation and by the Office of Naval Research under Grant N00014-13-1-0375.

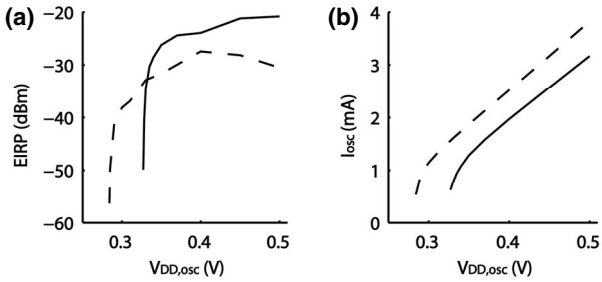

Fig. 7. RF oscillator characteristics. (a) EIRP; (b) I_{osc} for 33 GHz (solid) and 29 GHz (dotted) designs.

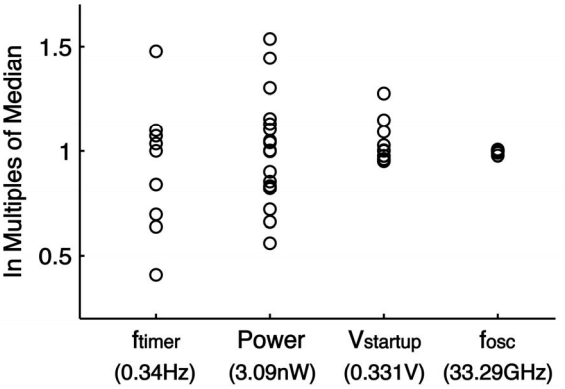

Fig. 8. Chip-to-chip performance distribution from 13 or more samples, with corresponding median values. $V_{startup}$ is the lowest value of $V_{DD,osc}$ to achieve 10 dB SNR at a 10-cm reading distance.

REFERENCES

[1] K. L. Shepard, T. Ito, and A. J. Griffith. "Extracting energy from the inner ear." *Nature Biotechnology 30*, 2012.

[2] J. A. Rogers, T. Someya, and Y. Huang. "Materials and mechanics for stretchable electronics," *Science 327*, 2010.

[3] N. Lane, and W. Martin. "The energetics of genome complexity." *Nature 467.7318* , pp. 929-934, 2010.

[4] M. Usami. "An ultra-small RFID chip: µ-chip," in *Advanced System Integrated Circuits 2004.*

[5] S. Pellerano, *et al*. "A mm-wave power-harvesting RFID tag in 90 nm CMOS." *Solid-State Circuits, IEEE Journal of* 45.8 (2010), pp. 1627-1637.

[6] F. Gutierrez, *et al*. "On-chip integrated antenna structures in CMOS for 60 GHz WPAN systems." *Selected Areas in Communications, IEEE Journal on*, 27.8, 2009.

[7] N. Deferm, et al. "A 120GHz fully integrated 10Gb/s wireless transmitter with on-chip antenna in 45nm low power CMOS," in *ESSCIRC (ESSCIRC), 2013*

[8] Y. Tsividis, *et al*. *Operation and Modeling of the MOS Transistor*. 3rd ed., Oxford University Press, 2011, p. 407.

[9] Y. S. Lin, *et al*. "A sub-pW timer using gate leakage for ultra low-power sub-Hz monitoring systems." *Custom Integrated Circuits Conference,* 2007.

[10] C. K. Liang and B. Razavi "A layout technique for millimeter-wave PA transistors." *Radio Frequency Integrated Circuits Symposium (RFIC)*, 2011.