RF Channelizer Architectures using Iterative Downconversion for Concurrent or Fast-Switching Spectrum Analysis

(Invited Paper)

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***Abstract*—We propose an RF channelizer architecture that uses the concept of 3-way Iterative Down-Conversion (IDC) to channelize a wideband incident spectrum while only using a fixed LO synthesizer. The proposed architecture can realize a concurrent channelizer that can analyze channels simultaneously, or a fast-switching channelizer that can analyze channels sequentially but with very short switching times between channels. We present an RF channelizer demonstrator prototype that was fabricated in a 65nm CMOS process. It implements a partially-concurrent architecture with the ability to concurrently down-convert a subset of channels while being able to switch very quickly between the non-concurrent channels. It splits an input spectrum of 0.6GHz-9GHz into 7 channels each of 1.2GHz bandwidth. Channelizer performance depends on the selected operation mode. The measured channel switching duration can be as fast as 8ns, and is always under $1\mu s$. The chip occupies an area of 2mm x 1mm and consumes an average power of 435mW while offering a dynamic range between 58dB to 63dB based on noise and linearity performance.**

I. Introduction

Future radio standards such as cognitive radio (CR) require broadband low-energy spectrum/signal analysis. Direct time-domain sampling and digitization over a multi-GHz bandwidth for digital signal analysis with multiple incident blockers necessitates a high-speed, high-dynamic-range, and consequently power-hungry, ADC. Frequency channelization can alleviate the energy requirement for spectrum analysis, as it relaxes the sampling rate and dynamic range requirements of the ADCs that follow due to the filtering of out-of-band blockers for each channel.

Active research is being conducted on broadband signal analysis and frequency channelization [1]–[4]. In [1], an up-downconversion architecture is utilized for DC-6GHz channelization with a fixed IF of 6GHz. The up-downconversion architecture has benefits in terms of harmonic rejection, interference mitigation and LO tuning range, but can be power hungry due to the larger number of blocks and the need for a higher-frequency LO signal. Furthermore, PLL settling leads to slow channel switching and so fast hopping signals cannot be tracked. In [2], multiple parallel receivers are used, each with their dedicated PLL. The LNA that splits the signal across multiple receivers is loaded with a large capacitance which limits the number of parallel channels. Operating multiple PLLs on the same chip is power hungry and often leads to coupling spurs.

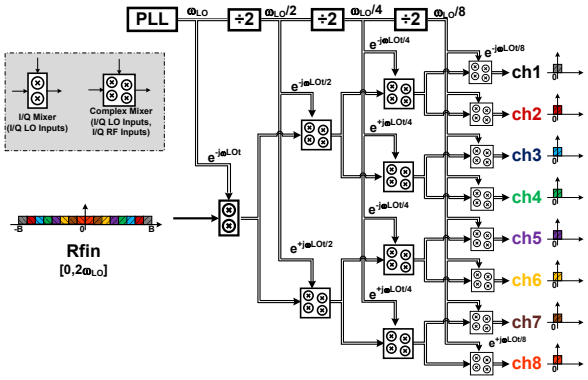

Fig. 1. Block diagram of the conventional IDC-based concurrent RF channelizer [3].

The iterative down-converter (IDC) has been introduced in [3], [4] to overcome the problem of LO synthesis in broadband frequency channelizers (Fig. 1). An IDC uses a cascade of image-rejection mixers to achieve LO synthesis from a fixed LO frequency and its subharmonics. However, this architecture suffers from channel-to-channel signal leakage that is limited by the finite image rejection or harmonic rejection of individual mixers.

In this paper, a novel 3-way splitting IDC cell is introduced to address the signal leakage performance. Using the 3-way IDC cell, a concurrent channelizer can be realized to analyze multiple channels in parallel or a fast-switching channelizer can be realized that analyzes channels sequentially but with a very short switching time between channels. The circuit design of a 65nm CMOS RF channelizer using a partially-concurrent IDC architecture is described that concurrently down-converts a subset of

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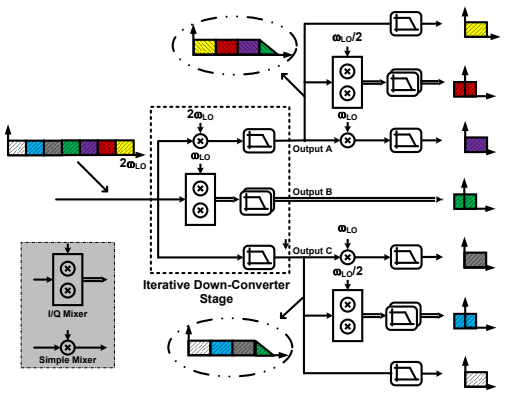


Fig. 2. Block diagram of a concurrent RF channelizer using the proposed three-way splitting IDC stage.

the different channels as well as rapidly switches from one non-concurrent channel to another. It decomposes an input spectrum of 0.6GHz-9GHz into 7 channels, each of 1.2GHz bandwidth, and produces 3 concurrent outputs.

II. Proposed 3-Way-Splitting Partially-Concurrent IDC Architecture

In the conventional IDC-based concurrent RF channelizer (Fig. 1), the effective LO in each branch of the IDC [3] is given by $\omega_{LO,eff} = \omega_{LO} \pm \frac{\omega_{LO}}{2} + ... + \frac{\omega_{LO,N}}{2^{N-1}}$ where N is the number of stages of frequency translation. However, with every stage of mixing, signal leakage is introduced due to finite image rejection and harmonic rejection. Harmonic rejection is typically limited to 30-40dB, which places a fundamental limitation on the signal leakage. The use of two-stage HRMs is possible to achieve higher harmonic rejection. However, using them in every mixer becomes a power hungry solution.

A key insight is that for several channels in the conventional IDC, there is significant redundancy in the multiple frequency translations used to finally obtain the channel at baseband. For instance, RF signals around $\omega_{LO}/2^{N-1}$ undergo N stages of frequency of translation instead directly being mixed with an LO of $\omega_{LO}/2^{N-1}$. Similarly, signals around $2\omega_{LO} - \omega_{LO}/2^{N-1}$ undergo N stages of frequency translation. Instead they can be down-converted in two steps using LOs of $2\omega_{LO}$ and $\omega_{LO}/2^{N-1}$.

The three-way splitting IDC cell, shown in Fig. 2, minimizes the number of frequency translations and performs only downconversions. Output A processes the upper half of the input spectrum by mixing the signal with $2\omega_{LO}$ and then filtering it. Output C filters out the lower half of the input spectrum without any mixing. Output B down-converts signals around the mid-band of the input signal using an LO of ω_{LO}. The addition of output B allows for a transition region between A and C so that the order of lowpass filters in A and C can be reduced without loosing full spectral coverage. All the required LO frequencies can still be obtained from a fixed LO synthesizer and its subharmonics obtained by division by two.

By cascading three-way IDC cells a fully concurrent RF channelizer can be realized as shown in Fig. 2. With two stages of IDCs, the input spectrum is split into 7 channels which are all available simultaneously. The signal leakage in a 2-way-IDC channelizer is limited by the harmonic rejection or image rejection of each mixer. This results in signal leakage in every channel . The proposed 3-way-IDC channelizer minimizes the number of mixers in several signal paths. This results in significant improvement in signal leakage performance in these paths.

The fully-concurrent channelizer architecture can be converted to a partially-concurrent, fast-switching architecture by combining the paths of Output A and Output C. This is easily accomplished by implementing a "transparent mode" into the (passive) $2\omega_{LO}$ mixer, where the switches are all kept on for the transparent mode. The block diagram of the prototype 0.6GHz-9GHz 65nm CMOS partially-concurrent, fast-switching RF channelizer based on such an architecture is shown in Fig. 3. It has two stages of the proposed 3-way-splitting IDC. The prototype has 3 concurrent outputs instead of 7 (as is the case for a fully concurrent channelizer). Output 1 down-converts channel 1 or 3 or 5 or 7, with an ability to rapidly switch between them. Output 2 down-converts channel 2 or 6, with an ability to rapidly switch between them. Output 3 down-converts channel 4. Since only a fixed LO source is used, the speed of switching is limited by bias settling in mixers and buffer amplifiers and signal settling in filters.

III. Circuit Implementation

Fig. 4 shows the circuit implementation of the various blocks of the channelizer along the path to Channel 2/6. Current driven passive mixers are used throughout the prototype for their superior linearity. A differential front-end LNTA provides a 100-ohm input impedance (differential) at the input interface of the chip and produces two amplified concurrent outputs to the first stage of the IDC. One output is used for midband down-conversion using the 4.8GHz I/Q mixer to directly down-convert channel 4. The second LNTA output drives the 9.6GHz dual-mode mixer, which can be operated either in transparent mode or in mixing mode. Based on its setting, either the lower or the upper part of the input spectrum is passed to the filter. Passive LC based filters were chosen for realizing the filtering considering the high frequency of operation and the superior linearity properties of an LC filter. The current buffer provides the appropriate load for the filters and produces concurrent outputs once again for the second 3-way IDC stage. In the second stage, one set of outputs of the current buffer (weighted as $1, \sqrt{2}$ and 1) drives the 2.4GHz harmonic-reject mixer and TIA to produce Output 2, which can fast-switch between channels 2 and 6 (shown in Fig. 4). The other drives a 4.8GHz dual-mode "I/Q" mixer (enabled by the availability of more LO phases from

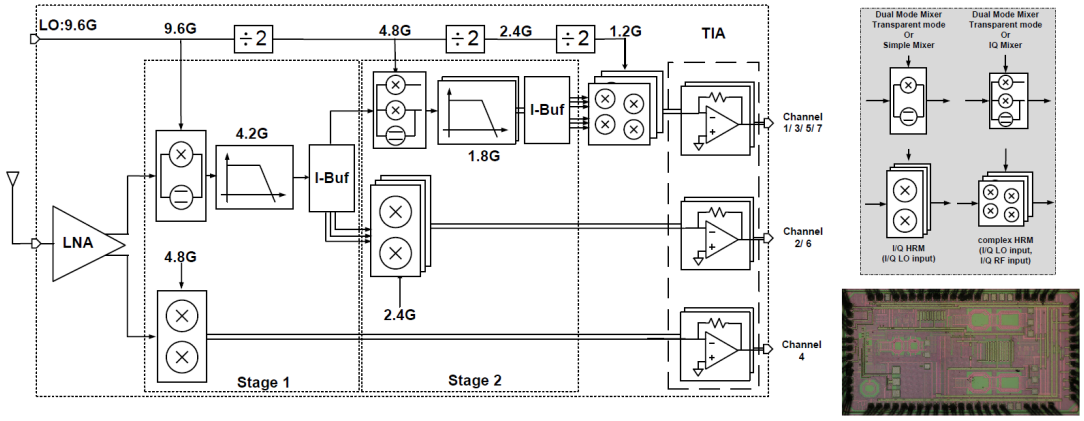


Fig. 3. Block diagram and chip microphotograph of the partially concurrent RF channelizer demonstration prototype with fast-switching using the proposed three-way splitting IDC stage.

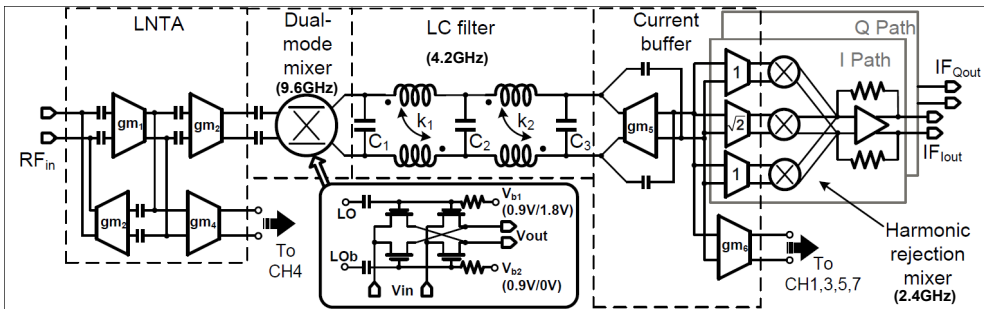


Fig. 4. Circuit implementation of various blocks of the RF channelizer along the path to Output 2, including the LNTA, 9.8GHz dual-mode mixer, 5th order 4.2GHz LC filter, current buffer and 2.4GHz harmonic rejection mixer.

TABLE I
RF CHANNELIZER MEASUREMENTS FOR P1DB, IIP3, NOISE FIGURE AND COMPUTED NOISE FLOOR AND SFDR

Channel		1	2	3	4	5	6	7
P1dB	[dBm]	-30.6	-21.7	-16.7	-21.3	-13.0	-13.8	-18.0
IIP3	[dBm]	-19.9	-12.4	-8.8	-12.5	-3.4	-5.5	-8.5
NF	[dB]	6.8	7.7	14.3	7.2	22.6	18.1	16.6
Noise Floor[1]	[dBm]	-107.2	-106.3	-99.7	-106.8	-91.4	-95.9	-97.4
SFDR	[dB]	58.4	62.6	60.6	62.9	58.7	60.2	59.3

[1] Noise bandwidth is assumed to be 1MHz

frequency division), filter, current buffer and a 1.2GHz harmonic-reject mixer and TIA to produce Output 1.

IV. MEASUREMENT RESULTS

Fig. 3 shows the die photo of the chip fabricated in a standard 65nm CMOS process. Table I presents the measured P1dB, IIP3, and NF for the channels of the RF channelizer. The spurious free dynamic range (SFDR) is computed as $\text{SFDR} = \frac{2}{3} \cdot (IIP3 - \text{NoiseFloor})$. A dynamic range between 58dB to 63dB based on noise and linearity performance is seen. Channel leakage measurements are depicted in Fig. 5. While several channels exhibit expected leakage performance, the leakage is degraded in some channels because of unexpected spurs in some of the mixers. The cause for these spurs is under investigation.

A. Concurrency

The RF Channelizer was experimentally verified to support concurrency: two signals were received simultaneously in Channel 1 and Channel 2. Fig. 6 shows the measured BER vs incident desired signal power for various power levels of signal in the adjacent channel. A 200Mbps BPSK signal was used in each channel resulting in a aggregate data rate of 0.4Gbps for two channels.

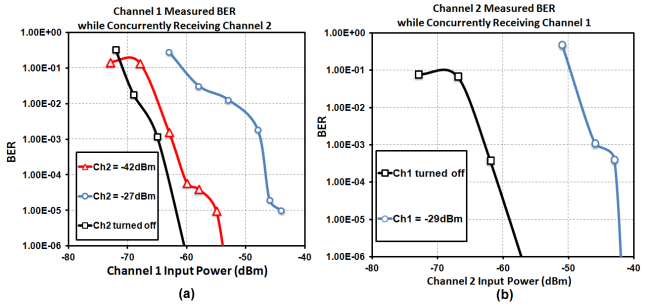


Fig. 6. (a) Measured BER of the RF channelizer receiving channel 1, while simultaneously receiving channel 2. (b) Measured BER of the RF channelizer receiving channel 2, while simultaneously receiving channel 1.

B. Fast-switching

By avoiding PLL frequency switching, rapid channel switching is enabled, and is now limited by the turn-ON/OFF times of the bias circuits in the signal path blocks which include mixers and current buffers. Based on measurements, the switching duration can be as fast as 8ns and is always lower than 1μs. A further improvement

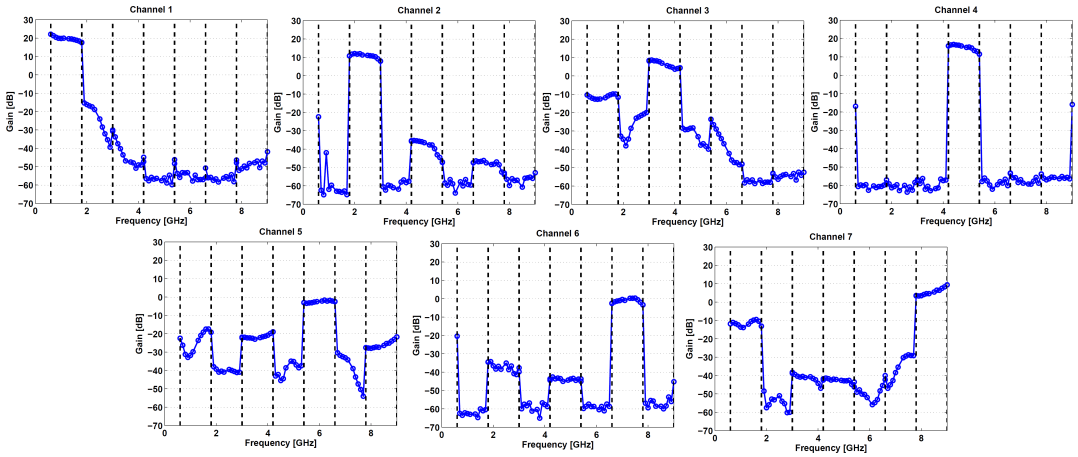
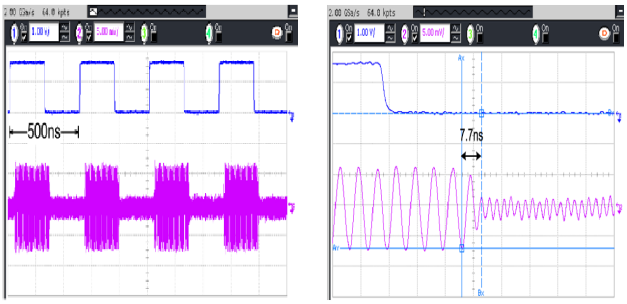


Fig. 5. Channel leakage measurements: conversion gain to each channel.

TABLE II
COMPARISON TABLE FOR STATE-OF-THE-ART RF CHANNELIZERS

Feature		[1] scanning, two-stage conversion	[2] 7 parallel receivers	[4] cascaded image reject mixers	This work partially-concurrent, fast-switching
Input BW	[GHz]	0-6	3.1-10.6	1.75-8.75	0.6-9
Power	[mW]	678[1]	342[1]	41	435
T_{hop}	[μs]	10	0.2[2]	few ns[3]	0.008-0.92
Concurrent O/Ps		1	7	1	3
No. of LO sources		2	7	1	1
IIP3	[dBm]	10	-5/-9	Not available	-3.4/-19.9
NF	[dB]	Not available	2.5/14	Not available	6.8/22.6
Signal Leakage	[dB]	Not applicable	36-70	11-37	11-63
CMOS Technology		130nm	130nm	130nm	65nm
Area	[mm x mm]	3.7x3.9	1.3x2.7	0.8x1.1	1x2

[1] Includes PLL power; [2] Estimated settling time using $\frac{1}{PLL-BW}$; [3] Data not available, estimate made from figures.



(a) (b)

Fig. 7. (a) Rapid switching between Channel 2 and 6 at output 2. (b) A closer look at the switching from Channel 2 to Channel 6.

in switching speed is possible by increasing the power consumption in bias circuits. Fig. 7 shows the results of a measurement demonstrating fast switching between Channel 2 and Channel 6.

V. CONCLUSIONS

Table II compares our RF channelizer with other state-of-art approaches to frequency channelization. The chip offers a dynamic range (computed based on IIP3 and NF) between 58dB to 63dB for various channels while consuming an average power of 435mW. It processes a very wide bandwidth while demonstrating concurrency and rapid channel switching (between 8ns and 920ns for various modes of switching). The RF channelizer was experimentally tested to support the concurrent reception of two 200Mbps BPSK data streams. Use of higher-order QAM modulations and aggregation of three concurrent outputs will result in multi-Gbps data rates.

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