A Watt-Level 2.4 GHz RF I/Q Power DAC Transmitter with Integrated Mixed-Domain FIR Filtering of Quantization Noise in 65 nm CMOS

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***Abstract* — This paper presents an S-band RF I/Q power DAC transmitter with embedded mixed-domain finite-impulse-response (FIR) filter to suppress out-of-band (OOB) quantization noise for FDD/co-existence. Watt-level output power and low output OOB noise level is achieved through (1) power combining (2) device stacking with thick oxide devices in a switching-class power amplifier (PA) and (3) embedded RF FIR filtering. To combat the strong conductance-to-amplitude/phase nonlinearity of switching-class digital PAs, a transformer-based FIR architecture is proposed that ensures completion of filtering after the nonlinearity. Implemented in 65 nm CMOS, the transmitter has a measured peak output power of 29.1 dBm with 42% system efficiency at 2.25 GHz. The measured noise floor at 100 MHz offset from the 2.4 GHz carrier is -134 dBc/Hz for a 20 MHz 64-QAM signal at 200 MSa/s including 8 dB noise floor suppression from transformer-based two-tap third-order FIR filtering, yielding an ENOB of 8.18.**

I. Introduction

The trend of CMOS scaling and demands for supporting multiple wireless communication standards have driven the investigation of highly digital RF transmitters [1]–[5]. However, these suffer from high levels of OOB quantization noise. This makes it challenging to use them in a FDD system or a co-existence environment with limited duplexer or antenna isolation. For FDD with typical commercial duplexer isolations, the transmitter OOB noise floor requirement can be as low as -160 dBc/Hz. The noise floor of digital RF transmitters can be reduced by increasing the baseband sampling frequency at the expense of higher digital power consumption or through higher resolution DACs which increases complexity and susceptibility to mismatches.

FIR-based quantization noise filtering has also been proposed to create notches in the OOB noise spectrum [6]–[8]. Authors in [6] used an FIR filtering technique with linear amplification stages at low output power levels (essentially digital modulators rather than PAs). The use of linear stages led to a low system efficiency.

In this paper, we present a digital RF transmitter which simultaneously achieves high-efficiency, watt-level output power and low OOB noise level. These are accomplished by (1) power combining (2) device stacking with thick oxide devices in a switching-class PA and (3) embedded RF filtering using a transformer-based FIR architecture to overcome the strong conductance-to-amplitude nonlinearity of switching-class PAs.

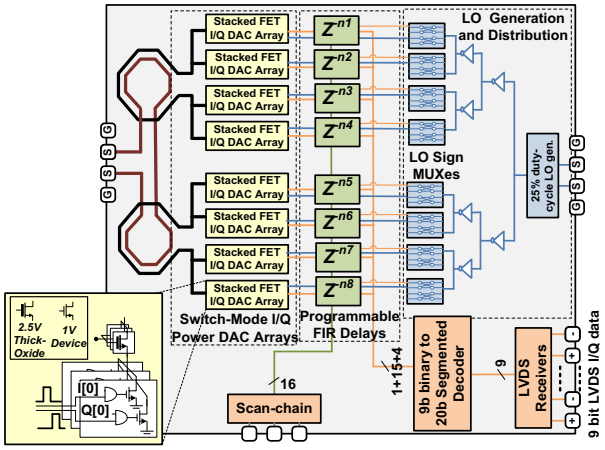


Fig. 1: Architecture of the proposed RF I/Q Power DAC transmitter with integrated quantization noise filtering.

II. Architecture

Effective quantization noise filtering by embedding FIR filters in switching-class PAs is challenging due to the strong digital control word (DCW) to amplitude/phase nonlinearity which adversely affects the filtering. Fig. 1 shows the block diagram of the proposed architecture which employs a two-tap transformer-based FIR structure to address this issue. Two differential switching-class PAs are transformer combined and drive a differential 50Ω load (Fig. 3). RF output is modulated by modulating the switch device ON conductance. The switch device of each unit PA is divided into two identical stacked FET array sections (see Fig. 1). Each array contains I and Q devices which are further sliced in an eight bit segmented fashion - four thermometer-weighted MSBs and four binary-weighted LSBs. Every slice has its own logic circuit and drivers to enable/disable them based on the DCW. The I and Q sections are driven by quadrature 25% duty-cycle LO signals which are generated on-chip from twice the LO frequency input. Negative I and Q words

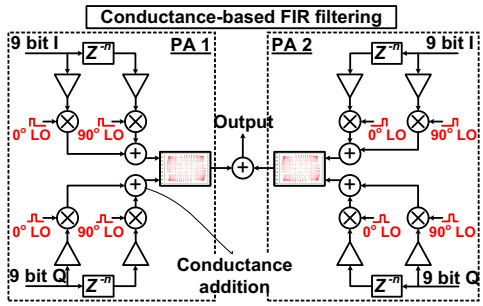
are obtained by exchanging the LO signals that go to each side of the differential circuit by means of an LO multiplexer, thus achieving a total resolution of *nine bits* in both I and Q. Each stacked FET array and LO multiplexer receives I/Q data from a programmable delay generator which retimes and delays the baseband DCWs by multiples of the sampling clock period. The programmable delay generators are designed to generate one to four sampling clock period delays based on a digital setting controlled by the scan-chain. On-chip LVDS receivers convert the received nine bit I and Q LVDS baseband data and the sampling clock to single-ended signals. This binary data is decoded by a nine-bit binary to twenty-bit segmented decoder before being routed to the programmable delay generators. There are two main configurations in which a first, second or third order two-tap FIR filter may be embedded within the transmitter as discussed below.

A. Switch Conductance-based Mixed-Domain FIR Filtering: Issues

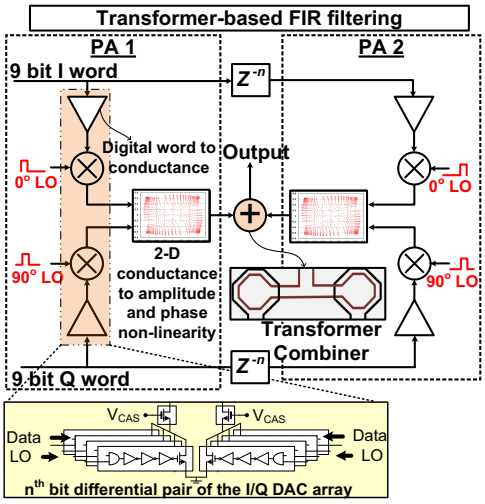
In this configuration (Fig. 2a), which is the baseline approach followed in [6], both unit PAs namely 'PA 1' and 'PA 2' are driven identically. The filtering happens in the conductances of the switch devices in each unit PA. The 'filtered conductance' undergoes a strongly nonlinear transform to output amplitude/phase which adversely affects the notch created in the filtering step. In Fig. 1, this configuration is enabled when the delays are set as - $n1 = n3 = n5 = n7$, $n2 = n4 = n6 = n8$ and $n1 \neq n2$. The transformer combiner acts as a conventional power combiner. However, unlike [6] which use linear amplification stages, here the FIR filtering is followed by a strong nonlinearity due to a switching PA implementation for high efficiency, adversely affecting the filtering.

B. Transformer-based Mixed-Domain FIR Filtering

We propose the transformer based FIR filtering configuration (Fig. 2b) in which the baseband data of PA 1 is delayed with respect to that of PA 2 and summation is performed across the transformer. Referring to Fig. 1, this configuration is enabled when the delays are set as - $n1 = n2 = n3 = n4$, $n5 = n6 = n7 = n8$ and $n1 \neq n2$. *The key insight is that the transformer participates in the FIR filtering by providing the necessary addition of delayed signals and hence, filtering is functionally completed after the conductance-to-amplitude/phase nonlinearity.* As the transformer is nominally a linear summer, the filtering quality is not impacted by the nonlinearity. The addition across the transformer is a weak nonlinearity dependent on the instantaneous difference in the DCWs that arrive at PA 1 and PA 2. Memory-based digital pre-distortion (DPD) techniques can further improve the quality of filtering by compensating for nonlinear addition.



(a)



(b)

Fig. 2: Configuration for FIR filtering through (a) addition of device conductances and (b) the proposed transformer-based FIR filtering with addition across the transformer.

In both the configurations discussed, the FIR filter notch positions may be arbitrarily set by either changing the sampling frequency or by programming the delay generators to change the filter-order.

III. Circuit Implementation

PA 1 and PA 2 are differential Class E/F_{odd} PAs [9], each delivering 500 mW to a 25Ω differential load. To support the large voltage swing, a two-stacked device configuration is used. The bottom device is a thin-oxide NMOS and the cascoded device is a thick-oxide NMOS. The cascode gate bias and device sizes ensure that the instantaneous junction potentials do not exceed twice the nominal supply voltage of that device. The width of the bottom device is 7.04 mm and the cascode device width is 21.2 mm (including differential devices of PA 1 and PA 2). The devices are driven by a cascade of three sized inverter stages followed by a NAND gate incorporating the enable logic. Zero Voltage Switching (ZVS) constraints fix the transformer winding inductance to 700 pH and

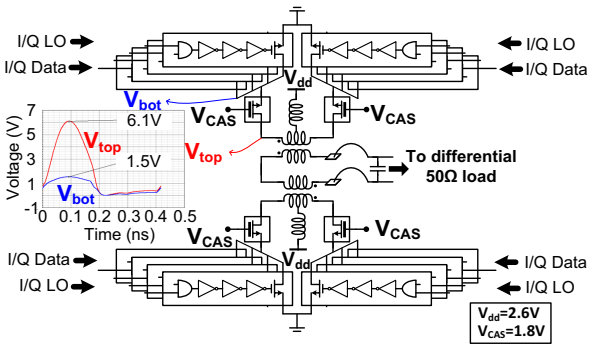


Fig. 3: Circuit diagram of the transformer combined Class E/F_{odd} digital PAs.

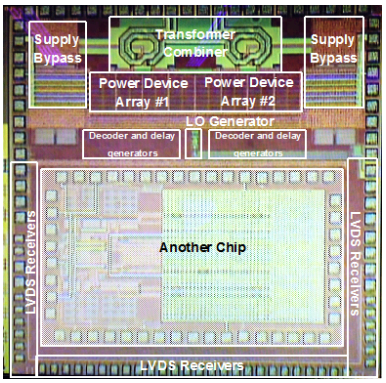


Fig. 4: Chip photograph of the transmitter.

the dc feed inductance to 200 pH. The 1:1 transformer has power combining efficiency of 62%. The matching network also provides the necessary filtering for the Class E/F$_{odd}$ operation and incorporates the output bondwire and QFN package trace. A corporate structure distributes the LO signal to all devices with minimum delay skewing.

IV. Measurement Results

The proposed transmitter is fabricated in 65 nm CMOS. The chip occupies 1.94 mm×0.8 mm excluding LVDS receivers and pads (Fig. 4). The LVDS baseband I/Q signals and the sampling clock are provided by an FPGA.

Fig. 5 shows the peak output power and efficiency of the transmitter across frequency. Here, the input I and Q DCWs were held constant at their peak positive values (255) while the LO frequency was swept. Peak output power of 29.1 dBm at 42% system efficiency is measured at 2.25 GHz. Fig. 6 shows the output power and efficiency versus backoff (I=Q) of the transmitter with optimized bias at 2.4 GHz. A peak output power of 29.9 dBm with 38% system efficiency is measured for the highest DCW at this frequency. The efficiency under back-off profile (Fig. 6b) follows that of a class-B PA.

Fig. 7 shows the constellation plot that results from a

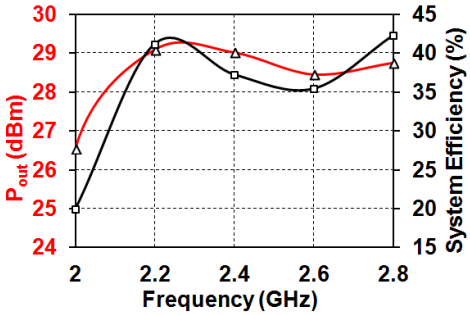
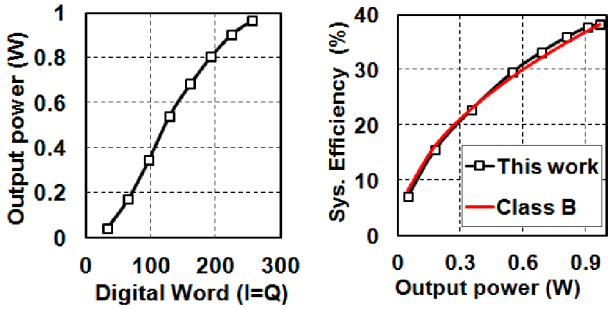


Fig. 5: Peak output power and efficiency across frequency of the transmitter. Main V_{dd} = 2.6V, Driver V_{dd} = 1.2V



(a) (b)

Fig. 6: (a) Output power vs. DCW for I=Q and (b) resultant system efficiency under back-off at 2.4 GHz. Main PA V_{dd} = 2.8V, Driver PA V_{dd} = 1.3V.

static measurement across equally spaced I/Q DCWs. The transmitter's output is downconverted to baseband I and Q signals using a vector signal analyzer. The plot shows the presence of significant AM-AM and AM-PM (conductance to amplitude/phase) nonlinearity for both I and Q. Two-dimensional 32×32 DPD LUTs are constructed which are used to generate predistorted 64-QAM baseband data with a bandwidth of 20 MHz and 200 MSps (limited by signal generation setup). Fig. 8 illustrates the effect of DPD on the output power spectral density (PSD). An improved DPD of the baseband signal yielded a -20 dB EVM. The noise-floor at 100 MHz offset from the 2.4 GHz carrier is -126 dBc/Hz with DPD and no filtering employed. The average output power is 18.75 dBm (due to operation at 3.6 dB backoff) at a system efficiency of 14.4%. *The implementation of FIR filtering features has virtually no impact on average efficiency.* Fig. 8 also shows the PSD of the transmitter configured as a third-order filter with the transformer-based FIR filtering option. The noise floor at 100 MHz offset from the carrier is seen to be -134 dBc/Hz - an 8 dB improvement over the case where no filtering is employed. Measurements with 5-6 times higher sampling rates (1 GSps) to further reduce the noise floor are underway. We expect that with the PA operated at peak power and at 1 GSps (5×200 MHz) the noise level

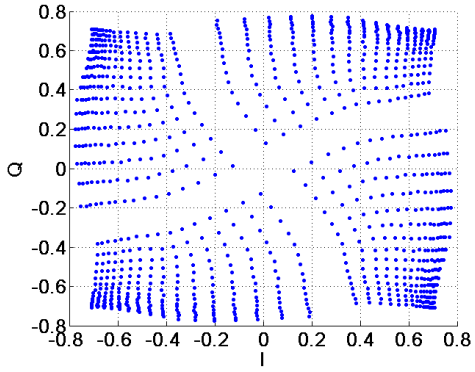


Fig. 7: The two dimensional nonlinearity constellation obtained for equally spaced values of I and Q. Only 32×32 points are shown here.

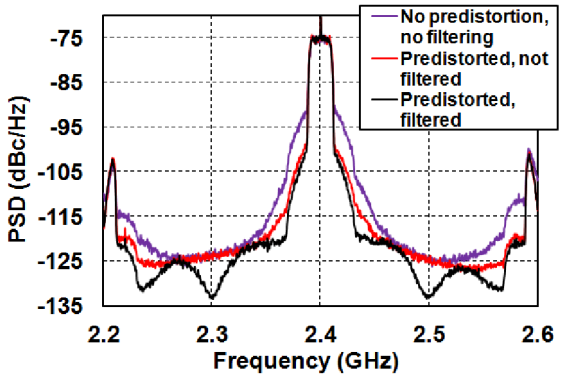


Fig. 8: PSD of the output of the transmitter normalized to total signal power showing the effect of 2D I/Q DPD and third-order two-tap transformer-based FIR filtering.

will reach -145 dBc/Hz. This means that an additional 2.5 bits of effective resolution enables digital transmitters to approach the OOB noise level required for FDD systems. Memory-based DPD to compensate for the weak residual nonlinearity in transformer-based filtering is ongoing and will further improve notch depth.

Table I summarizes the important performance metrics of fully integrated RF transmitters which include on-chip (phase/amplitude or I/Q) modulation circuits. The effective number of bits (ENOB) is calculated using,

$$SQNR = 6.02 \times ENOB + 4.77 + 10.\log(f_{samp}/2),$$

where the signal-to-quantization-noise ratio (SQNR) is defined as the ratio of the signal power to noise floor at 100 MHz offset from the carrier [6]. The implemented prototype achieves the highest peak output power and ENOB for the same modulation bandwidth.

V. Conclusion

A fully integrated watt-level high-efficiency digital RF transmitter with embedded quantization noise filtering has been demonstrated. An effective technique to overcome the output side nonlinearity limitation for FIR filtering in switching class PAs has also been shown. The implemented prototype is a step towards making RF power DACs a viable option for FDD/co-existence.

TABLE I: Comparison of State-of-the-art Fully Integrated Digital RF Transmitters

Reference	[2]	[5]	**This Work**
Technology	65nm CMOS	40nm CMOS	**65nm CMOS**
Frequency	2.2 GHz	2.44 GHz	**2.4 GHz**
Resolution	8 amplitude, 9 phase bits	13 I/Q bits	**9 I/Q bits**
Sampling rate	1 GSps	800 MSps	**200 MSps**
Peak power	23.3 dBm	24.7 dBm	**29.9 dBm**
Peak efficiency	43%	37%	**38.3%**
Avg. power	16.8 dBm	18.8 dBm	**18.75 dBm**[3]
Avg. efficiency	19.3%	17%	**14.4%**[2]
Modulation format	802.11g 64 QAM	802.11g 64 QAM	**64 QAM**
PAPR	6.5 dB	5.9 dB	**7.5 dB**
Bandwidth	20 MHz	20 MHz	**20 MHz**
Noise floor at 100 MHz offset	-135.8 dBc/Hz	-133.7 dBc/Hz	**-134 dBc/Hz**[1]
ENOB	7.32	7.13	**8.18**

1) With two-tap third-order transformer-based filtering. 2) Includes power consumption of all blocks except LVDS receivers. 3) PA is operated at 3.6 dB backoff power level.

Acknowledgments

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