A 200GHz Power Mixer in 130nm-CMOS Employing Nonlinearity Engineering

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***Abstract* — CMOS high-mmWave/sub-mmWave sources leverage device nonlinearity, either in oscillators or frequency multipliers, to generate harmonics beyond the technology f_{max}. We propose a power mixer topology that exploits nonlinearity engineering to enhance the output harmonic content. By engineering the amplitude and phase of the fundamental and second-harmonic content in the mixer device voltage waveforms, the output third harmonic power is enhanced significantly beyond that achievable in conventional frequency triplers. A 200GHz power mixer in 130nm CMOS generates 50μW of output power at a frequency $1.5\times$ higher than f_{max}.**

***Index Terms* — CMOS, frequency multipliers, mm-wave.**

I. Introduction

Scaled CMOS nodes (130nm-45nm) have maximum frequencies of oscillation (f_{max}) and cutoff frequencies (f_T) from 130-300GHz and 90-200GHz respectively. Consequently, signal generation in CMOS in the high millimeter-wave (mmWave) (150-300GHz) and the sub-mmWave (>300GHz) frequency ranges requires use of device nonlinearity to generate harmonics of the fundamental, either in oscillators [1]-[3] or in frequency multipliers [4]-[7].

We propose a *nonlinearity-engineered* power mixer topology which generates the third harmonic by mixing the input fundamental with it's second harmonic. By engineering the amplitudes and relative phase shift of the inputs, a larger swing can be sustained at the device nodes for a given breakdown voltage. The relative phase shift also allows us to alter the large signal region of operation of the device and optimize inherent device nonlinearity. Our proposed topology can generate upto $9\times$ more third harmonic power from the same device than a conventional frequency tripler. While the discussion is in the context of the third harmonic, the idea can be extended to other output harmonics.

II. mmWave/Thz Power Generation Challenges

Recently in [6], the authors investigate limits on output power in conventional frequency multipliers. Output power is determined by the device harmonic current and output load resistance. For high mm-wave range, the optimal load for a given device size is dominated by the equivalent parallel resistance of the substrate in bulk CMOS. The magnitude of harmonic current is limited by the maximum input voltage swing (subject to breakdown limits) and input duty cycle. For these conditions, it was shown that to first order in frequency doublers [6], the power delivered to 50Ω without impedance transformation is

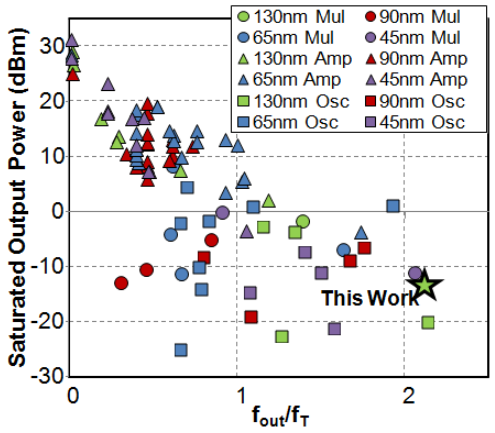

Fig. 1. Comparison of our work with state-of-the-art CMOS signal sources across output frequency normalized to technology f_T.

$$P_{out} = \frac{F_2^2}{100\Omega}\left(\frac{C_{in}}{C_{out}} \times \frac{C_{sb}}{C_{db}}\right)^2 (V_{dd} - V_{th})^2 \frac{\left(\frac{f_T}{f_{out}}\right)^2}{1 + \frac{f_{out}^2}{f_{NQS}^2}} \quad (1)$$

where F_2 is the ratio of the 2nd harmonic current (at f_{out}) to the peak of the clipped sinusoidal output current, $C_{in} = C_{gs} + C_{gd}$, $C_{out} = (C_{db}C_{sb})/(C_{db} + C_{sb})$. f_{NQS} is a pole associated with the finite time for channel charge build-up at high frequencies (Non-Quasi-Static or NQS effect). From this equation, ignoring NQS, output power across frequency normalized to f_T emerges as a relevant metric to compare performance of frequency multipliers across technology, Fig. 1. Further, it shows that nonlinearity engineering that enhances harmonic content of output current (captured by F_2) is an interesting topic for investigation.

For frequency multipliers, the authors of [4] and [5], study altering the duty cycle of a fundamental input on harmonic current in common source configuration. For oscillators, the authors [3] study the impact of relative phase of the gate and drain voltage of the oscillator device on the fundamental swing generating harmonic current through device nonlinearity. In [1], the authors maximize output second harmonic power of an oscillator designed for maximum startup gain by transforming 50Ω to an optimal

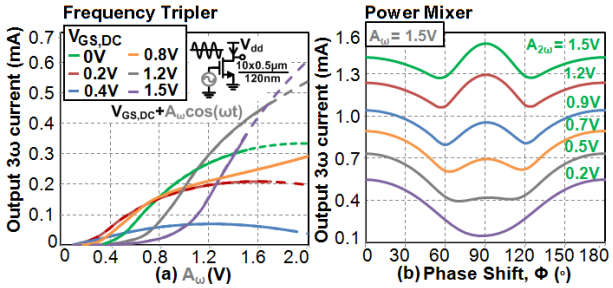

Fig. 2. Third harmonic current (a) as a function of fundamental amplitude and gate bias voltage in a conventional frequency tripler for a $\frac{10\times0.5\mu}{120nm}$ device. (b) as a function of second-harmonic amplitude $A_{2\omega}$ and relative phase ϕ between the fundamental and second-harmonic drive in $\frac{10\times0.5\mu}{120nm}$ power mixer. A_ω=1.5V

load. However, *engineering the harmonics in the gate-source voltage of a power device* at mmWave and THz frequencies for enhanced output power remains a topic of interest with potentially significant benefits.

III. Power Mixer With Nonlinearity Engineering

In a conventional frequency tripler, a fundamental signal is fed at the device gate (inset in Fig. 2(a)). Harmonic traps (not shown) at the gate force the second and third harmonic voltages (fed back through C_{gd}) at the gate to zero. This suppresses harmonic currents generated by harmonic voltages at the gate which are detrimental to output power, [4]. The drain voltage swings only at the desired (third) harmonic frequency due to the use of multiple phases that cancel the fundamental and second harmonic (not shown here). Previous works explored the effect of duty cycle on output power [4] and [5]. The device duty cycle is a function of the gate bias $V_{GS,DC}$ and the input amplitude A_ω. In Fig. 2(a), we plot the simulated third harmonic current for different combinations of bias and amplitude. For any bias $V_{GS,DC}$, the harmonic current increases with increasing input amplitude. The maximum amplitude that can be applied for a $V_{GS,DC}$ is limited by the breakdown condition such that the voltage difference between any two nodes cannot exceed $2\times V_{dd}$ =3V. In the positive half cycle, V_{gs} breakdown limits the input swing and V_{gd} breakdown limits the swing in the negative half cycle. The limitation on amplitude is shown in Fig. 2(a) by the dashed line. We see that the breakdown condition limits the maximum third harmonic current from a $\frac{10\times0.5\mu}{120nm}$ device to about 450μA.

Using the same device as a mixer to multiply second harmonic and fundamental signal is attractive as a more powerful second-order nonlinearity will generate third harmonic current. To provide good isolation between the two, second harmonic is fed at the gate and fundamental at the source (Fig. 3(a)). The impedance at the source is of the order of $1/g_m$ and is much lower than gate impedance, implying higher drive power at the source for the same

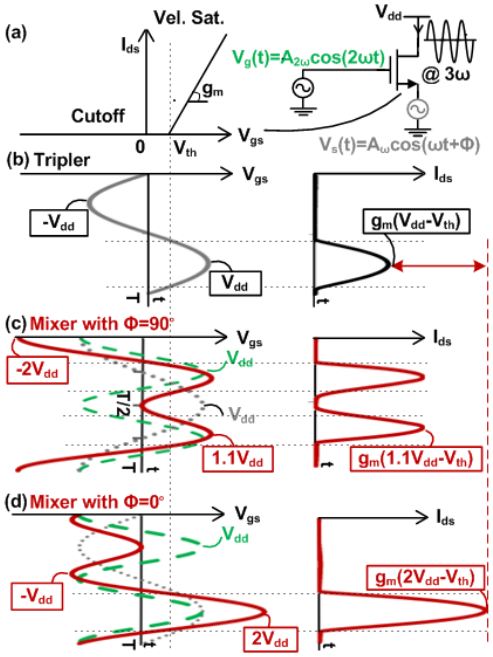

Fig. 3. (a) Power mixer configuration and piece-wise linear current model. (b) Maximum fundamental gate drive and device current in a tripler biased at 0V. Gate-source voltage and current in a power mixer for $A_{2\omega}$=A_ω=1.5V and (c) $\phi = 90°$, (d) $\phi = 0°$.

swing. Power at fundamental is more readily generated than at second harmonic, so the latter is fed at the gate.

Initially, consider a power mixer biased at 0V at gate and source. If the drain swing is small, so that the drain can be assumed fixed at V_{dd}, the V_{gd} and V_{ds} breakdown conditions set a maximum limit on $A_{2\omega}$ and A_ω to V_{dd}. With these amplitudes, the phase of the fundamental input relative to the second harmonic, ϕ, dictates the limits of the V_{gs} swing. The $1:2$ relationship between the input harmonics means that only values of $0°$ to $180°$ need be considered for ϕ. Changing ϕ allows us to alter the large signal region of operation of the device and optimize inherent device nonlinearity. The V_{gs} waveform for $\phi = 0°$ has a maximum of $2V_{dd}$ while $\phi = 90°$ has a minimum of $-2V_{dd}$ (Figs. 3(c), (d)). All other ϕ result in a V_{gs} swing within $-2V_{DD}$ to $2V_{DD}$. Fig. 3 also shows the device current for both cases as well as a frequency tripler biased at 0V and input voltage pushed to the breakdown limit. A piecewise linear model is assumed for the device current that ignores dependance on drain voltage due to channel length modulation or triode (Fig. 3(a)). $\phi = 0°$ results in a current with a high peak value (significantly higher than that of the tripler), while $\phi = 90°$ results in a current with high third harmonic content relative to its peak.

As both peak current and relative third harmonic content are significant, Fig. 2(b) depicts the simulated absolute third harmonic output current of a $\frac{10\times0.5\mu}{120nm}$ device as a function of relative phase ϕ, as well as $A_{2\omega}$ for $A_\omega = 1.5$V.

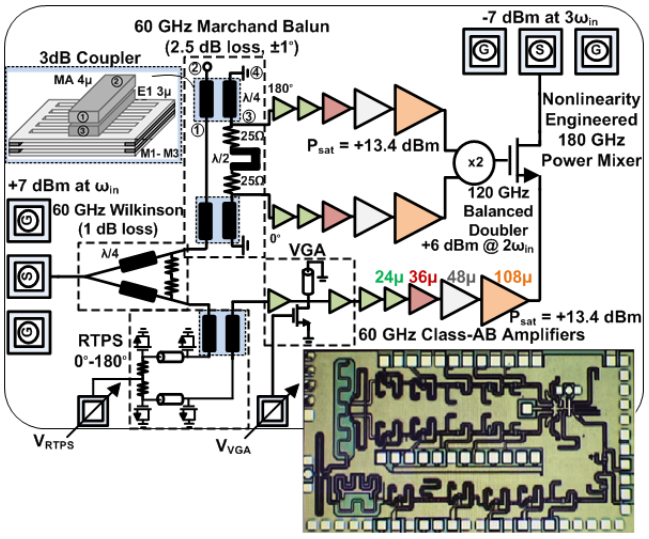

Fig. 4. Block diagram of the implemented 200GHz output frequency, 2.5mm×1.4mm power mixer in 130nm CMOS.

When $A_{2\omega} = 1.5$V, the optimal phase is $90°$ and the third harmonic current is 1.5mA ($3\times$ higher than a frequency tripler). This corresponds to $9\times$ higher output power as the optimal load is only determined by device size (via the substrate network). However, generation of $A_{2\omega} = 1.5$V swing at 2ω ≈130GHz in 130nm CMOS is challenging. The implemented prototype in simulation achieves $A_{2\omega}$=0.7V, for which $\phi = 0°$ is optimal and the output third harmonic current is $2\times$ higher than a tripler ($4\times$ higher power).

The simulations above ignore the NQS effect. This will not change the conclusions at high frequencies as NQS causes a roll-off in the harmonic current of both circuits.

IV. A 200GHz Power Mixer in 130nm CMOS

A block diagram of the implemented power mixer with 189GHz output (originally designed for 180GHz) is in Fig. 4 along with simulated performance numbers. The power mixer is implemented in 130nm CMOS (f_{max} ≈130GHz). The second harmonic signal feeding the gate is generated on-chip by a balanced frequency doubler [6]. The input 60 GHz is split by a Wilkinson divider. One output feeds a Marchand balun which drives two Class AB V-Band amplifier chains. These provide the differential input swing required by the balanced doubler. In frequency multipliers, and indeed in the power mixer as well, significant fundamental power is needed to produce large input swings. To mitigate the fundamental power generation challenge, two-way device stacking is employed in the amplifiers to enable operation from a 3V supply and increase output power to 50Ω. The first four stages are conjugate matched for maximum gain. The last stage is designed for output power and efficiency(Fig. 5(a)). The amplifier chain has a simulated small-signal gain of 21dB, 13.4dBm saturated

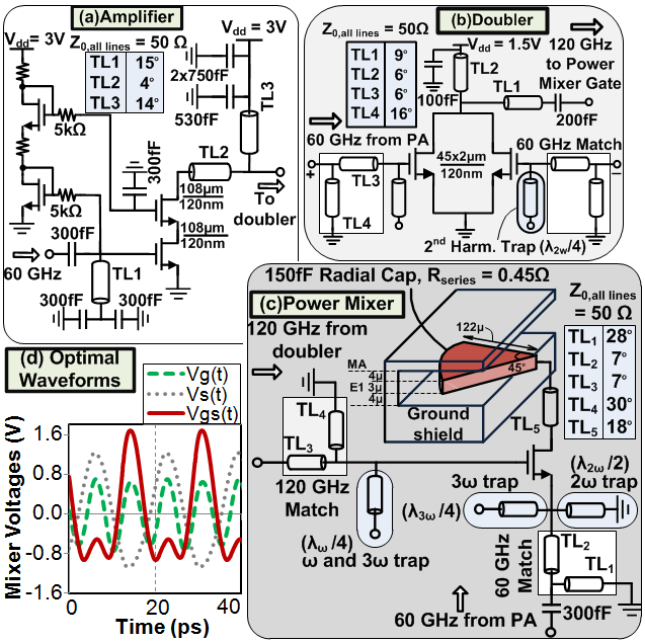

Fig. 5. Circuit diagrams of (a) last stage of V-band amplifier chain, (b) balanced frequency doubler, (c) power mixer. (d) Simulated device voltage waveforms for power mixer at the optimal phase-shift $\phi = 0°$ (with V_{RTPS} =0.3V). $A_{2\omega}$=0.7V and A_ω =1.5V.

output power and 6.8% drain efficiency at 60GHz. The circuit of the doubler is in Fig.5(b). A breakout of the doubler and its driver shows an output power of +4.2dBm at 134GHz when its driver amplifiers saturate [6].

The Marchand balun uses 3dB coupled line couplers with 50Ω characteristic impedance and balun output impedance of 25Ω. For output matching and isolation two 25Ω resistors and a $\lambda/2$ line are placed between outputs, [8]. Without this, the output isolation is 6dB. The network adds $180°$ phase shifted path with 6dB attenuation between outputs to improve isolation. The simulated input and output match is 15 dB and the isolation of balanced ports is 22 dB from 50−70GHz. The 3dB coupler has two broadside coupled $\mu-$trip lines in the top metals, MA and $E1$. Even mode impedance of 120Ω was achieved by slow-wave technique by opening 60μm long and 10μm wide slots in the ground plane. Odd mode (21Ω) confines the signal between $\mu-$strips.

The other Wilkinson output feeds an identical amplifier chain to provide fundamental signal at the power mixer's source. To alter the relative phase shift of the two harmonic paths a reflection-type phase shifter (RTPS) [9] with CLC termination is used. As noted in Sec. III, a $1:2$ ratio of harmonics implies the RTPS must have a range of $0° - 180°$. To compensate for its loss, a reflection-type attenuator is placed between two amplifier stages as a variable gain amplifier (VGA) with 7dB to 0.6dB gain for $V_{VGA} = 0$V to 1.5V respectively. This ensures constant fundamental swing at the mixer source across phase settings.

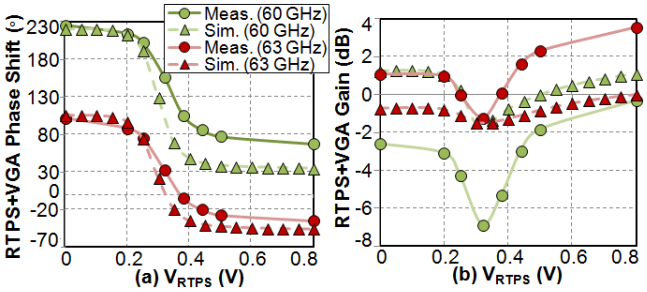

Fig. 6. Measured and simulated (a) phase shift and (b) gain of the RTPS-VGA test structure with VGA on maximum gain setting.

The circuit diagram of the implemented power mixer is in Fig. 5(c). In addition to the desired second harmonic, first and third harmonic current can feed back through C_{gd} and generate first and third harmonic voltages at the gate. At the source, apart from the desired fundamental swing, second and third harmonic voltages can appear when harmonic currents from the transconductance flow into the source impedance. The additional swings generate harmonic currents through the transconductance that are detrimental to desired output power. To mitigate this, harmonic traps are added at the gate and source similar to conventional frequency multipliers [4]. To mitigate loss in the capacitive bypass at the end of shorted lines in the matching networks, the gate and source are biased at 0V. At the drain, device capacitance is resonated at 180GHz. The output bypass (150fF) is by a *Radial Stub* (series resistance, $R_{series} = 0.45\Omega$) in layer $E1$ sandwiched in the ground plane to avoid loss in an equivalent Metal-Insulator-Metal capacitance ($R_{series} = 3\Omega$). The drain bias is provided through the bias-T of the output probe. To maximize power delivered at 180GHz, the output 50Ω is transformed to 25Ω and the mixer device size is chosen accordingly.

V. Measurement Results

A breakout of the RTPS-VGA cascade is measured with an Anritsu VNA. The performance across RTPS control (V_{RTPS}) with VGA at maximum gain is in Fig. 6.

The power mixer is measured using an Anritsu DC-67GHz signal generator followed by a Quinstar PA at the input and a WR-5 2^{nd}-harmonic Millitech mixer down-converter at the output. The saturated output power across output frequency is in Fig. 7(a). A peak power of -13dBm is seen at 189GHz. Here, the VGA was at maximum gain and the V_{RTPS} was at the optimum 0.3V. Fig. 7(b) shows variation in saturated output power with V_{RTPS} at 189GHz. In simulation, swings of $A_{2\omega} = 0.7$V and $A_{\omega} = 1.5$V are seen at the power mixer irrespective of RTPS setting. For these swings, a relative phase of $\phi = 0°$ is theoretically optimal (Fig. 2(b)). Indeed, V_{RTPS}=0.3V (seen to be optimal in simulation) yields 0° at the mixer (waveforms in Fig. 5(d)). In measurement as well, peak

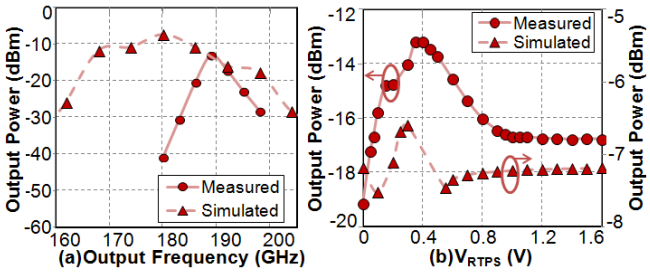

Fig. 7. (a) Saturated output power across output frequency. $P_{\text{in,meas.}} = 11$dBm and $P_{\text{in,sim.}} = 7$dBm. VGA is at maximum gain, V_{RTPS}=0.3V (optimal). (b) Variation in output power at 189GHz with V_{RTPS}. Simulations are at nominal value of 180GHz.

output power is achieved at V_{RTPS}=0.3V and the nature of the variation closely matches simulation.

The total DC power is dominated by driver amplifiers consuming ≈ 300mW in each chain while the doubler and power mixer consume only 24mW.

Fig. 1 in Section II compares the measured output power across normalized output frequency. When compared with other 130nm CMOS works at this frequency, the implemented power mixer achieves 7dB higher output power.

VI. Conclusion

A 200GHz power mixer that exploits nonlinearity engineering to enhance the output harmonic content and generates 50μW of output power was demonstrated in 130nm CMOS ($f_{max} = 130$GHz). While the techniques presented were for third harmonic generation, the idea can be extended to other output harmonics.

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