An RF Instantaneous-Hop Frequency Synthesizer based on a Zero-Initial-Phase-Error Multi-Modulus Divider

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***Abstract* — In this paper, we propose an instantaneous-hop frequency synthesizer based on a zero-initial-phase-error multi-modulus divider that breaks the fundamental trade-off between hopping time, spectral purity and frequency resolution. In the proposed synthesizer, initial frequency error and phase error at the instant of hop are virtually eliminated through frequency presetting in the high-resolution voltage-controlled oscillator (VCO) and the proposed zero-initial-phase-error divider. This eliminates the acquisition process and enables "instantaneous hops" to within a frequency error that is only limited by the resolution of digital control. An IC prototype is implemented and fabricated in a standard 65nm CMOS technology. The implemented frequency synthesizer operates over 4-5.84 GHz with three discrete divider ratios (80,88,96) and achieves instantaneous hops to within an average of 3.64 MHz of the desired output frequency. The prototype dissipates 16.8 mW from 1.2V power supply.**

***Index Terms* — Phase locked loops, Digital-controlled oscillators**

I. Introduction

Fast-hopping frequency synthesizers are useful in several applications. A fast-hopping synthesizer enables rapid and energy-efficient spectrum analysis in emerging cognitive radios [1]. Military receivers employ fast frequency-hopping as an electronic protection against jammers [2]. Multiband orthogonal frequency division multiplexing (MB-OFDM) communication systems have been proposed for high data-rate wireless communication in the 3-10 GHz ultra-wide-band (UWB) spectrum [3]. OFDM and fast frequency hopping together provide interference immunity, reduced multi-path fading and multiple access.

Conventional phase-locked-loop (PLL) based frequency synthesizers trade-off loop bandwidth, settling time, noise, spurs and frequency resolution [4]. Prior works seek to expedite the locking process of the PLL. The works in [5], [6], [7] effectively vary bandwidth, mode, and type of PLL respectively between transient locking and steady-state operation to mitigate the bandwidth versus settling time trade-off in type-II integer-N PLLs. [8] utilizes a pre-determined look-up table (LUT) to preset the digital control word (DCW) of the VCO in the PLL. This reduces the initial VCO frequency error, but the potentially harmful initial phase error induced by the divider is not addressed.

We propose a PLL where initial frequency and phase error at the hop instant are eliminated through digitally-intensive initial-condition control. This eliminates acquisition and enables "instantaneous hops" to within a frequency error limited only by the DCW resolution.

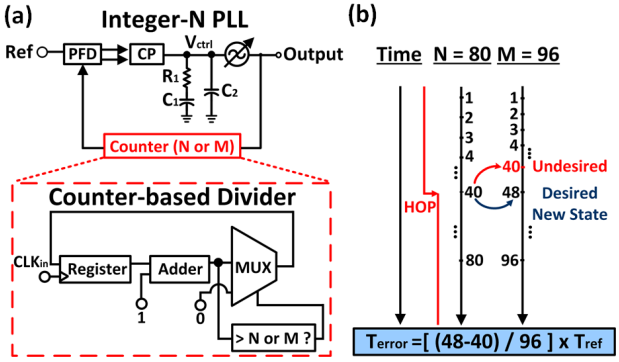

Fig. 1. (a) PLL with a binary-sequence counter-based divider. (b) Mechanism of initial phase error in the counter-based divider.

II. Zero-Initial-Phase-Error Multi-Modulus Divider

The conventional integer-N charge-pump PLL (shown in Fig. 1(a)) is a nonlinear dynamical feedback system characterized by its state variables. Specifying the values of all state variables completely defines the system's state. An LC-VCO based charge-pump PLL is a mixed-mode system whose state variables include inductor current and capacitor voltage in the VCO, the control voltage across the loop filter's capacitor, and the state of the digital divider (which is essentially a digital finite-state-machine (FSM) counter). Initial conditions are critical in the transient response of such systems. *We propose the assignment of initial conditions to each state variable in the system at the hop instant through extensive digital control and calibration to essentially hop to a locked state.*

The digital divider is essentially a counter with a programmable terminal count. Fig. 1(b) shows the transient behavior of a conventional binary-sequence counter-based divider at the frequency hop instant. If the terminal count is set to either $M = 80$ or $N = 96$ at the hop instant, the counter induces an initial phase error to the reference signal if its original state (count 40 here) is maintained. Typical multi-modulus dividers use pulse-swallow counters or cascaded divide-by-2/3 structures, which have their

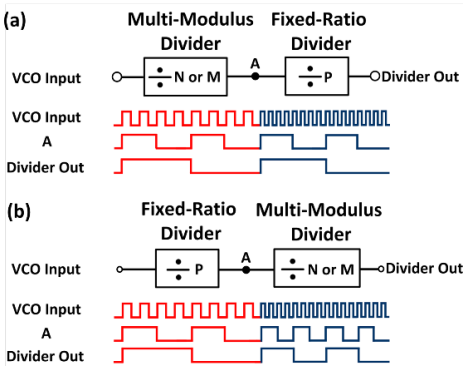

Fig. 2. (a) Multi-modulus divider first: no initial state control is necessary in the fixed-ratio divider that follows. (b) Fixed-ratio divider first: initial state control is required throughout the chain.

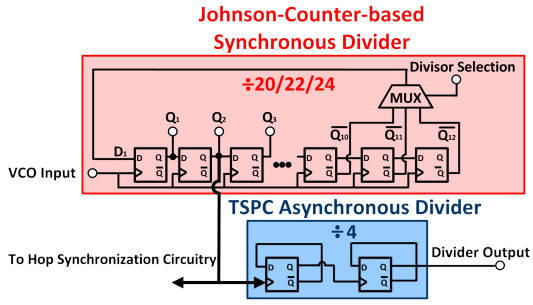

Fig. 3. Proposed zero-initial-phase-error divider structure.

own state-machine descriptions and so, initial-phase-error mechanisms. These initial phase errors can be eliminated by reconfiguring the state of the FSM at the hop instant.

To implement a divider with initial-state control, two aspects must be addressed. First, as in Fig. 2, assuming the divider chain has multi-modulus and fixed-ratio dividers, one aspect is if the multi-modulus divider should be at the input or at the output of the divider chain. If zero initial phase error is achieved, this means that after reconfiguration of the divider modulus at the hop instant, the divider output is unchanged and perfectly aligned to the reference. Placing the multi-modulus divider at the front of the chain implies no initial-state control is necessary in the fixed ratio dividers that follow (Fig. 2(a)), easing the digital control that is exercised at the hop instant.

A second aspect is if the front-side multi-modulus divider should be synchronous or asynchronous. Asynchronous dividers are generally used as reduction in clock frequency down the chain reduces dynamic power consumption. In such chains the sub-dividers at different clock frequencies are mutually skewed due to divider delays. This makes initial-state control and even defining a state fundamentally problematic. Thus, to enable instantaneous hops, the multi-modulus divider must be synchronous at the cost of slightly higher power consumption. The following fixed-ratio divider can be asynchronous.

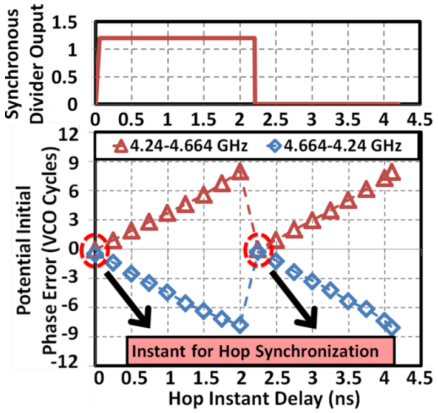

Fig. 4. Potential initial phase error in the proposed divider structure for upward and downward hops.

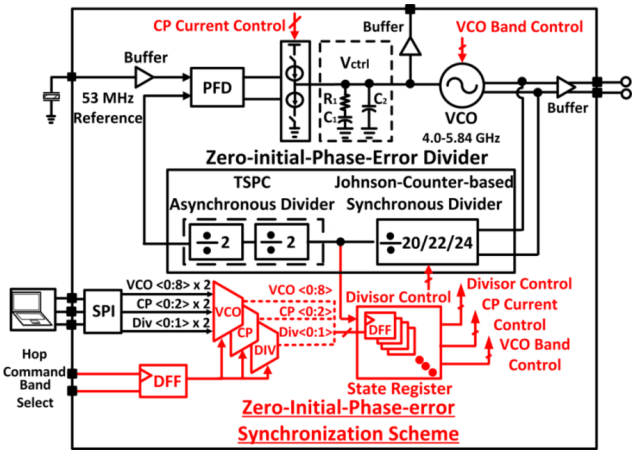

Fig. 5. 4.0-5.84 GHz instantaneous-Hop PLL block diagram.

With these considerations, we propose a zero-initial-phase-error divider shown in Fig. 3 with a synchronous divide-by-20/22/24 Johnson-counter divider followed by asynchronous flip-flop-based divide-by-2 dividers. The multi-modulus nature of the Johnson-counter dividers is from the 3-1 multiplexer (MUX) that controls feedback. As shown in Fig. 4, in the absence of state reconfiguration at the hop instant, the initial phase error accumulates throughout the period of the synchronous divider output and resets to zero at each rising/falling edge. Thus, if the hop instant is synchronized with the rising edge of the synchronous divider output, initial phase error is eliminated without extensive digital controls. The delay induced by this synchronization will be less than one period of synchronous divider output ($\sim$ 4.7ns in this prototype).

III. 4.0-5.84 GHz Instantaneous-Hop PLL

A type-II third-order charge-pump PLL (Fig. 5) forms the core of the proposed synthesizer. The PLL has an LC-VCO operating over 4.0-5.84 GHz which is tuned with an accumulation-mode varactor and a high-resolution 9-bit DCW (Fig. 7), and the programmable 80/88/96

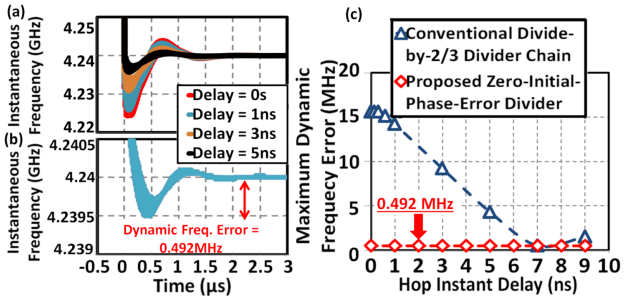

Fig. 6. Instantaneous frequency versus time for different hop instants in (a) a conventional PLL using divide-by-2/3 asynchronous dividers, (b) proposed instantaneous-hop PLL. (c) Maximum dynamic frequency error versus hop instant in both cases.

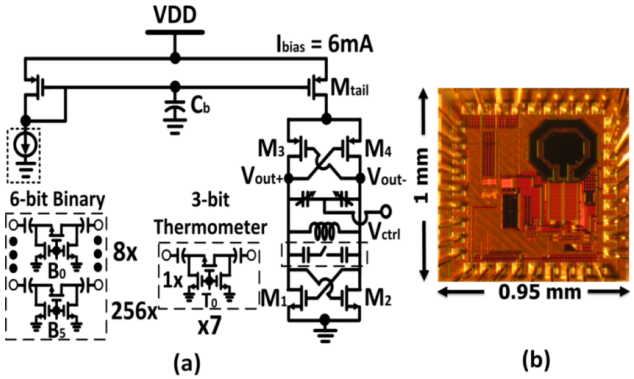

Fig. 7. (a) 4.0-5.84 GHz 9-bit digitally-controlled LC-VCO with analog varactor tuning. (b) Chip microphotograph.

divider chain described earlier (Fig. 3). A 53 MHz off-chip crystal oscillator enables locking of the PLL to 4.24, 4.664 and 5.088 GHz with division ratios of 80, 88 and 96 respectively. A conventional tri-state phase-frequency detector (PFD) and passive loop filter are integrated on chip. The loop parameters are designed for a bandwidth of 800 kHz and phase margin of 45°. Loop filter capacitor C_1, C_2 are 35 and 5 pF respectively, R_1 is 6kΩ.

As described earlier, for zero initial phase error, the hop instant must be synchronized with the rising edge of the synchronous divider output. In addition to state variables, the charge pump current is also reprogrammed at the hop instant to maintain constant loop bandwidth due to varying K_{VCO} gain. Note that the charge pump current is not a PLL state variable and does not contribute to initial condition errors. In this prototype, an on-chip state register stores the DCW of 9-bit VCO, divider ratio control and charge pump current control. A second on-chip memory with a serial interface (SPI) stores the settings for the different frequencies between which the PLL hops (limited to two in this prototype). The externally-applied hop signal clocks a flip-flop that registers the externally-applied 1-bit band select signal. This flip-flop then selects the settings of one of the two possible output frequencies for loading into the state register which is clocked by the synchronous divider output to ensure hopping at its rising edge.

Other initial conditions include V_{ctrl}, the inductor current and capacitor voltage of the VCO. The DCW of 9-bit VCO ensures that the VCO can be programmed to lock with V_{ctrl} close to $V_{dd}/2$ for any output frequency. Choosing the initial DCW prior to hop appropriately could eliminate the need for setting V_{ctrl}. Controlling the initial inductor current and capacitor voltage in the VCO is challenging as they are analog signals. However, as the division ratios are large, the impact of not controlling them is small. The residual errors due to finite DCW resolution, initial phase errors in the VCO due to the LC state variables and delays in the digital control path will settle at a rate determined by the loop bandwidth and their magnitude will determine the dynamic frequency error during settling. The prototype has been designed to achieve an extremely low dynamic frequency error of 3.64 MHz on an average (dominated by DCW resolution), significantly lower than the varactor tuning range. The frequency drift of the VCO due to process, voltage, and temperature (PVT) variations can be tackled by periodic calibration [9]. Increasing the resolution of the initial condition digital control can lead to even lower dynamic frequency errors.

To show the benefit of this architecture, Verilog-AMS models are simulated for the proposed divider and a conventional cascaded asynchronous divide-by-2/3 divider chain (with realistic divider delays). A Verilog-AMS VCO model is built with a tuning curve fit to measurements. The PFD is modeled in Verilog-AMS while charge-pump is at the transistor-level. Fig. 6 shows the simulated settling behavior for a hop from 4.664 to 4.24 GHz. Frequency presetting is done in both cases while the external hop signal is varied in time over one reference cycle. The proposed divider eliminates initial phase error, and thus minimizes V_{ctrl} overshoots and dynamic phase error by 1-2 orders of magnitude during settling.

IV. Measurement Result

A 65nm CMOS prototype was fabricated with 0.95 mm^2 chip-area, Fig. 7(b). It draws 14 mA current from a 1.2V supply. The measured tuning range of the VCO is 4.0-5.84 GHz. Fig. 8(a)-(d) shows the VCO's frequency, K_{VCO}, frequency-difference between two successive DCW values at mid-V_{ctrl}(0.6V), and single-band frequency tuning range across all DCW. With these, a DCW for any desired output frequency placing the required V_{ctrl} near mid-VDD with residual initial frequency error less than 3.64 MHz on an average can be found.

Fig. 9 shows the hopping behavior. To monitor hopping, the V_{ctrl} node is noted with a unity-gain buffer. The PLL output is also quadrature-downconverted and captured on an oscilloscope to determine the instantaneous frequency.

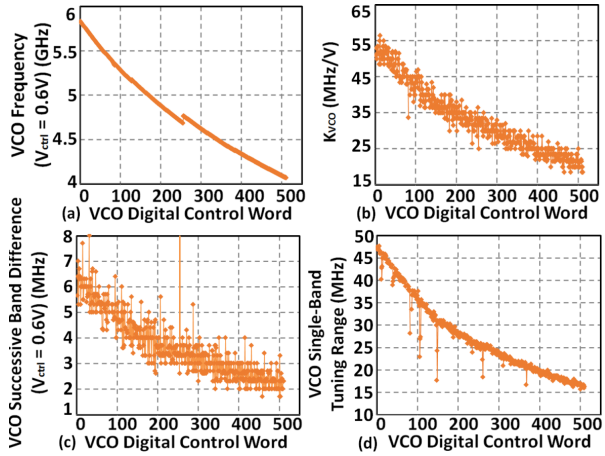

Fig. 8. Measured 4.0-5.84 GHz 9-bit LC-VCO performance at V_{ctrl} = 0.6V versus DCW: (a) frequency (b) K_{VCO} (c) frequency difference between two successive DCW (d) single-band frequency coverage as V_{ctrl} is varied from 0-1.2V.

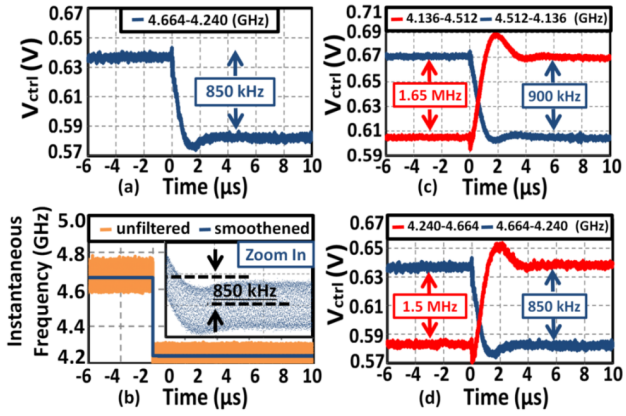

Fig. 9. Measured (a) control voltage and (b) instantaneous output frequency for a hop from 4.644 GHz to 4.24 GHz showing a maximum dynamic frequency error of 850 kHz. Measured control voltage for upward and downward hops (maximum upward/downward dynamic frequency error) between (c) 4.136 GHz and 4.512 GHz (1.65MHz, 900kHz) (d) 4.24 GHz and 4.644 GHz (1.5MHz, 850kHz). The 4.664 to 4.24 GHz downward hop is a repeat of (a).

Fig. 9(a) shows V_{ctrl} in a hop from 4.664 to 4.24 GHz as divider ratio changes from 88 to 80. The PLL settles within 4μs with minimum overshoot. Fig. 9 (b) shows the instantaneous frequency during this period. The dynamic frequency error never exceeds 850 kHz. Fig. 9(c) shows V_{ctrl} in a hop from 4.136 to 4.512 GHz with divider ratio programmed from 88 to 96. Fig. 9(d) shows V_{ctrl} in a hop between 4.24 and 4.644 GHz. In all cases, a very small dynamic frequency error is maintained.

Measured phase noise for 4.24, 4.664 and 5.088 GHz carriers at 1MHz-offset are -115.2, -114.4 and -112.1 dBc/Hz respectively. Table I compares state-of-the-art fast-locking/hopping PLLs.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON TABLE

Work	[5]	[7]	This Work
Architecture	Hybrid-PLL	Dynamic phase-compensation	**Zero initial phase error**
Tech. (CMOS)	0.18-μm	0.18-μm	**65nm**
Frequency (GHz)	2.368-2.496	5.27-5.6	**4.0-5.84**
Power (mW)	29.6	19.8	**16.8**[1]
Supply (V)	1.8	1.8	**1.2**
Reference	64 MHz	10 MHz	**53 MHz**
Loop BW	400 kHz	120 kHz	**800 kHz**
Phase noise @1MHz	-113.0[2] dBc/Hz	-114.28[3] dBc/Hz	**-115.2**[4] dBc/Hz
Reference Spurs	-54 dBc	<-70 dBc	<**-50** dBc
Dynamic Frequency Error	N/R	N/R	**<3.64 MHz average**
Settling-Time	20 μs	20 μs	**5** μs[5]
Chip Area	2.08 mm^2	1.61 mm^2	**0.95** mm^2

[1]Excludes VCO output buffer
Phase noise measured at [2]2.409 GHz [3]5.34 GHz [4]4.24 GHz carriers
[5]For residual errors corresponding to a dynamic frequency error < 3.64 MHz

V. CONCLUSION

An instantaneous-hop frequency synthesizer based on a zero-initial-phase-error multi-modulus divider that breaks the fundamental trade-off between hopping time, spectral purity and frequency resolution is shown.

VI. ACKNOWLEDGEMENTS

The authors thank the DARPA CLASIC program for financial support and Integrand Software for EMX donation.

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