A 0.5GHz-1.5GHz Order Scalable Harmonic Rejection Mixer

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***Abstract*—In this paper, a harmonic rejection mixer architecture capable of operating for a wide range of LO frequencies is demonstrated. The mixer can be configured to suppress any particular harmonic of the LO or multiple harmonics simultaneously. The level of suppression of each harmonic is controlled by a set of independent gain and phase tuning parameters. Feasibility of extension of this concept to higher order harmonics is also demonstrated.**

A proof-of-principle prototype has been designed and fabricated in a 45nm SOI technology. Experimental results demonstrate an operation range of 0.5GHz to 1.5GHz for the LO frequency while offering harmonic rejection better than 55dB for the 3^{rd} harmonic and 58dB for the 5^{th} harmonic across LO frequencies. The mixer consumes 17mW of power from a 1V power supply while occupying an area of 0.352mm^2.

***Index Terms*—Harmonic rejection mixer, cognitive radio.**

I. Introduction

Harmonic rejection mixers (HRMs) have become a necessity in wide-band communication systems. Significant progress has been achieved in understanding the challenges since the classical HRM was demonstrated in [1]–[3].

A limitation of the classical HRM architecture is that the harmonic rejection performance is typically limited to about 30-40dB due to gain and phase mismatches [2], [4]. Two-stage mixing based HRMs have been demonstrated [5] to have superior harmonic rejection. However, there is not much published work using this technique for suppressing higher order harmonics.

The classical HRM architecture described in [1] rejects the 3^{rd} and 5^{th} harmonics leaving the higher order harmonics un-rejected. In order to suppress the higher harmonics, more LO phases and parallel paths are added. An adaptation of this idea has been demonstrated in [6] for TV-Tuner applications. However, this technique has not been demonstrated for LO's above 300MHz.

Superior harmonic rejection using calibration has been demonstrated in [4]. However, with an increase in the number of parallel paths, the number of elements to be tuned scales up. The task of calibrating is harder as the exact source of mismatch becomes more unclear with the increasing number of LO phases and parallel paths.

Fig. 1 shows the block diagram of a cognitive radio receiver. The receiver consists of a broadband LNA, a HRM, a frequency synthesizer to generate wide range of frequencies, an ADC and a DSP. In order to enable simultaneous reception of multiple wireless signals (for instance Wifi, 3G, GPS, etc), the frequency synthesizer would be required to produce multiple LOs simultaneously. Unlike in TV-Tuner applications where the entire band is usually occupied, the spectrum in Cognitive Radios might not be full of strong blockers. For instance, there could be a blocker present around the n^{th} harmonic of LO while the signals around 3^{rd} harmonic are harmless.

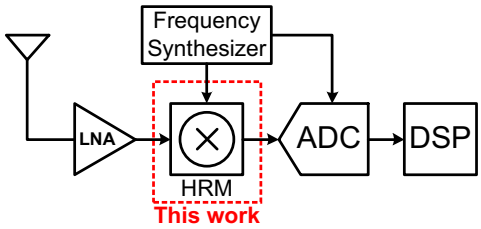
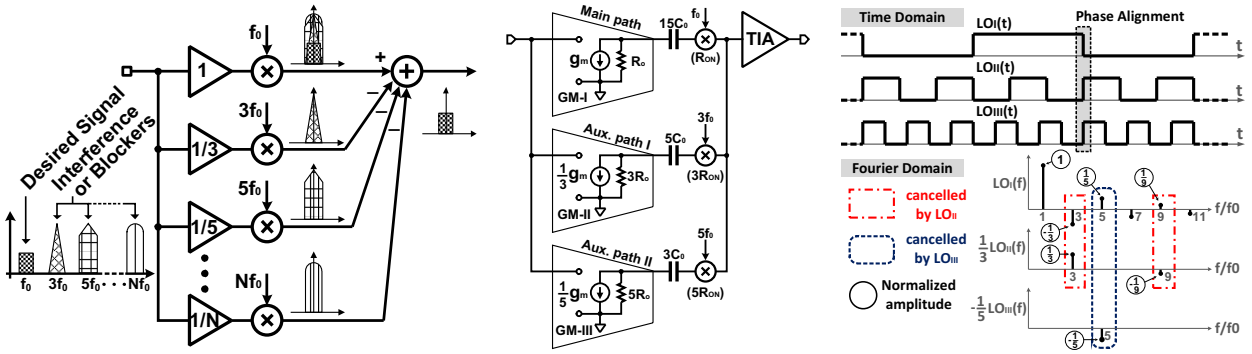


Fig. 1. A cognitive radio receiver consisting of a broadband LNA, a harmonic rejection mixer, ADC-DSP for signal processing and a frequency synthesizer to produce various LOs and clocks.

In this paper we demonstrate a HRM architecture that exploits the availability of multiple LOs and enables suppressing of any particular harmonic. Calibration for rejection of each harmonic of LO can be done independent of other. The rest of the paper is organized as follows: Section II describes the operation of the proposed harmonic rejection mixer architecture and makes some theoretical comparisons with the classical HRM in terms of achievable harmonic rejection. Section III provides details of the circuit implementation is provided. Section IV gives the measurement results and the conclusions are presented in section V.

II. The Proposed Harmonic Rejection Mixer

A model of the proposed harmonic rejection mixer with qualitative illustration of interference cancelling mechanism is shown in Fig. 2(a). The system consists of one main signal path which operates as a conventional mixer and multiple auxiliary paths for interference cancellation. Due to hard switching caused by the LO, interference around harmonic frequencies of LO are also down-converted to IF band and fall in same band as the desired signal. To cancel a particular down-converted interference, an associated auxiliary path is enabled to generate the



(a) (b) (c)

Fig. 2. (a) Block diagram of the reconfigurable HRM architecture (b) Design considerations enabling good gain matching for a perfect harmonic rejection. (c) Appropriate LO phase alignment for a perfect harmonic rejection.

opposite of the interference. The outputs of the two paths are added to cancel the interferer at the IF output.

Depending on the blocker profile, the relevant auxiliary paths can be enabled to enhance the system's resilience to out-of-band interference. The other auxiliary paths can be disabled to reduce power consumption.

We have designed a prototype HRM with one main path and two auxiliary paths for 3rd and 5th harmonic rejection. The suppression of the 3rd harmonic's products depends only on first auxiliary path, while the suppression of the 5th harmonic's products depends on the second auxiliary path. Tuning of HR3 and HR5 can be done independently of each other.

In classical HRMs, the approximation of $\sqrt{2}$ leads to intrinsic gain errors, degrading the harmonic rejection ratio. Our proposed HRM requires a ratio of $1:\frac{1}{3}:\frac{1}{5}$ which avoids approximation of irrational numbers.

A. Gain matching and LO Phase Alignment

Effective transconductance (G_{mX}) of a transconductor is given by

$$G_{mX} = \frac{R_{oX}}{R_{oX} + R_{ONX} - j\frac{1}{\omega C_X} + R_{TIA}} \cdot g_{mX} \qquad (1)$$

where g_{mX} is the transconductance and R_{oX} is the output resistance of GM-X, C_X and R_{ONX} are AC-coupling capacitance and ON-resistance of the switches in signal path X and R_{TIA} is the input impedance of TIA. The appropriate transconductances, impedances and admittances for a perfect cancellation are shown in Fig. 2(b).

In addition to the requirements on the accuracy of signal amplitudes in various paths, there is also a requirement on the phases of LOs. The LO phase alignment for ideal rejection of the harmonics is shown in Fig. 2(c).

For a certain phase misalignment (θ) and gain mismatch (Δ) the theoretically achievable harmonic rejection is given by (2), where HR_n is the harmonic rejection (in dB) obtainable for n^{th} harmonic.

$$HR_n = 20\log\left(\frac{n}{\sqrt{\Delta^2 + n^2\theta^2}}\right) \qquad (2)$$

Theoretically achievable harmonic rejection for various gain and phase mismatches are plotted in Fig. 3. It can be seen that our HRM has a higher achievable harmonic rejection when compared to classical HRM.

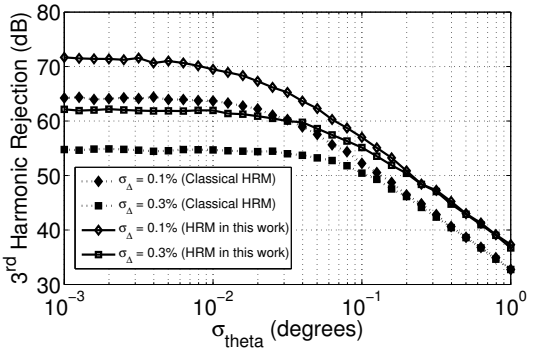
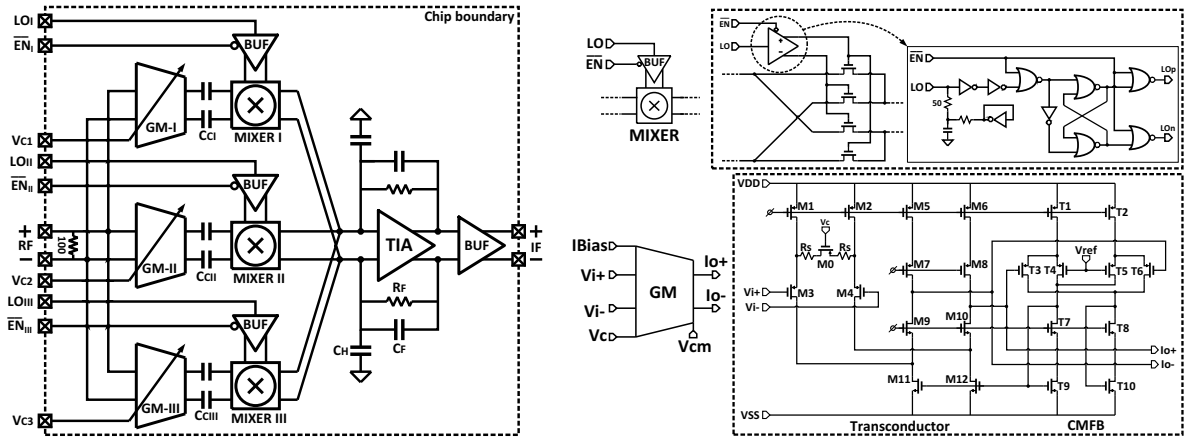


Fig. 3. Theoretically achievable 3rd harmonic rejection in the presence of gain and phase mismatches for the proposed HRM architecture and the classical HRM.

III. Circuit Implementation

The block diagram of the implemented HRM is shown in Fig. 4(a). Input voltage signal drives three transconductors (GM-I, GM-II and GM-III). The currents are coupled to passive mixers through scaled AC-coupling capacitors. The harmonic components from main path are cancelled upon the addition of the down-converted signals. The TIA provides low input impedance for the passive mixers and converts signal current back to voltage.

In order to overcome any mismatch in transconductances, tuning is implemented in the transconductors. For enabling appropriate alignment of the LO phases (as shown in Fig. 2(c)) a voltage controlled delay cell is needed. However, in this proof-of-concept prototype the voltage controlled delay has been realized off-chip.



(a) (b)

Fig. 4. (a) Block diagram of the harmonic reject mixer. (b) Circuit implementation of the tunable transconductor and passive mixer.

A. Tunable Transconductors

The implementations of the transconductors are shown in Fig. 4(b). In order to achieve a perfect harmonic cancellation, $g_{mI} : g_{mII} : g_{mIII}$ needs to be designed with ratio of $1 : \frac{1}{3} : \frac{1}{5}$. High output impedance is also required for transconductors so folded-cascode structure is implemented. The output impedances of three transconductors are scaled with ratio of $1 : 3 : 5$ and the values were designed as $7.2\text{k}\Omega, 21.6\text{k}\Omega, 36\text{k}\Omega$. In circuit implementation, scaling of g_m and R_{out} can be achieved by scaling the number of transistor fingers in the ratio ($F_I : F_{II} : F_{III} = 15 : 5 : 3$).

The tuning is realized by using voltage controlled degeneration resistors. The transconductance vs control voltage (V_c) is shown in Fig. 5.

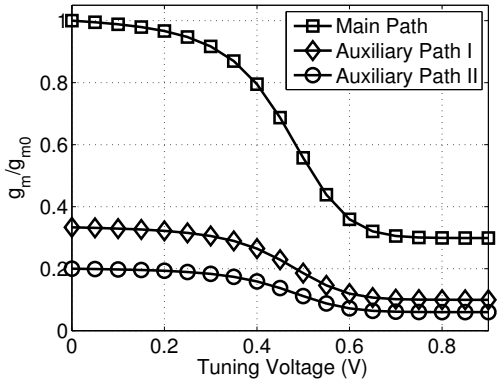


Fig. 5. Simulated transconductance vs tuning voltage for the transconductors. The transconductances are normalized to 3mS (g_{m0}).

B. Passive Mixers

The three transconductors connect to three passive current-commutating mixers which are driven by LO buffers, as shown in Fig. 4(b). The mixers are AC-coupled to the transconductors with scaled capacitors and the lower cut-off frequency is 200MHz.

NMOS switches are used for passive mixers. $R_{ON,switch}$ are designed relatively smaller compared to $R_{out,GM}$ to avoid current loss. Also $R_{ON,switch}$ of three mixers are scaled with ratio of $1 : 3 : 5$ to avoid mismatches.

In the LO buffer, non-overlapping clocks are generated by using cross-coupled NOR gates to avoid the case of partial turn-on of both the switches. NOR gate at outputs of clock buffer is used to disable the LO, thereby turning-off the particular signal paths when necessary.

C. Trans-Impedance Amplifier and Output Buffer

The topology of TIA is based on OTA with shunt-shunt feedback which reduce the input and output impedance. Parallel capacitors are added at input of TIA for decreasing high frequency signal swing. The output buffer is designed for 50Ω matching by using source follower structure.

IV. Measurement Results

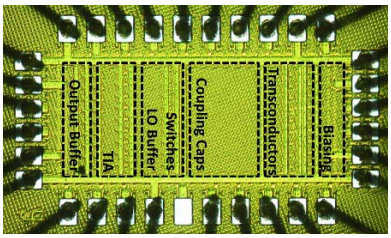


Fig. 6. Die photo of the prototype chip.

The die-photo of the chip prototype is shown in Fig. 6. The chip was fabricated in 45nm SOI Technology. The active area of the HRM is $0.352mm^2$ ($800\mu m \times 440\mu m$).

At the time of paper submission, the transconductance and LO phase calibrations were done manually. The transconductance was controlled using an external voltage.

Agilent E8257D signal generators were used to drive the LO ports of the mixer. The phase of the LO was controlled using the phase shifter inside the signal generators. The measurements results presented here are intended for proof of concept. Also, the harmonic rejection measurements were conducted for one harmonic at a time in order to demonstrate the ability to suppress a particular blocker without having to turn-on all the harmonic rejection paths.

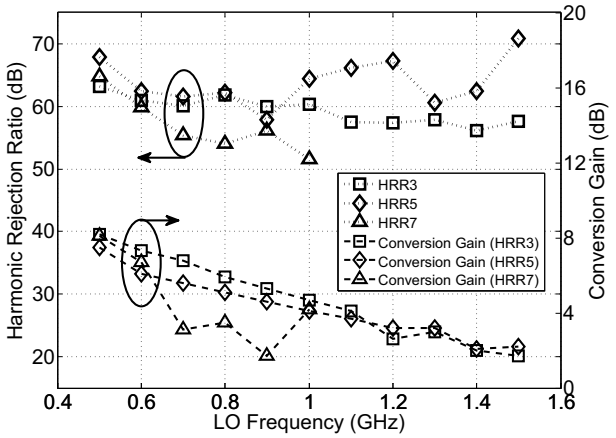


Fig. 7. Measured 3rd, 5th and 7th harmonic rejection and the corresponding conversion gain of the mixer for various LO frequencies.

Fig. 7 shows the measured harmonic rejection and the corresponding conversion gain at various LO frequencies. The harmonic rejection ratios (HRRs) were measured to be better than 55dB for 3rd harmonic and above 58dB for 5th harmonic for LO frequencies up to 1.5GHz.

In order to demonstrate the ease of extension to higher order harmonics, seventh harmonic rejection was also measured. Gm designed for cancelling the 5th harmonic was tuned to produce lesser transconductance. The measured seventh harmonic is also shown in Fig. 7.

A comparison of 3rd harmonic rejection with other existing HRMs is presented in Fig. 8. It can be seen that the proposed harmonic rejection mixer provides good rejection for a wide range of LO frequencies starting from 0.5GHz to 1.5GHz.

The mixer was measured to have a Noise Figure of 35dB, IIP3 of -3dBm and IIP2 of -2dBm while operating with a conversion gain of 8dB for an LO frequency of 800MHz.

V. Conclusions

A 1.5GHz harmonic rejection mixer using auxiliary path cancellation technique for cognitive radio application has been demonstrated in this paper. This work exploits the availability of multiple LOs in a cognitive radio transceivers. It can be configured to suppress any particular harmonic of LO in addition to the ability of

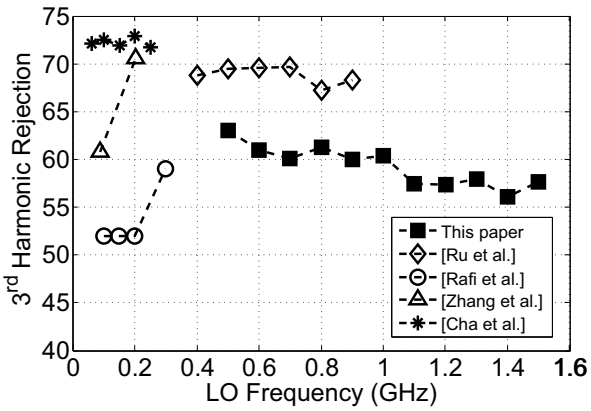


Fig. 8. A comparison for the 3rd harmonic rejection at various LO frequencies with the state-of-the-art HRMs.

simultaneously suppressing multiple LO harmonics. The architecture could be easily extended to suppressing higher harmonics by adding additional parallel paths.

The proposed architecture has been prototyped in 45nm SOI technology to demonstrate 3rd and 5th harmonic suppression. The HRM is demonstrated to operate up to an LO of 1.5GHz providing >55dB of 3rd harmonic rejection and >58dB 5th harmonic rejection. In comparison with existing state of art, we have demonstrated a harmonic rejection mixer that operates at a higher frequency. Further, the feasibility of extending the concept to a higher harmonic rejection has also been demonstrated using 7th harmonic rejection measurements.

Acknowledgements

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