A Compact Fully Integrated High-Efficiency 5GHz Stacked Class-E PA in 65nm CMOS based on Transformer-based Charging Acceleration

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***Abstract*—Device stacking enables CMOS power amplifiers (PAs) to increase the maximum achievable output voltage swing by sharing the voltage stress across multiple stacked devices, leading to higher output power and efficiency. A key requirement in stacked class-E power amplifiers is the creation of class-E-like voltage swings at the intermediary nodes. In this paper, we propose a transformer-based charging acceleration technique for stacked class-E PAs. Specifically, in a 2-stacked class-E PA, a shunt inductor is connected at the intermediary node and is magnetically coupled to the choke inductor. When compared with the conventional approach of using an uncoupled shunt inductor, the transformer-based charging acceleration approach significantly reduces the sizes of both inductors and also eliminates the extra area of the shunt inductor through vertical stacking of the windings. Because of the reduced inductor sizes, the associated loss is also reduced leading to an improvement in efficiency of approximately 7% for the 5GHz prototype described here. The differential 5GHz class-E prototype is fabricated in a standard 65nm low-power (LP) CMOS process (IBM 10LPe), and achieves a drain efficiency of 42% and an output power of 19.7dBm while consuming only 0.31mm^2 of chip area.**

***Index Terms*—CMOS power amplifers, class-E, transformer**

I. Introduction

Switching PAs, such as the class-E PA [1], in conjunction with linearizing architectures [2], are attractive candidates for wireless transmitters because of their extremely high efficiency. However, the high peak voltage swings of class-E PAs impose significant stress due to the low breakdown limit of the highly scaled CMOS technologies. Consequently, low supply voltages need to be used which limit output power. Output power and efficiency are also limited in RF CMOS PAs by the limited quality factor of on-chip inductors.

Output swing, output power and efficiency can be increased in CMOS PAs through device stacking – the stress from a certain large voltage swing is shared between two or more devices. However, stacked class-E PAs have other inherent power loss mechanisms, which degrade efficiency [3],[4]. In a conventional 2-stacked class-E PA (Fig. 1(a)), the bottom device is explicitly driven, and the swing at the intermediary node turns off the stacked device during the OFF half-cycle. However, once the stacked device turns off, the voltage of the intermediary node ceases to increase as the stacked device no longer conducts current to charge the parasitic capacitance at the intermediary node. This leads to unequal distribution of voltage stress and increased conduction loss in the stacked device. In [3], the authors propose the connection of an inductor at the intermediary node to tune out the parasitic capacitance seen at that node, which helps accelerate the ON/OFF switching of the top device (Fig. 1(b)). However, the

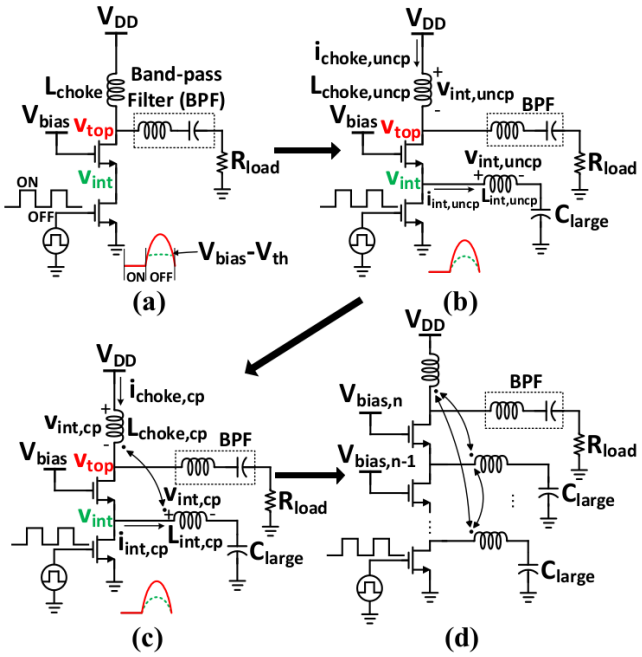

Fig. 1. (a) Conventional 2-stacked class-E PA. (b) 2-stacked class-E PA employing an intermediary inductor. (c) 2-stacked class-E PA employing proposed transformer-based charging acceleration. (d) Generalization of the transformer-based charging acceleration concept to an n-stacked Class E PA.

use of an additional inductor can substantially increase the chip area. To address this problem, a novel transformer-based charging acceleration technique is proposed in this work. This technique involves coupling the RF choke and the intermediary inductor to form a transformer (Fig. 1(c)). Since the voltages across these inductors when uncoupled (and consequently their currents) are scaled versions of each other, coupling the two inductors can considerably reduce *both* of their sizes without compromising the charging acceleration effect. Moreover, vertically coupling the two inductors results in effective utilization of the area of a single inductor. In addition, the reduced inductor sizes lead to reduced power loss, leading to an improvement in efficiency of up to 7% in the 5GHz class-E prototype described in this paper. Fig. 1(d) depicts a generalization of the concept to an n-stacked class-E PA, where all pairs of inductors are coupled, leading to significant reduction in inductor values and loss. In practice, pairwise coupling of 3 or more inductors through vertical stacking is impractical as one or more of the inductors would need to be implemented in the thin lower metal layers. We anticipate that an n-stacked implementation might exploit interwound

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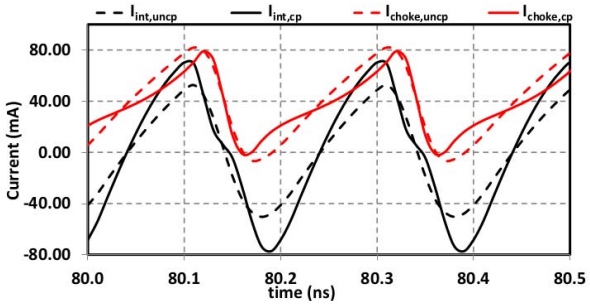


Fig. 2. Inductor current waveforms before and after coupling

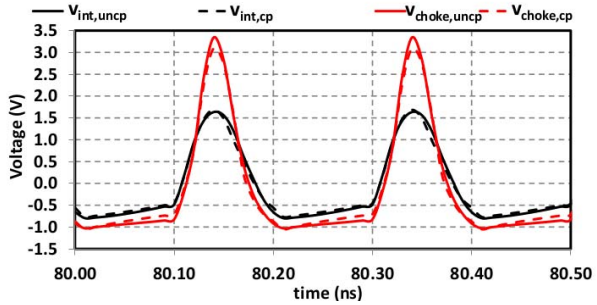


Fig. 3. Inductor voltages before and after coupling

transformers on the same metal layer in conjunction with vertical stacking, or limit coupling to mutually exclusive pairs.

II. Transformer-Based Charging Acceleration

In this section we present a detailed analysis of the transformer-based charging acceleration concept. A 2-stacked class-E PA employing an intermediary inductor (as described in [3]) is shown in Fig. 1(b). Based on the analytical formulation described in [5], the choke inductance value is chosen for optimal efficiency taking into account switch and passive loss, while the top device size is chosen so that the optimal load impedance is 50Ω, eliminating the need for load impedance transformation. The size of bottom device is chosen to optimize the ON-resistance while representing an appropriate load for the driver. The inductor connecting to the intermediary node, which is independent of the RF choke, is properly chosen to resonate with the parasitic capacitance seen at this node. A SpectreRF simulation is run using PDK models for the devices. All inductors are modeled with a series resistance resulting in a Q of 10 at 5GHz. The currents of the choke and intermediary inductor as well as their voltages are shown in Figs. 2 and 3. It can observed that the current waveforms through the RF choke and intermediary inductor are nearly identical in waveform shape except for a DC offset and a scaling factor. In order to avoid changing the circuit's operating conditions as coupling is introduced, the voltages across the choke and intermediary inductors must be kept the same, which leads to the following relationship:

$$L_{choke,cp} + \frac{k\sqrt{L_{choke,cp} \cdot L_{int,cp}}}{N} = L_{choke,uncp} \quad (1)$$

$$L_{int,cp} + N \cdot k\sqrt{L_{choke,cp} \cdot L_{int,cp}} = L_{int,uncp}. \quad (2)$$

TABLE I
Performance Comparison with and without Inductor Coupling

	P_{in} (mW)	P_{out} (mW)	η (%)	PAE (%)	V_{top} (V)	V_{int} (V)
Uncoupled	8.48	46.74	54.9	44.94	4.08	2.39
Coupled	8.12	51.68	62	52.3	4.354	2.2

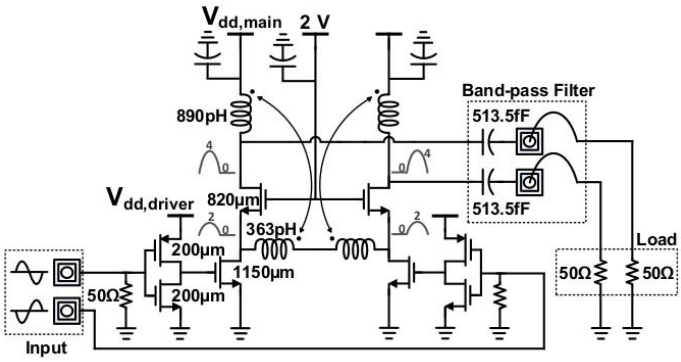


Fig. 4. Circuit diagram of the implemented differential 5GHz class-E PA utilizing transformer-based charging acceleration.

where N is the ratio of the currents through these two inductors when uncoupled (typically 1∼1.3), and k is the coupling coefficient (0.7 in this design as seen from EM simulations). Solving this system of equations one can obtain the new values of the coupled choke and intermediary inductors for a given coupling coefficient k. From (1) and (2), one can see that $L_{choke,cp} < L_{choke,uncp}$ and $L_{int,cp} < L_{int,uncp}$. This leads to area saving and reduced passive loss. Furthermore, implementation of the inductors as vertically stacked spirals results in effective utilization of the area of a single inductor.

Figs. 2 and 3 also show SpectreRF simulations with modified choke and intermediary inductor values once coupling is introduced. As expected, the inductor currents and voltages largely remain unchanged. A summary of these simulation results are shown in Table I. The transformer-based charging acceleration technique improves efficiency by approximately 7% due to reduced inductor sizes and consequently inductor loss. It should be noted that measured efficiency numbers presented later in this paper are lower than the numbers seen in Table I due to the inclusion of driver DC power consumption and the presence of layout-related parasitics.

III. Circuit Implementation

The circuit diagram of the implemented differential 5GHz class-E PA utilizing transformer-based charging acceleration is shown in Fig. 4. Owing to its differential configuration, the intermediary inductor from each half-circuit is connected in series, eliminating the need for the DC blocking capacitors. All the devices shown in the figure are triple-well devices. The body terminal of each device is connected to a large resistor, which significantly reduces power loss in the substrate resistance. The RF choke (0.89nH), intermediary inductors (0.363nH) and devices are sized based on the design approach discussed previously. A separate choke inductor is used for each half-circuit because EM simulations in the IE3D EM

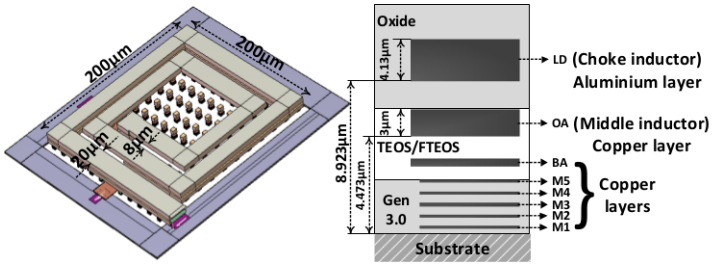
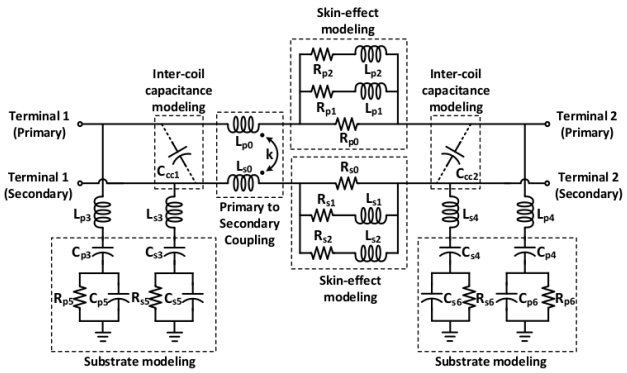


Fig. 5. Transformer 3D view and IBM 10LPe's metal-stack



Param.	Value		Param.	Value		Param.	Value
L_{p0}	850pH		R_{p0}	1.39Ω		k	0.7
L_{p1}	950pH		R_{p1}	1.5Ω		C_{CC1}	200fF
L_{p2}	1.2nH		R_{p2}	1Ω		C_{CC1}	0fF
L_{s0}	380pH		R_{s0}	0.95Ω			
L_{s1}	300pH		R_{s1}	0.7Ω			
L_{s2}	600pH		R_{s2}	0.5Ω			

Fig. 6. Broadband transformer circuit model.

solver show that the use of a differential choke results in negligible area improvement. The output harmonic filter is formed using an on-chip MIM capacitor with a Q of 60 at 5GHz and the inductance of the output wirebonds.

The transformer is designed to have a choke inductance of 890pH and an intermediary inductance of 363pH (compared to uncoupled values of 1.21nH and 700pH). In order to minimize ohmic and substrate losses, the two top-most metal layers in the stack, seen in Fig. 5, are chosen. The vertically-stacked transformer structure is chosen to maximize the area savings and coupling coefficient at the cost of an increase in inter-coil capacitance. The choke is designed as a spiral of dimensions $200\mu m \times 200\mu m$ with 2.25 turns in the LD layer[1]. The intermediary inductor is also a spiral with the same dimensions but with 1.25 turns in the OA layer. In order to satisfy process metal density requirements, a manual metal fill consisting of square dummy strucutures is placed on all metal layers to occupy 9% of the area under the transformer. The square fill structures are sized at 5μm$\times 5\mu$m to minimize losses due to eddy currents induced on them. The transformer is simulated in the IE3D EM solver and is fitted to the circuit model shown in Fig. 6. This model captures various physical

[1]The thick LD layer is chosen for the choke as choke loss is seen to have a more significant impact on efficiency than intermediary inductor loss.

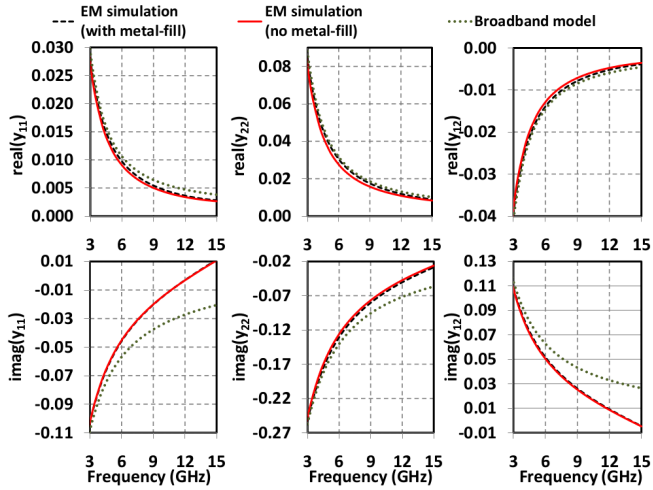


Fig. 7. Y-parameters of the implemented transformer from EM simulations (with and without metal-fill) and from the fitted circuit model.

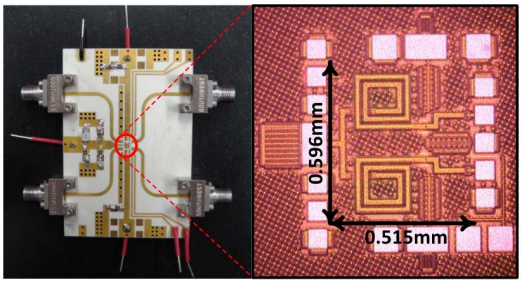


Fig. 8. Test fixture and chip microphotograph of the implemented differential 5GHz class-E PA utilizing transformer-based charging acceleration.

effects such as the skin-effect, finite coupling between the spirals, inter-coil parasitics, oxide capacitance, and substrate parasitics. The model contains 31 parameters some of whose values are mentioned in Fig. 6. This broadband circuit model matches well with the Y-parameters of the EM simulated transformer over a frequency range of DC-15GHz (Fig. 7). The Y-parameters shown are for the transformer with one of the terminals on both spirals shorted to ground as it would be in the implemented circuit. Fig. 7 also compares the Y-parameters of the transformer without metal-fill with the transformer with manual metal-fill. It can be seen that the presence of metal-fill has negligible impact on the characterisitics. The primary and secondary coils have Q's of 20 and 13 respectively, at 5GHz.

The maximum peak AC swing across transistor junctions is limited to $2\times V_{DD}$ = 2V for long-term reliability [3]. This enables a top device gate bias of 2V and a maximum swing of 4V at its drain. While the drain voltage peaks to $3.562\times V_{DD}$ in an ideal class-E PA [1], active and passive component losses prevent voltage swings from reaching their ideal values, and consequently V_{DD} can be increased beyond its theoretical value. Each bottom device is driven by a square wave generated by a complementary class-D driver amplifier. The sizes of the PMOS and NMOS devices of the class-D driver are optimized to maximize overall efficiency. A shunt 50Ω resistor is purposefully placed at each class-D driver input

TABLE II
PERFORMANCE COMPARISON WITH PRIOR RF CMOS PAS ABOVE 5GHZ.

Ref.	Technology	Freq. (GHz)	V_{DD} (V)	P_{sat} (dBm)	Peak η (%)	Peak PAE (%)	Operation Mode	Power Combining	Chip Area
This work	**65nm LP-CMOS**	**5**	**2**	**19.7**	**42%**	**N/A**	**Fully-integrated 2-stacked differential class-E**	none	$0.31mm^2$
[6]	65nm CMOS (uses I/O devices)	6.5	3.6	29.6	N/A	20.3	Differential, 3-stacked class-E/Fodd with off-chip passive components	none	$2.86mm^2$
[7]	65nm CMOS	5.8	1	24.3	27	N/A	Fully-integrated class-AB with on-chip diff.-single-ended conversion	4-way	$0.81mm^2$
[8]	0.18μm CMOS	5.8	3.6	21.4	N/A	39.7	Fully-integrated single-ended cascode	none	$1.1mm^2$
[9]	0.18μm CMOS	5	3.3	26.5	N/A	26.7	Fully-integrated differential class-AB	none	$2.52mm^2$
[10]	0.18μm CMOS	5	1.8	19.2	N/A	17.5	Fully-integrated differential class-AB	none	$0.54mm^2$
[11]	0.18μm CMOS	5	1.8	17.4	N/A	27.1	Fully-integrated single-ended class-AB	none	$0.84mm^2$
[12]	0.18μm CMOS	5.8	1.8	15.7	N/A	25.1	Fully-integrated single-ended class-E	none	$0.81mm^2$

to provide a matched interface for measurement. Since this resistor consumes input power and would not be present in a fully integrated transmitter SoC implementation, the drain efficiency η is chosen to be the performance metric instead of the PAE. The simulated PAE in the absence of this resistor is seen to be only 1-3% lower than the drain efficiency.

Parasitic capacitance and resistance from the device layout is extracted using Calibre PEX. Transmission line models built using IE3D are used for all RF signal as well as supply lines.

IV. MEASUREMENT RESULTS

The chip microphotograph and its test fixture are shown in Fig. 8. The chip is mounted on a Rogers 4350 RF laminate-based PCB, and the input and output pads are wirebonded to 50Ω microstrip traces that are connectorized using Southwest DC-40GHz connectors. The loss of the output microstrips and the Southwest connectors are de-embedded. The PCB is designed to enable output wirebonds of appropriate length (and therefore, inductance) for the output harmonic filter.

The measured and simulated output power across frequency for a $V_{DD,main}$=2V and across $V_{DD,main}$ at 5GHz is shown in Fig. 9. The measured and simulated drain efficiency across frequency for a $V_{DD,main}$=2V and across $V_{DD,main}$ at 5GHz is shown in Fig. 10. In all cases, $V_{DD,driver}$ is 1.1V. At 5GHz, with $V_{DD,main}$=2V, the implemented PA achieves an output power of 19.7dBm at a drain efficiency of 42%. A comparison with the prior work is shown in Table II. It can be seen that the implemented PA utilizes only a fraction of the area of the listed PAs while achieving similar performance.

V. CONCLUSION

A compact fully-integrated high-efficiency 5GHz class-E PA in 65nm LP CMOS based on transformer-coupled charging acceleration is presented. Topics for future research include extension of the topology to higher levels of stacking, and the implementation of linearizing achitectures for class-E PAs.

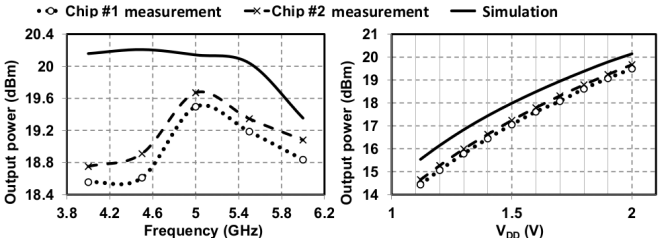


Fig. 9. Measured and simulated output power across frequency for $V_{DD,main}$=2V and across $V_{DD,main}$ at 5GHz

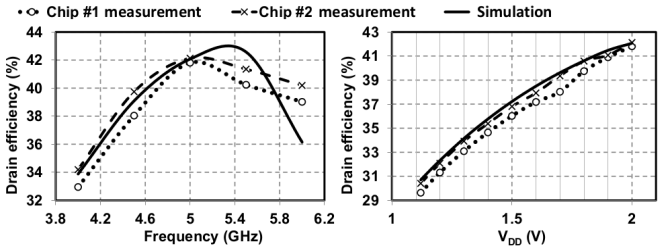


Fig. 10. Measured and simulated drain efficiency across frequency for $V_{DD,main}$=2V and across $V_{DD,main}$ at 5GHz

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