High Power, High Efficiency Stacked mmWave Class-E-like Power Amplifiers in 45nm SOI CMOS

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***Abstract*—Stacking devices in CMOS power amplifiers (PAs) increases the achievable output voltage swing, thereby increasing the output power and efficiency, particularly at millimeter-wave frequencies. This work presents stacked CMOS PAs based on an improved Class-E design methodology, where device loss is explicitly accounted for in the analysis and design procedure. Design guidelines and fundamental limits on achievable performance are presented. Two fully-integrated 45GHz prototypes with 2 and 4 stacked devices have been fabricated in IBM's 45nm SOI CMOS technology. Measurement results yield a peak PAE of 34.6% for the 2-stacked PA with a saturated output power of 17.6 dBm, and a peak PAE of 19.4% for the 4-stacked PA with a saturated output power of 20.3 dBm. The former represents the highest PAE reported for CMOS mmWave PAs, and the latter represents the highest output power achieved from a CMOS mmWave PA. The paper also describes the modeling of active and passive devices for mmWave CMOS PAs for good model-hardware correlation.**

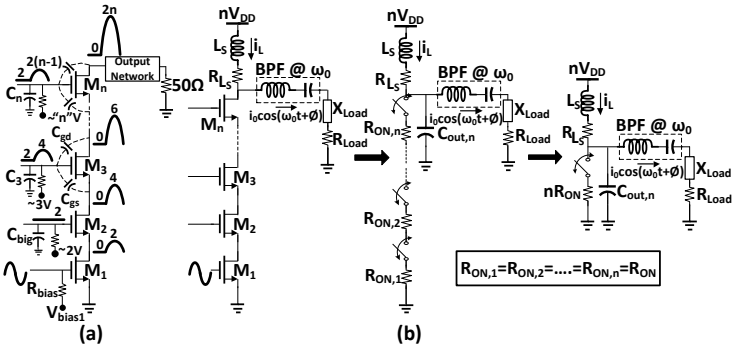

Fig. 1. (a) Stacked CMOS Class-E-like PAs with voltage swings annotated in volts. (b) Loss-aware Class-E design methodology for stacked PAs.

I. Introduction

The design of high-efficiency, high-power, mmWave CMOS power amplifiers (PAs) is challenging because of the limited breakdown voltage of highly-scaled CMOS technologies, low available gain of devices, and poor quality of on-chip passives. Switching PAs (such as Class-E PAs [1]) in CMOS are yet to be explored at mmWave frequencies due to the lack of ideal square-wave drives (resulting in soft switching), impracticality of harmonic shaping of voltages and currents, low PAE due to the high input drive levels required to switch the devices and high loss levels in the device/switch. Thus, at mmWave frequencies, one can practically implement a "switch-like" PA.

One technique to increase the output power of a PA is the stacking of multiple devices, which increases the voltage swing at the load. Stacking can be aggressively pursued in SOI CMOS relative to bulk CMOS due to the mitigation of the drain-bulk junction breakdown mechanism for the topmost device. Stacking for mmWave SOI CMOS PAs has been explored recently in the context of linear PAs [3]. In this paper, we explore stacked "Class-E-like" PAs. A loss-aware Class-E design methodology that accounts for high device loss [2] is used to understand the design trade-offs and determine the fundamental limits of performance. Two 45GHz prototypes with 2 and 4 stacked devices have been fabricated in IBM's 45nm SOI CMOS technology. The modeling of active and passive devices for mmWave CMOS PAs is also described.

II. Stacked CMOS Class-E-like PAs: Concept and Fundamental Performance Limits

Fig. 1(a) depicts the concept of a stacked CMOS Class-E-like PA. Multiple devices of equal size are stacked, and to preserve input power and improve PAE, only the bottom device is driven by the input. The stacked devices turn on and off due to the swing of the intermediary nodes. The topmost drain is loaded with an output network that is designed based on Class-E principles, and consequently sustains a Class-E-like voltage waveform. The intermediary drain nodes must also sustain Class-E-like voltage swings with scaled amplitudes so that the voltage stress is shared equally among all devices. In the 45nm SOI CMOS technology employed, the nominal V_{DD} of the high-speed thin-oxide devices is ≈1V and for long-term reliability, the maximum peak AC swing across any two transistor junctions is limited to $2\times V_{DD}$=2V [4]. Consequently, for an n-stack, the peak output swing is $2n$ V as marked on Fig. 1(a), and the appropriate intermediary node swings are also noted. Appropriate voltage swing may be induced at the intermediary nodes through techniques such as inductive tuning [4] and capacitive charging acceleration [5] that have been explored at RF frequencies for cascode Class-E PAs. The trade-offs associated with inductive tuning for Class-E-like PAs at millimeter-wave frequencies will be discussed later in this paper. In order to conform to the peak AC swing requirement across the gate-source junction in the on half cycle and the gate-drain junction in the off half-cycle, the gates of the devices in the stack must swing as shown in Fig. 1(a). This swing at each gate is induced through capacitive coupling from the corresponding source and drain via C_{gs} and C_{gd} respectively and is controlled through the gate capacitor C_n. The DC biases of all gates are applied through large resistors.

To facilitate a theoretical analysis, the improved loss-aware Class-E design methodology described in [2] is employed. The basic Class-E design methodology of ensuring

978-1-4673-1556-2/12/$31.00@2012 IEEE

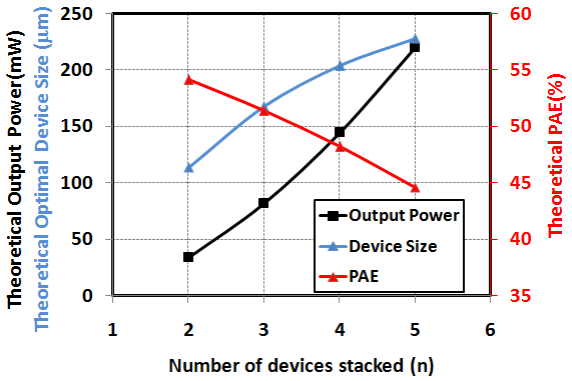

Fig. 2. Theoretical output power, PAE and optimal device size as a function of number of devices stacked based on the loss-aware Class-E design methodology.

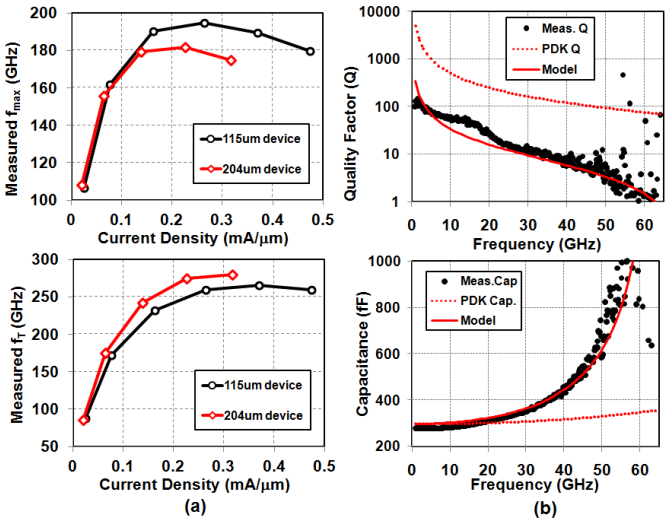

Fig. 3. (a) Measured (extrapolated) f_{max} and f_T of $\frac{2.793\mu m \times 41}{40nm}$ and $\frac{2.793\mu m \times 73}{40nm}$ power devices in IBM 45nm SOI CMOS across current density. (b) Series capacitance ($C = -\frac{1}{\omega \times imag(\frac{1}{Y_{21}})}$) and Q ($= \frac{imag(Y_{21})}{real(Y_{21})}$) of a L=12$\mu$m, W=11.42$\mu$m 280fF VNCAP from the PDK model, EM-simulation-based model and measurements.

zero-voltage switching (ZVS) and zero-derivative-of-voltage switching (ZdVS) [1] is no longer optimal in the presence of high loss levels in the switching device and/or passive components. The improved loss-aware Class-E design methodology formally takes switch loss and passive loss into account. The methodology also incorporates the input power required to drive the switch and enables optimization of PAE rather than drain efficiency. In essence, the loss-aware Class-E design methodology is an analytical load pull for optimal PAE in the presence of high loss levels and input power requirements. For the purpose of this analysis, the stacked devices are assumed to behave as a single switch with linearly-increased breakdown voltage and on-resistance, and an output capacitance that is the same as that of the top device. For various levels of stacking (n), the design methodology is used to analytically vary device-size and DC feed inductance to find the design point with maximum PAE under the constraint of a 50Ω load impedance to avoid impedance transformation losses. Device on-resistance, output capacitance and input-drive-power as functions of device size are determined from post-layout device simulations. Inductor Q is assumed to be 15 based on EM simulations. Fig. 2 depicts the optimal output power and the corresponding PAE for different levels of stacking, as well as the optimal size of each stacked device. It is clear that due to the increasing achievable output voltage swing, stacking in Class-E-like CMOS PAs enables dramatic increases in output power (near-quadratic due to linear increase in output swing). The PAE reduces with increased stacking due to increasing total switch loss. However the methodology ensures that the PAE degradation is gradual. In order to do this, the design methodology requires the size of each stacked device to increase with n to reduce their on-resistance. Consequently careful device layout is required for high levels of stacking.

This analysis takes into account several mmWave non-idealities, and consequently, the results in Fig. 2 represent the fundamental limits on achievable performance in stacked CMOS Class-E-like PAs. In practical implementations, the main non-ideality that causes deviation from these limits is soft switching of the stacked devices due to the lack of square-wave drives. Nevertheless, the optimal design points predicted are excellent starting points for simulation-based optimization.

III. Power Device, Passive Component Modeling

In IBM's 45nm SOI CMOS technology, an accurate high-frequency model for the device which accounts for intrinsic input resistance (IIR) as well as layout-related wiring resistances, capacitances and inductances of the gate, drain and source fingers and vias is non-existent. The model provided in the design kit is augmented to incorporate the impact of IIR [6]. Wiring resistances and capacitances, extracted using Calibre PEX, and high-frequency models for the gate and drain vias, simulated in the IE3D EM field solver, are also added to the design kit model. Fig. 3(a) shows the measured f_{max} and f_T of the power devices used in the implemented 2-stacked and 4-stacked PAs. Device measurements were performed up to 65GHz, open-short de-embedding was performed to a reference plane at the top of the gate and drain vias, and the measured f_{max} and f_T were obtained by extrapolating the measured U and h_{21} at 20dB/decade. The measured U is observed to have 20dB/decade slope upto 65GHz and the modeled U exhibits the same slope upto f_{max}. It is difficult to achieve f_{max} for power devices that is similar to that of smaller devices due to layout challenges [7]. Nevertheless, through careful layout, peak f_{max} of ≈180GHz and ≈190GHz are achieved for these power devices. For reference, our measurements reveal that a $\frac{1\mu m \times 10}{40nm}$ device achieves an f_{max} of approximately 250GHz in this technology.

Vertical Natural Capacitors (VNCAPs), also called interdigitated capacitors, are available in the PDK. Fig. 3(b) shows the measured series capacitance and Q for a L=12μm, W=11.42μm 280fF VNCAP that is used in the input matching network of the 4-stack PA. An EM-simulation-based model

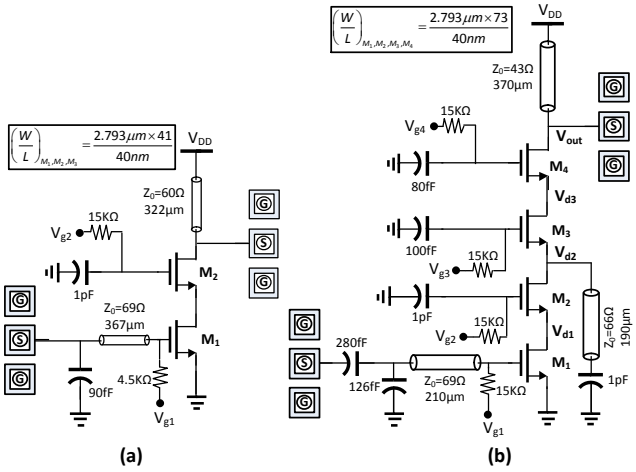

Fig. 4. Schematic of Class-E like PA with (a) 2 devices stacked, and (b) 4 devices stacked.

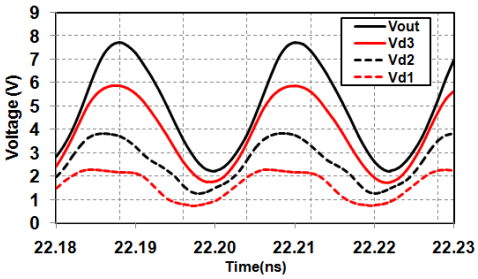

Fig. 5. Drain voltage waveforms of the 4-stacked Class-E-like PA ($V_{g1} = 0.3V$, $V_{g2} = 2V$, $V_{g3} = 3V$, $V_{g4} = 4.4V$, $V_{DD} = 5V$).

and measurements of the VNCAP reveal that extra series inductance and loss need to be added to the PDK model. Inductors in the design are implemented using coplanar waveguides (CPW). Measurements of a typical 66Ω CPW reveal a Q of 15-18 in Q-band (33-50GHz). Device decoupling capacitors (DGNCAPs) used in the design are also characterized.

IV. Implementation Details

The schematics in Fig. 4 depict the Class-E-like PAs implemented by stacking 2 and 4 floating-body devices. Device sizes and DC feed inductance values are chosen based on the theoretical analysis, and supply and gate bias voltages and gate capacitor values are selected based on the considerations described earlier. For the first stacked device (M_2 in both designs), as described earlier, the gate voltage must be held to a constant bias. This can be accomplished through a large bypass capacitor placed as close as possible to the gate to mitigate stray inductance that can result in oscillations. DGNCAPs are suitable for this purpose since they are implemented in the lowest metal layer and provide much higher capacitance density than the VNCAPs. All other capacitors, including gate capacitors for the higher stacked devices, which are not large in value, are implemented using VNCAPs. For both the designs, the output harmonic filter is eliminated to avoid passive loss with minimal impact on performance.

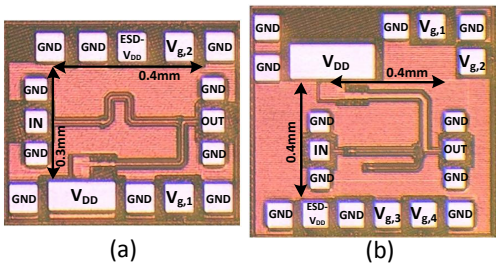

Fig. 6. Chip microphotographs of the mmWave stacked Class-E-like PAs with (a) 2 devices stacked, and (b) 4 devices stacked.

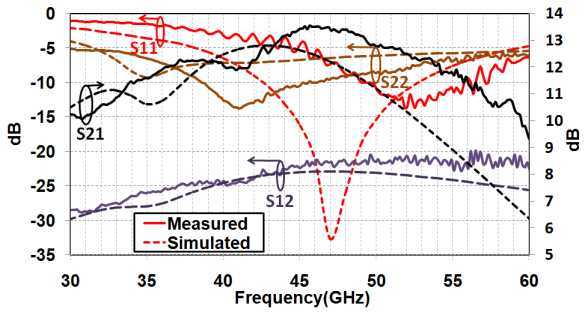

Fig. 7. Small signal S-parameters of 2-stacked Class-E-like PA ($V_{g1} = 0.5V$, $V_{g2} = 1.6V$, $V_{DD} = 2.3V$).

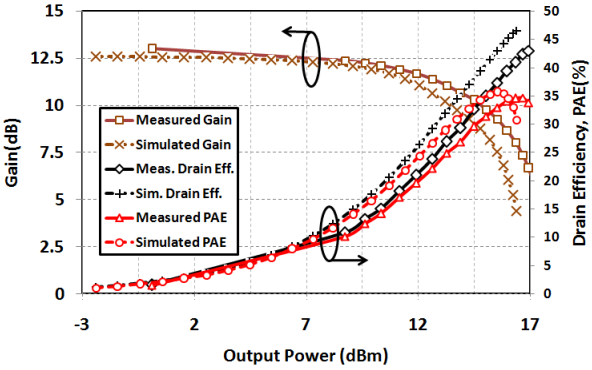

Fig. 8. Large signal performance of the 2-stacked Class-E-like PA at 47GHz ($V_{g1} = 0.4V$, $V_{g2} = 1.7V$, $V_{DD} = 2.4V$).

As was mentioned earlier, a tuning inductor may be placed at intermediary nodes to improve their voltage swing and make them more Class-E-like. Simulation results indicate that the improvement in swing for the 2-stacked PA is offset by the resultant increased conduction loss of the devices. Consequently, no tuning inductor is used. For the 4-stacked PA, a tuning inductor at V_{d2} is seen to provide benefit. Intuitively, a 4-stacked configuration can be viewed as a stack of two 2-stacked PAs with a tuning inductor in between.

V. Experimental Results

The implemented PAs (Fig. 6) are tested in chip-on-board configuration through on-chip probing. Figs. 7-10 depict the simulated and measured small signal S-parameters and large-signal performance of the two PAs. Measurement results yield a peak PAE of 34.6% for the 2-stacked PA with a saturated

TABLE I
COMPARISON WITH STATE-OF-THE-ART FULLY-INTEGRATED CMOS MMWAVE PAS

Ref.	Technology	Freq. (GHz)	P_{sat} (dBm)	η (%)	Peak PAE (%)	Gain (dB)	Class of Operation	Power Combining
This work	**45nm SOI**	**47**	**17.6**	**42.4**	**34.6**	**13**	Class E, 2-stacked	None
This work	**45nm SOI**	**47.5**	**20.3**	**23**	**19.4**	**12.8**	Class E, 4-stacked	None
[8]	65nm	60	17.9	N/A	11.7	19.2	Class A	Differential, 4-way-combined (differential output)
[9]	90nm	60	19.9	N/A	14.2	20.6	N/A	4-way-combined
[10]	65nm	60	18.6	N/A	15.1	20.3	N/A	Differential, 2-way-combined (single-ended output)
[11]	65nm SOI	60	14.5	N/A	25	16	Class AB, cascode	None
[3]	45nm SOI	45	18.2	N/A	23	8	Class AB, 3-stacked	None
[12]	65nm	79	19.3	N/A	19.2	24.2	N/A	Differential, 4-way-combined (with on-chip balun)
[13]	40nm	60	15.6	N/A	25	N/A	N/A	Differential, 2-way-combined (outphasing) (differential output)

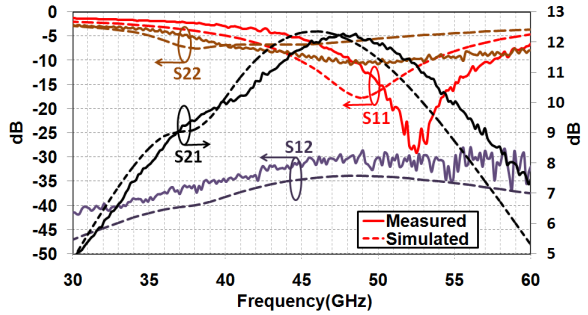

Fig. 9. Small signal S-parameters of 4-stacked Class-E-like PA($V_{g1} = 0.3V, V_{g2} = 2V, V_{g3} = 3V, V_{g4} = 4.4V, V_{DD} = 5V$).

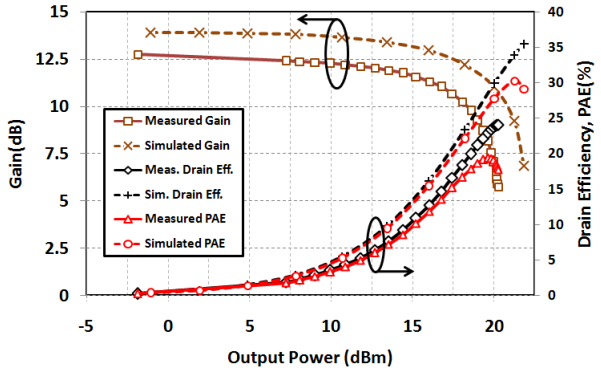

Fig. 10. Large signal performance of the 4-stacked Class-E-like PA at 47.5GHz($V_{g1} = 0.4V, V_{g2} = 1.7V, V_{g3} = 2.8V, V_{g4} = 4V, V_{DD} = 4.7V$).

output power of 17.6 dBm, and a peak PAE of 19.4% for the 4-stacked PA with a saturated output power of 20.3 dBm. At a supply voltage of 2.7V, the 2-stacked PA delivers a saturated output power of 18.1dBm with 2% peak-PAE degradation. The 2-stacked PA exhibits the highest PAE reported for CMOS mmWave PAs. The 4-stacked PA exhibits the highest output power achieved from a CMOS mmWave PA (Table I). Prior CMOS mmWave PAs with comparable output power rely on power combining. Consequently, the power combining of several 4-stacked Class E PAs can lead to output powers that approach 1W. A good correspondence is also seen between the measured and simulated results due to the modeling effort.

VI. CONCLUSION

High-power, high-efficiency Class-E-like PAs are demonstrated at 45GHz using device stacking and a modified loss-aware Class-E design methodology in IBM's 45nm SOI CMOS technology. Stacked Class-E-like SOI CMOS PAs represent an important step towards the implementation of watt-class, efficient, mmWave PAs.

VII. ACKNOWLEDGEMENTS

The authors acknowledge the DARPA ELASTx program (Dr. S. Raman), and AFRL (Drs. R. Worley and P. Watson).

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