215GHz CMOS signal source based on a Maximum Gain Ring Oscillator topology

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***Abstract*—This paper introduces a Maximum Gain Ring Oscillator (MGRO) topology that maximizes the power gain achieved by the active devices using appropriately designed passive matching networks to maximize the frequency of oscillation. A design methodology is provided along with guidelines for the design of the passive matching network. In the absence of passive losses, the topology can oscillate at the f_{max} of the active devices. In the presence of passive loss, the losses can be taken into account in a closed-form fashion to maximize oscillation frequency. Based on this topology, an oscillator operating at approximately 107.5GHz is implemented using the 56-nm body-contacted devices of IBM's 45nm SOI CMOS technology (f_{max} is about 200GHz). The second harmonic of this oscillation is extracted using a load-pull-optimized, extraction network. This topology can be generalized for the extraction of any harmonic from MGROs with different number of stages. The oscillator generates -14.4dBm of power at 216.2GHz while drawing 57.5mW of DC power. The modeling of 45nm SOI devices for millimeter-wave design is also described.**

***Index Terms*—oscillators, Submillimeter wave ICs.**

I. Introduction

The millimeter-wave (30-300GHz) and terahertz (300GHz-3THz) frequency ranges have been receiving increasing interest in recent times. Recently, efforts have been made to implement CMOS signal sources in the high mmWave and low terahertz ranges [1], [2], and to develop oscillator topologies that increase the maximum oscillation frequency over conventional approaches [3], [4].

II. IBM 45nm SOI CMOS Modeling

Fig. 1(a) depicts the small-signal model of a body-contacted (BC) SOI MOSFET based on a simplified BSIM4SOI model and externally added layout parasitics. Fig. 1(b) depicts the gate-over-device layout that is utilized for the MOSFET. This layout approach is employed to minimize gate wiring resistance and allow a symmetric doubly-contacted gate. The IBM 45nm SOI CMOS PDK does not model r_{IIR}, r_{BDB} and r_{BSB} in the body resistance network, and externally added layout parasitics. r_{IIR}, r_{BDB} and r_{BSB} are determined from the measurements described below. Capacitive layout parasitics are estimated using the Calibre extraction tool, and via inductances and coupling are determined using the IE3D EM field solver. Note that the g_m has been split and is controlled by two nodes, to improve the model fit. This splitting is expected because of the distributed nature of the gate node.

A $10\times1\mu$m/56nm body-contacted (BC) device was measured upto 67GHz. Pads and feedlines were deembedded using open-short(OS) deembedding [5], shifting the reference plane to the top of the gate and drain vias. The model described in Fig. 1(a) was then fit to measurement. Plots of Mason's Unilateral Gain (MUG) and h_{21} from the measurements and the model are shown in Fig. 1(c) for $J = 0.56mA/\mu$m, the bias under which the device operates in the implemented oscillator. The measured f_{max} and f_T are 204GHz and 140GHz respectively. However, in the presence of r_{IIR} modeling, transient simulations in Spectre do not converge. Consequently, for transient simulations, a bias-independent $r_{IIR,eq}$ resistance is added external to the model to achieve a simulated f_{max} of about 200GHz.

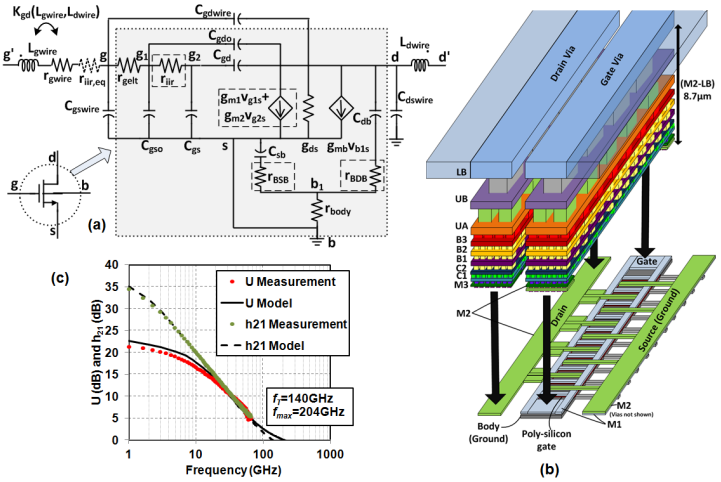

Fig. 1. (a) Small-signal model of an SOI MOSFET based on a simplified BSIM4SOI model and externally added layout parasitics. (b) Gate-over-device layout. (c) Measured and modeled U and h_{21} of a $10\times1\mu$m/56nm body-contacted NMOS device at current density $J = 0.56mA/\mu$m.

III. Maximum Gain Ring Oscillator Topology

While oscillators are large-signal circuits, small-signal concepts of f_{max} and maximum power gain are relevant to compute the startup gain of an oscillator topology and consequently its maximum oscillation frequency. The conventional way in which high-frequency CMOS oscillators are built is the cross-coupled oscillator topology (XCO) (Fig. 2(a)). The XCO can be viewed as a ring of two tuned amplifiers with a single effective inductor acting as the matching component between the amplifiers. This is insufficient to convert the input impedance of the second amplifier to the optimal load impedance needed by the first for maximum power gain. Consequently, the XCO can be expected to exhibit a maximum oscillation frequency that is below f_{max}.

The MGRO, as shown in Fig. 2(b), rectifies the matching problem by including additional reactive components in the matching network between the stages. If the Y-parameters of each device are represented by [**Y**] with $Y_{ij} = G_{ij} + jB_{ij}$,

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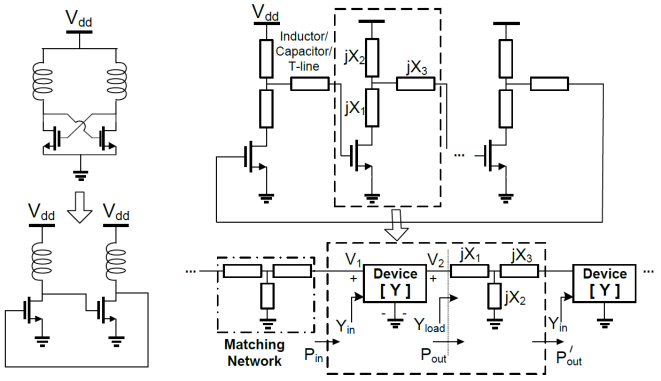

Fig. 2. (a) Cross-coupled oscillator as a two-stage tuned ring oscillator with a single inter-stage matching inductor. (b) MGRO concept.

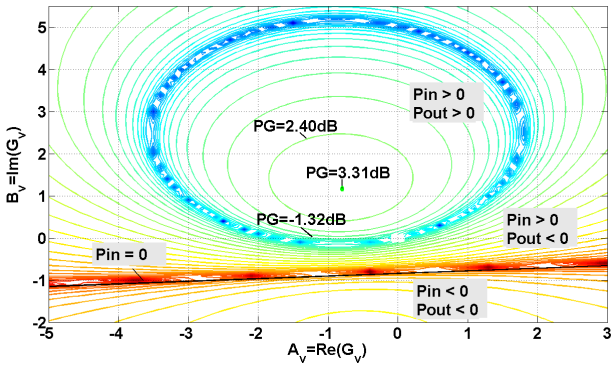

Fig. 3. Power gain (PG) circles on the G_v plane at 100GHz for the $10\times1\mu$m/56nm body-contacted(BC) NMOS device.

$$Y_{in} = \frac{1}{Z_{in}} = Y_{11} + G_v Y_{12} \tag{1}$$

$$Y_{load} = \frac{1}{Z_{load}} = -\left(\frac{Y_{21}}{G_v} + Y_{22}\right) \tag{2}$$

$$PG = \frac{P_{out}}{P_{in}} = \frac{|G_v|^2 Re(Y_{load})}{Re(Y_{in})} = \frac{-\left((A_v^2 + B_v^2)G_{22} + A_v G_{21} + B_v B_{21}\right)}{(G_{11} + A_v G_{12} - B_v B_{12})} \tag{3}$$

where $G_v = \frac{V_2}{V_1} = A_v + jB_v$ is the voltage gain across each device. P_{in} is the power flowing into the gate of the device, P_{out} is the power delivered out of the drain, and P'_{out} is the power delivered after the matching network[1]. Y_{in} is the input impedance of the device and Y_{load} is the impedance to which the input impedance of the subsequent stage is transformed by the matching network. In the absence of passive loss, $P'_{out} = P_{out}$ and hence, device power gain, and consequently oscillator startup gain, can be maximized by determining the complex G_v value that maximizes PG in (3). This may be performed either analytically or numerically if the device Y-parameters are known. Fig. 3 depicts power gain (PG) circles on the real-imaginary plane of G_v at 100GHz for the $10\times1\mu$m/56nm BC NMOS device at the bias condition under which the device operates in the implemented oscillator. The maximum achievable power gain is 3.3dB.

When the passive matching components contain loss, the maximum oscillation frequency will be lower than f_{max} and the optimal G_v value might change. We can use Foster's second theorem to arrive at the following expression.

$$E_E - E_M = \frac{1}{4\omega}\left(|G_v V_1|^2 Im\left(Y_{load}\right) - \frac{2P'_{out}}{Re\left(Y_{in}\right)} Im\left(Y_{in}\right)\right) \tag{4}$$

where E_E and E_M are the stored electric and magnetic energies in the matching network respectively. If the RHS of (4) is positive, the matching network must store net electric energy; otherwise the net stored energy is magnetic. Assuming that the matching network may be constructed with inductors and capacitors of quality factors Q_L and Q_C respectively, the total loss in the matching network is $P_{loss} = 2\omega\frac{E_M}{Q_L} + 2\omega\frac{E_E}{Q_C}$. If the net stored energy is magnetic, to minimize P_{loss}, only inductors should be used. The use of capacitors will require an increase in the stored magnetic energy to compensate for the non-zero E_E. For MOSFET devices, the matching network must typically store net magnetic energy. Assuming an all inductor network ($E_E = 0$), the net power gain including matching network loss can be written as

[1]This formulation and the developed design methodology is general and can be used for device configurations other than common-source, or even configurations involving multiple devices.

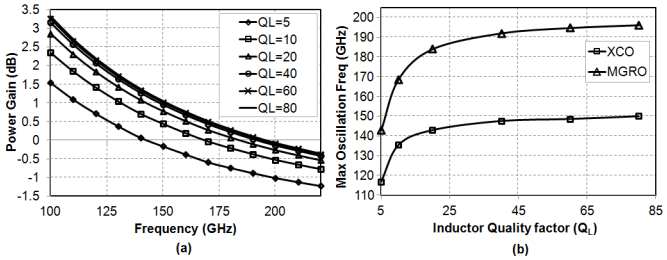

Fig. 4. (a) PG'_{max} of the $10\times1\mu$m/56nm body-contacted NMOS device versus frequency for different Q_L values. The annotated Q_L values are at 100GHz, and Q_L is assumed to scale linearly with frequency. (b) Maximum oscillation frequencies of the device in the MGRO and XCO topologies as a function of the Q_L at 100GHz.

$$P'_{out} = P_{out} - P_{loss} = P_{out} - 2\omega\frac{E_M}{Q_L} \tag{5}$$

$$PG' = \frac{P'_{out}}{P_{in}} = \frac{|G_v|^2}{2}\left[\frac{Q_L Re(Y_{load}) + Im(Y_{load})}{Q_L Re(Y_{in}) + Im(Y_{in})}\right] \tag{6}$$

Oscillator startup gain is now maximized by determining the G_v value that maximizes PG' in (6) while restricting oneself to G_v values that result in net stored magnetic energy. It is interesting that for such matching networks employing only inductors, P_{loss} and consequently PG' are independent of network topology (T-match, pi-match etc.) or number of inductors, but only depend on Q_L. PG' contour plots similar to Fig. 3 may be plotted to maximize PG' with respect to G_v.

Fig. 4(a) depicts the PG'_{max} of the $10\times1\mu$m/56nm BC NMOS device versus frequency for different Q_L. Fig. 4(b)

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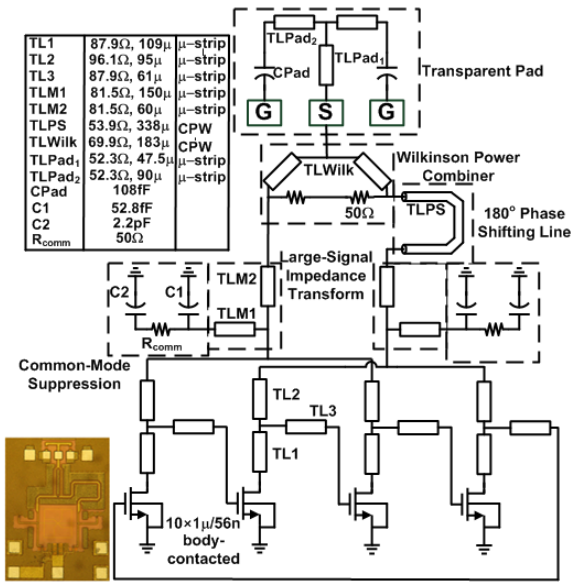

Fig. 5. Circuit diagram and chip microphotograph of the 870μm $\times$ 620μm 215GHz signal source.

depicts the maximum oscillation frequency of the MGRO topology as a function of Q_L (namely the frequencies at which $PG'_{max} = 1$) and compares it with the simulated maximum oscillation frequency of the XCO topology. A significant enhancement is observed.

In addition to maximizing power gain for startup, the total phase shift in the ring must also equal an integral multiple of 2π at the desired frequency. While two reactances are sufficient to achieve the impedance transformation for optimal G_v, a third reactance is required to arbitrarily control the phase shift ϕ across a stage. This allows flexibility in the number of stages N ($N\phi = 2n\pi$, $n \in \mathbf{Z}$). A larger number of stages allows power combining of the harmonic signals generated by a larger number of transistors at the expense of DC power.

IV. Harmonic Power Extraction

Based on this topology, an oscillator operating at 107.5GHz is implemented using IBM's 45nm SOI CMOS technology. A four-stage MGRO is implemented using 10$\times$1μm/56nm BC NMOS devices (Fig. 5). In the implemented 215GHz signal source (Fig. 5), two differential pairs are identified and tied together above $TL2$. The second harmonic is extracted by phase shifting one common-mode path by 180° followed by the use of a Wilkinson power combiner. A 50Ω load impedance may not be optimal for the common-mode paths. In this prototype, a load-pull simulation was performed to maximize the second-harmonic output power after phase shifting and combining. A two-transmission-line matching network (TLM1 and TLM2) is implemented to transform 50Ω to the optimal impedance.

V. Experimental Results

The signal source is tested in chip-on-board configuration through on-chip probing and a WR-3 Second Harmonic Mixer Downconverter (SHMD) from VDI. The measured oscillation frequency and calibrated output power of the source are

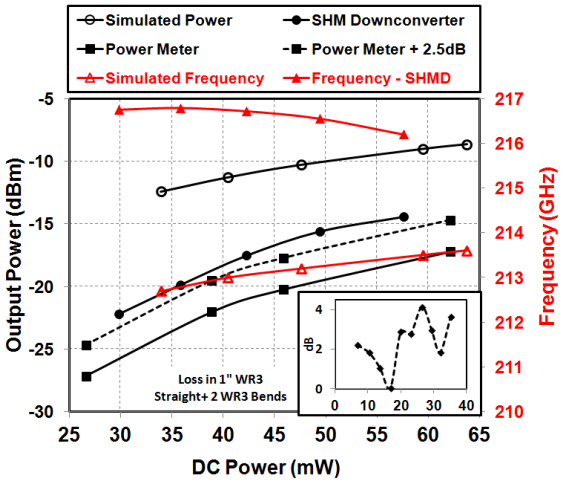

Fig. 6. Oscillator frequency and power measured by a WR3 SHMD and an Erickson PM4. Measurement details are in the text.

depicted in Fig. 6. The oscillator generates -14.4dBm of power at 216.2GHz while drawing 57.5mW of DC power. The signal source is also tested using an Erickson power meter (PM4). This second setup needs two additional WR-3 bends and a WR-3 straight, with unknown losses, for routing compared to the SHMD setup. Assuming negligible reflection, we measured their losses by performing another measurement on the oscillator with the SHMD, while including these three connected components in the WR-3 path of the mixer. The measured loss, which is the difference in the two SHMD measurements, is shown in the inset of Fig. 6. The average loss (2.5dB) agrees with the simulated loss provided by Custom Microwave. The PM4 measurement is corrected by 2.5dB. A strong agreement with the first WR-3 SHMD measurement is seen. The results also compare well with simulation.

VI. Conclusion

A -14.4dBm, 215GHz signal source using a Maximum Gain Ring Oscillator (MGRO) topology is demonstrated using the 56-nm BC devices of IBM's 45nm SOI CMOS process. The performance achieved by this CMOS source is comparable with state-of-the art CMOS sources above 200GHz [1]- [3], [6]- [7] given the DC power consumption and f_{max} of the technology employed.

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