An Improved Analysis and Design Methodology for RF Class-E Power Amplifiers with Finite DC-feed Inductance and Switch On-Resistance

Anandaroop Chakrabarti, Harish Krishnaswamy
Department of Electrical Engineering, Columbia University, New York, NY-10027

***Abstract*—Previous analytical efforts to incorporate the impact of finite switch ON-resistance into the design procedure of Class-E power amplifiers (PAs) have imposed one or both of the so-called "Class-E switching conditions", namely zero voltage switching (ZVS) and zero derivative of voltage at switching (ZDVS). These are essential for high efficiency operation only in the absence of losses. In this work, more general design equations have been derived without imposition of either ZVS or ZDVS. The optimal design is found to exhibit neither ZVS nor ZDVS, thereby validating the analysis. For the first time, an attempt has been made to incorporate the input power into the analysis, which facilitates optimization of power-added efficiency (PAE). The resulting designs exhibit better performance in terms of output power and PAE compared to existing design approaches. The analytical results have been verified through Spectre-RF simulations at 5GHz in 0.18μm and 65nm CMOS. Through this design procedure, we further demonstrate that Class-E PAs at 5GHz based on thick-oxide devices in 0.18μm CMOS, despite their lower speed, outperform those based on 65nm CMOS devices due to their higher voltage-handling capability.**

I. Introduction

The Class-E PA [1] has been the subject of extensive research owing to its potential for high-efficiency operation with a relatively simple output network. The presence of a finite DC-feed inductance, switch ON-resistance or passive loss contribute significant complexity to the mathematical analysis of the circuit. However, integrated solutions using real electron devices necessitate that these non-idealities be taken into account so as to avoid sub-optimal designs. The different sources of loss can be accounted for in 2 ways: 1) perturbation analysis, which assumes that losses are small enough so that currents and voltages remain unchanged, or 2) comprehensive circuit analysis with all parameters derived in presence of loss.

The availability of thick upper metal layers in modern fabrication technology can be exploited to implement high quality on-chip inductors (Q>15 in [2]). Consequently, perturbation analysis can be used to estimate passive loss. However, at GHz-range RF frequencies, particularly when thick-oxide devices or stacked devices are employed to increase effective breakdown voltage and output power, a comprehensive analysis for ON -resistance is essential. In [3], the authors incorporate the finite DC-feed inductance into the analysis, but compute all sources of loss perturbatively. Other works have performed a comprehensive analysis with switch ON-resistance (R_{on}) *and* finite DC-feed inductance [4]− [7], but impose one or both of the "Class-E switching conditions", namely ZVS and ZDVS. It must be emphasized that these conditions are essential for high-efficiency operation only when losses are small. In presence of appreciable R_{on}, it might be beneficial to sustain some ZVS loss in order to reduce conduction loss. In this work, we analyze the Class-E PA in the presence of a finite DC-feed inductance and finite R_{on} without the constraints of either ZVS or ZDVS.

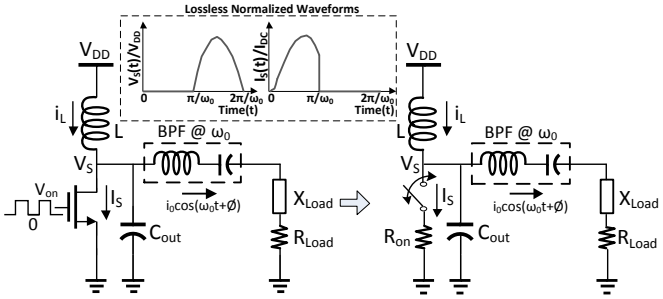

Fig. 1. Class-E PA with finite DC-feed inductance and non-zero switch on-resistance

In addition, we present the first attempt to incorporate input power into the optimization procedure. Traditional design approaches [3]− [7] have aimed to optimize for drain efficiency ($\eta = \frac{P_{out}}{P_{dc}}$). A more relevant metric for efficiency, especially for switching PAs at high frequencies, is the power-added efficiency ($PAE = \frac{P_{out}-P_{in}}{Pdc}$), since significant power has to be expended to drive the device as a switch. DC-feed inductance loss has been included in a perturbative fashion.

The improved design equations thus provide preliminary design points suitable for further optimization, thereby minimizing tedious load-pull simulations, and also enable comparison of technologies and device choices. Through this design procedure and Spectre RF simulations, we demonstrate that Class-E PAs at 5GHz based on thick-oxide devices in 0.18μm CMOS, despite their lower speed, outperform those based on 65nm CMOS devices due to their higher voltage-handling.

II. Improved Analysis of Class-E PA

A. Circuit Model and Assumptions

The circuit diagram of the Class-E CMOS PA is shown in Fig. 1. In the absence of R_{on} and passive loss, the switch

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voltage and switch current resemble those depicted in the inset in Fig. 1 when Class-E switching conditions are satisfied. For the ensuing derivations, we make the following assumptions:

1) The MOSFET can be represented by a switch with finite series ON-resistance R_{on} in parallel with a linear capacitor C_{out}.
2) $R_{on} \ll \frac{1}{\omega_0 C_{out}}$.
3) The loaded quality factor (Q_L) of the series resonant filter in the output network is large.
4) Duty-cycle of the switch is 50%, though the analysis can be extended to any arbitrary duty-cycle.
5) Filter loss is negligibly small, since filter inductance can be realized using bondwire inductance.

B. Circuit Analysis

Let us assume that the switch is open ("OFF") for $0 \leq t < \frac{T}{2}$ and closed ("ON") for $\frac{T}{2} \leq t < T$, where $T = \frac{2\pi}{\omega_0}$ is the switching period. We use the subscripts "ON" and "OFF" for voltages and currents to indicate the respective half-cycles. Using assumption 3, the load current can be represented as

$$i_{load} = i_0 \cos(\omega_0 t + \phi) \ . \tag{1}$$

During the "ON" half-cycle $\frac{T}{2} \leq t < T$, we have the following relations:

$$V_{DD} - V_{S,ON} = L\frac{di_{L,ON}}{dt} \tag{2}$$

$$\text{and} \qquad V_{S,ON} = \left(i_{L,ON} - i_0 \cos(\omega_0 t + \phi)\right) R_{on} \ . \tag{3}$$

The current through C_{out} is neglected in view of assumption 2. Using Eqn. (3), we can rewrite Eqn. (2) as

$$\frac{dV_{S,ON}}{dt} + \left(\frac{R_{on}}{L}\right) V_{S,ON} - i_0\omega_0 R_{on}\sin(\omega_0 t + \phi) - \left(\frac{V_{DD}R_{on}}{L}\right) = 0 \ . \tag{4}$$

The solution to this linear differential equation is of the form

$$V_{S,ON}(t) = V_{DD} + a_1 e^{\beta t} + a_2 \cos(\omega_0 t + \phi) + a_3 \sin(\omega_0 t + \phi) \ , \tag{5}$$

where

$$a_1 = V_{S,ON}(\frac{T}{2}) - V_{DD} - \frac{R_{on} i_0 e^{-\frac{\beta T}{2}} + \frac{\beta}{\omega_0} R_{on} i_0 e^{-\frac{\beta T}{2}} \sin(\phi)}{\left(1 + \frac{\beta^2}{\omega_0^2}\right)}$$

$$a_2 = \frac{-R_{on} i_0}{1 + \frac{\beta^2}{\omega_0^2}} \ , \ a_3 = \frac{-R_{on} i_0 \beta}{\omega_0 \left(1 + \frac{\beta^2}{\omega_0^2}\right)} \ , \ \beta = \frac{-R_{on}}{L} \ , \tag{6}$$

and $V_{S,ON}(\frac{T}{2})$ is a constant to be evaluated.

For the "OFF" half-cycle $0 \leq t < \frac{T}{2}$, when the switch is open,we can write equations identical to (2) and (3) and arrive at

$$\frac{d^2 V_{S,OFF}}{dt^2} + \frac{V_{S,OFF}}{LC_{out}} - \frac{i_0\omega_0}{C_{out}}\sin(\omega_0 t + \phi) - \frac{V_{DD}}{LC_{out}} = 0 \ . \tag{7}$$

The solution to this second order linear differential equation is given by

$$\begin{aligned} V_{S,OFF}(t) =& V_{DD}\left[1 - \cos(\omega_s t\right] + V_{S,OFF}(0)\cos(\omega_s t) \\ &+ \frac{V_{S,OFF}^{'}(0)}{\omega_s}\sin(\omega_s t) \\ &+ \frac{i_0\omega_0 \sin(\phi)}{C_{out}\left(\omega_s^2 - \omega_0^2\right)}\left[\cos(\omega_0 t) - \cos(\omega_s t)\right] \\ &+ \frac{i_0\omega_0^2\cos(\phi)}{C_{out}\left(\omega_s^2 - \omega_0^2\right)}\left[\frac{\sin(\omega_0 t)}{\omega_0} - \frac{\sin(\omega_s t)}{\omega_s}\right] \ , \end{aligned} \tag{8}$$

where $\omega_s = \frac{1}{\sqrt{LC_{out}}} = n\omega_0$, while $V_{S,OFF}(0)$ and $V_{S,OFF}^{'}(0)$ are constants to be evaluated. The values for $V_{S,ON}(\frac{T}{2})$, $V_{S,OFF}(0)$ and $V_{S,OFF}^{'}(0)$ can be arrived at by imposing the following continuity conditions:

$$i_{L,OFF}(0^+) = i_{L,ON}(T^-), V_{S,OFF}\left(0^+\right) = V_{S,ON}\left(T^-\right) \tag{9}$$

$$i_{L,OFF}(\frac{T^+}{2}) = i_{L,ON}(\frac{T^-}{2}) \ . \tag{10}$$

The load impedance Z_{load} is computed as the ratio of the fundamental component of the switch voltage to that of the load current. Since no constraints have been imposed on either the switch voltage or its derivative at switch turn-on, we need to account for possible capacitive discharge loss. Under the assumption $R_{on} \ll \frac{1}{\omega_0 C_{out}}$, this loss can be estimated as

$$P_{loss,cap} = 0.5 f_0 C_{out}\left[V_{S,OFF}^2\left(\frac{T^-}{2}\right) - V_{S,ON}^2\left(\frac{T^+}{2}\right)\right] \ . \tag{11}$$

The loss in the switch is given by

$$P_{loss,switch} = R_{on} * \frac{1}{T}\int_{\frac{T}{2}}^{T}\left(\frac{V_{S,ON}}{R_{on}}\right)^2 \ dt \ . \tag{12}$$

In order to incorporate input power into the formulation, the input power (P_{in}) is approximated as

$$P_{in} = k f_0 C_{in} V_{on}^2 \ , \tag{13}$$

where $C_{in} = C_{gs} + C_{gd}$ in the triode region, V_{on} is the input drive level in the "ON" half-cycle and k is a fitting parameter determined from schematic simulations [9]. Finite reverse isolation (i.e. $C_{gd} \neq 0$) causes the value of parameter k to vary with the parameter n (since output network component values change), but for preliminary analysis, this dependence is ignored. Finally, if $R_{choke} = \frac{\omega_0 L}{Q_{choke}}$ is the series resistance in the DC-feed inductance, its loss can be calculated using perturbation analysis as

$$P_{loss,choke} = R_{choke} * \frac{1}{T}\left(\int_0^{\frac{T}{2}} i_{L,OFF}^2 dt + \int_{\frac{T}{2}}^{T} i_{L,ON}^2 dt\right) \tag{14}$$

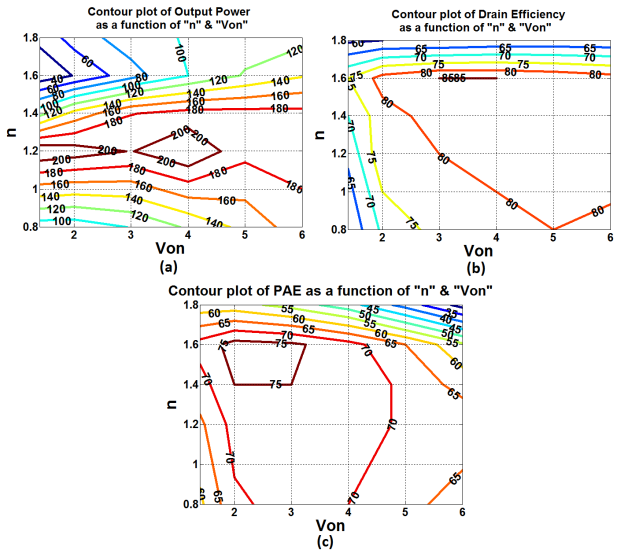

Fig. 2. (a) Output power, (b) drain efficiency, and (c) PAE for optimal Class-E PAs based on 0.7μm channel-length thick-oxide devices in IBM's 0.18μm CMOS technology as functions of V_{on} and n.

C. Optimization Procedure and Comparison to Prior Art

The circuit may now be optimized for PAE by choosing the appropriate load impedance. This is achieved by means of a MATLAB code which sweeps the magnitude i_0 and phase ϕ of the load current to arrive at a design point with optimal PAE for a given device size, input drive level V_{on} and the parameter n. A global optimization is performed subsequently by varying V_{on} and n to select the design point with highest PAE for a fixed device size. If the load impedance is different from 50Ω, then a matching network needs to be designed to perform impedance transformation. In prior works, the loss associated with this matching network has not been considered. In this work, subsequent to PAE optimization, the device size (and all other circuit components) are scaled so that $R_{load} = 50\Omega$ to determine the power that can be delivered to a 50Ω load and to eliminate the loss in a matching network.

In order to demonstrate the benefit of this improved technique, we focus on the 0.7μm channel-length thick-oxide devices in IBM's 0.18μm CMOS technology. The maximum instantaneous voltage swing in a cycle across any two device terminals is typically limited to twice the recommended V_{DD} for long-term reliability in PAs [8]. The recommended V_{DD} for these devices is 5V, making them suitable for moderate and high-power applications. $R_{on}(\Omega) = 5200/(W \times (V_{on} - V_{th}))$, where W is the device width in microns and V_{th}=0.5V, C_{out}/W=0.9fF/μm and C_{in}/W=2fF/μm. Optimal PAE designs for 5GHz Class E PAs are determined from the MATLAB code as functions of V_{on} and n (Fig. 2). Passive losses are ignored to facilitate comparison with prior art. Transient simulations are also performed in Cadence using a switch-based model with appropriate R_{on} and C_{out} for the various points in Fig. 2. These simulations show excellent agreement with theoretical results due to the comprehensive analysis.

TABLE I
COMPARISON OF THE GENERALIZED "LOSSY" CLASS-E ANALYSIS WITH PRIOR TECHNIQUES FOR 5GHZ CLASS E PAS

Technique	This work	R_{on} ignored +ZVS+ZDVS [3]	R_{on}+ZVS [7]	R_{on}+ZVS +ZDVS [6]
n	1.4	1.6	1.4	1.4
C_{out}(fF)	631	373	560	437
V_{DD}(V)	3.34	3.09	3.1	3.09
P_{dc}(mW)	217	157	231	218
P_{out}(mW)	179	125	177	161
P_{in}(mW)	15	9	14	11
η(%)	83	79	77	74
PAE(%)	75	74	71	69

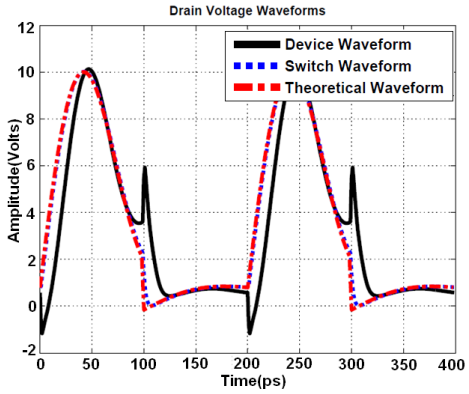

Fig. 3. Drain voltage waveforms for optimized device-based design vs. theoretical and switch-based simulations

From the contour plots, it is evident that for a fixed n, there exists an optimum value for V_{on} which maximizes PAE, since an increase in V_{on} is accompanied by an increase in input power. For a fixed V_{on}, PAE reaches a maximum for a certain optimum value of n. This is in contrast to the analysis of [3], where η increases uniformly with n when only device loss is present. This is a consequence of incorporating passive loss as well as optimization of PAE, since output power reduces significantly for high values of n.

Table I compares the theoretical PAE-optimal design point from the presented methodology with those resulting from prior art, all designs being scaled to drive a load with $R_{load} = 50\Omega$. Evidently, our approach results in the highest efficiency numbers, and while the work in [3] results in a PAE that is similar, the output power is much higher in our approach.

III. TECHNOLOGY COMPARISON FOR RF CLASS-E PAS

Integrated GHz-range wireless transmitters are often implemented in deeply-scaled CMOS technologies due to the benefits enjoyed by digital and mixed-signal circuitry. While deeply-scaled CMOS devices exhibit high speed and low loss, they suffer from low breakdown voltages, limiting the output power that can be generated in a power amplifer. Stacking two or more devices helps increase the overall voltage swing and output power [8], [10]. In this section, the developed Class-E design methodology is used to compare the 0.7μm thick-oxide devices in IBM's 0.18μm CMOS technology with

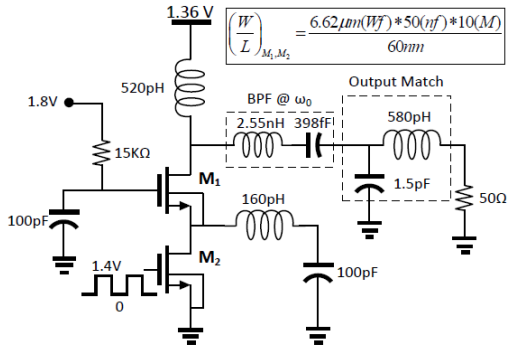

Fig. 4. Circuit diagram for 2-stacked class-E PA in 65nm CMOS technology

TABLE II
COMPARISON OF 5GHZ CLASS-E PA USING THICK-OXIDE 0.7μM CHANNEL-LENGTH DEVICES IN 0.18μM CMOS VS. THIN-OXIDE DEVICES IN 65NM CMOS

Technology	0.18μm CMOS		65nm CMOS	
	Switch	Device	Switch	Device
n	1.2	1.2	1.4	1.4
Device size(μm)	600	600	3310	3310
L(nH)	1.3	2.61	0.24	0.52
V_{DD}(V)	3.77	3.77	1.36	1.36
$R_{load}(\Omega)$	50	50	8	8
P_{dc}(mW)	296	257	296	351
P_{out}(mW)	202	169	202	161
P_{in}(mW)	13	35.9	13	19
$\eta(\%)$	68	66	68	46
PAE(%)	64	52	64	40

the thin-oxide devices in IBM's 65nm CMOS technology ($R_{on} \times W$=820Ω-μm for V_{gs}=1V and C_{out}/W=0.48fF/μm).

The design procedure described in the previous section is used to find a PAE-optimal design point at 5GHz for the 0.7μm thick-oxide device. Passive losses are included in the design procedure with a Q_{choke} of 15. The output series filter inductance is assumed to be obtained through the output bondwire. Integrated capacitors at 5GHz typically have negligible loss levels. This PAE-optimal design point is used as the starting point for realistic design that utilizes PDK device models and is simulated in Spectre RF. Practical design issues, such as non-ideal switching characteristics and finite reverse isolation of the device, require minor modifications to the circuit parameters. A comparison between the theoretical PAE-optimal design point, simulations based on an ideal switch-based model and the PDK-model-based design is summarized in Fig. 3 and Table II. A very close agreement is seen, proving the usefulness of the methodology as a starting point for realistic yet optimal designs.

For theoretical analysis, a stacked configuration of two 65nm CMOS devices is assumed to behave as a switching device with the C_{out} and twice the R_{on} of each device, along with twice the output voltage swing allowed for a single device. This results in a maximum swing of 4V at the output since the recommended V_{DD} is 1V for a single device. A PAE-optimal design point at 5GHz is obtained from the design procedure and is summarized in Table II. Due to the relatively lower voltage swing of a stack of two 65nm CMOS devices, the 50Ω load must transformed to an 8Ω impedance to achieve an output power of 200mW to match the performance of the 0.7μm thick-oxide device. This matching network is assumed to be implemented using low-loss off-chip components. This design point is used as a starting point for a realistic PDK-based design (Fig. 4). The use of an inductor at the intermediary node of the stacked devices [8] and a source-bulk connection for the cascode triple-well device [10] is required for optimal performance of the stacked Class E PA.

Interestingly, though the theoretical results in the two technologies compare well, actual simulation results clearly indicate the benefit of using a slower device with larger output swing in 0.18μm CMOS. This is due to the degradation in performance seen in a realistic stacked 65nm CMOS design. This degradation is associated with the swing of the intermediary node, and the resultant delayed turn-off and early turn-on of the cascode device, resulting in extra conduction loss [8], [10]. Also, the stacked 65nm CMOS design requires external matching components to be competitive in output power.

IV. CONCLUSION

An improved analysis technique and design methodology for Class-E PAs is proposed. For the first time, input power is incorporated as an integral component in the optimization procedure. Analytical results are verified by means of Spectre RF simulations, which indicate the benefit of this technique compared to existing work. A comparison of two different CMOS technologies is conducted to demonstrate the usefulness of the proposed design procedure in deciding on an appropriate technology for a specified output power.

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