

Fabrication Technology

By

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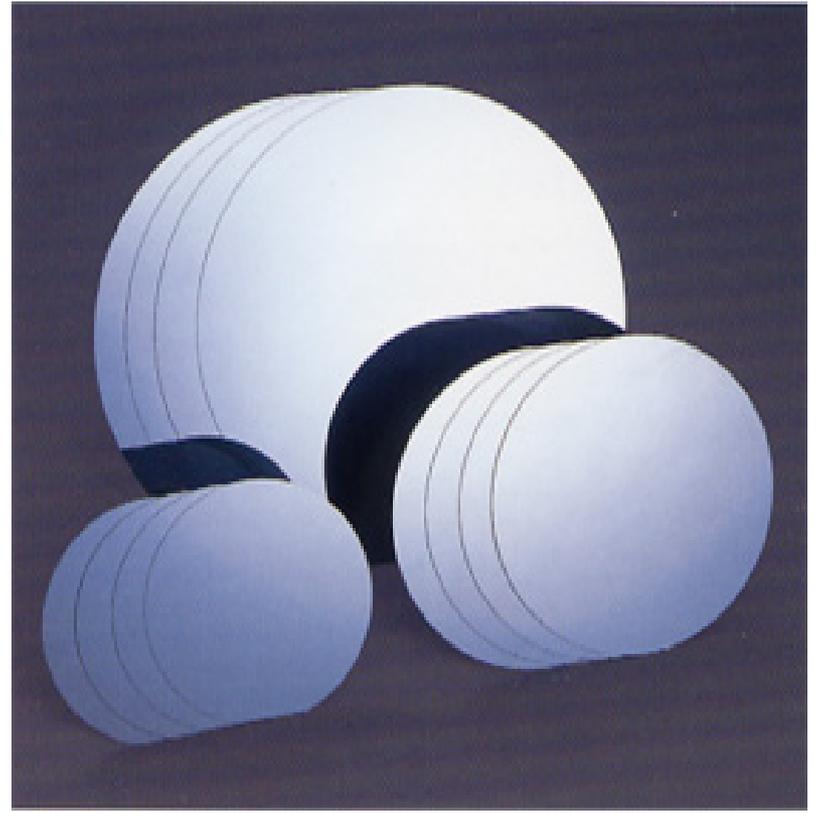
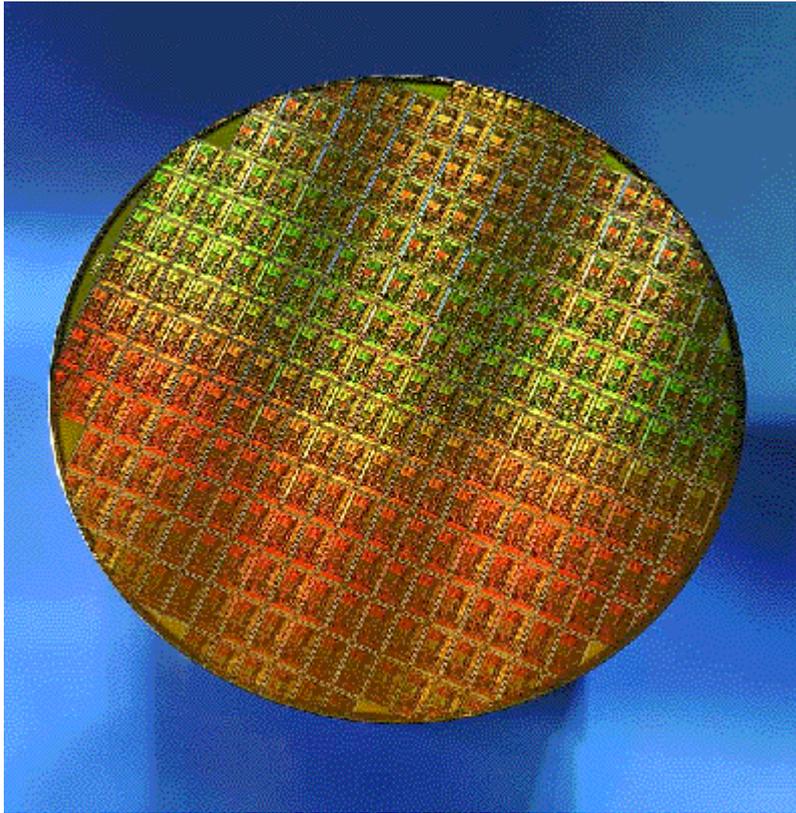
OUTLINE

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- Planar PN junction diode fabrication,
- Fabrication of resistors and capacitors in IC's.

INTRODUCTION

- The microminiaturization of electronics circuits and systems and then concomitant application to computers and communications represent major innovations of the twentieth century. These have led to the introduction of new applications that were not possible with discrete devices.
- Integrated circuits on a single silicon wafer followed by the increase of the size of the wafer to accommodate many more such circuits served to significantly reduce the costs while increasing the reliability of these circuits.



WHY SILICON?

Semiconductor devices are of two forms

- (i) Discrete Units
- (ii) Integrated Units

Discrete Units can be diodes, transistors, etc.

Integrated Circuits uses these discrete units to make one device.

Integrated Circuits can be of two forms

- (i) **Monolithic**-where transistors, diodes, resistors are fabricated and interconnected on the same chip.
- (ii) **Hybrid**- in these circuits, elements are discrete form and others are connected on the chip with discrete elements externally to those formed on the chip

- ✓ Two other semiconductors, germanium and gallium arsenide, present special problems while silicon has certain specific advantages not available with the others.
- ✓ A major advantage of silicon, in addition to its abundant availability in the form of sand, is that it is possible to form a superior stable oxide, SiO_2 , which has superb insulating properties.
- ✓ Gallium arsenide crystals have a high density of crystal defects, which limit the performance of devices made from it.
- ✓ Compound semiconductors, such as GaAs (in contrast to elemental semiconductors such as Si and Ge) are much more difficult to grow in single crystal form.
- ✓ Both Si and Ge do not suffer, in the processing steps, from possible decomposition that may occur in compound semiconductors such as GaAs.
- ✓ Lastly, at the present time, silicon remains the major semiconductor in the industry.

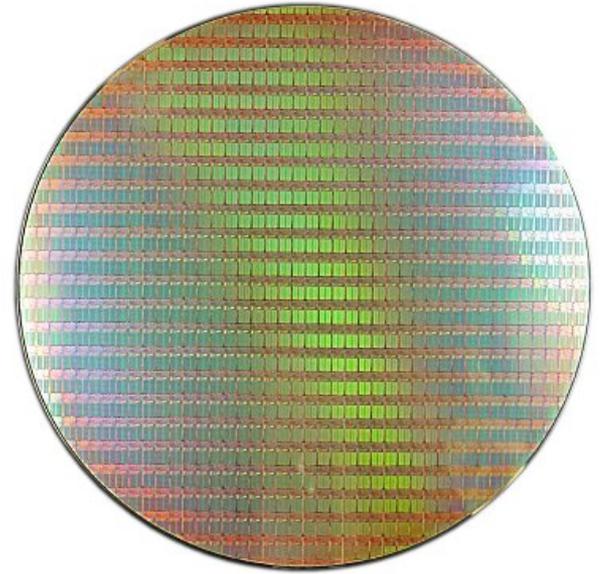
THE PURITY OF SILICON

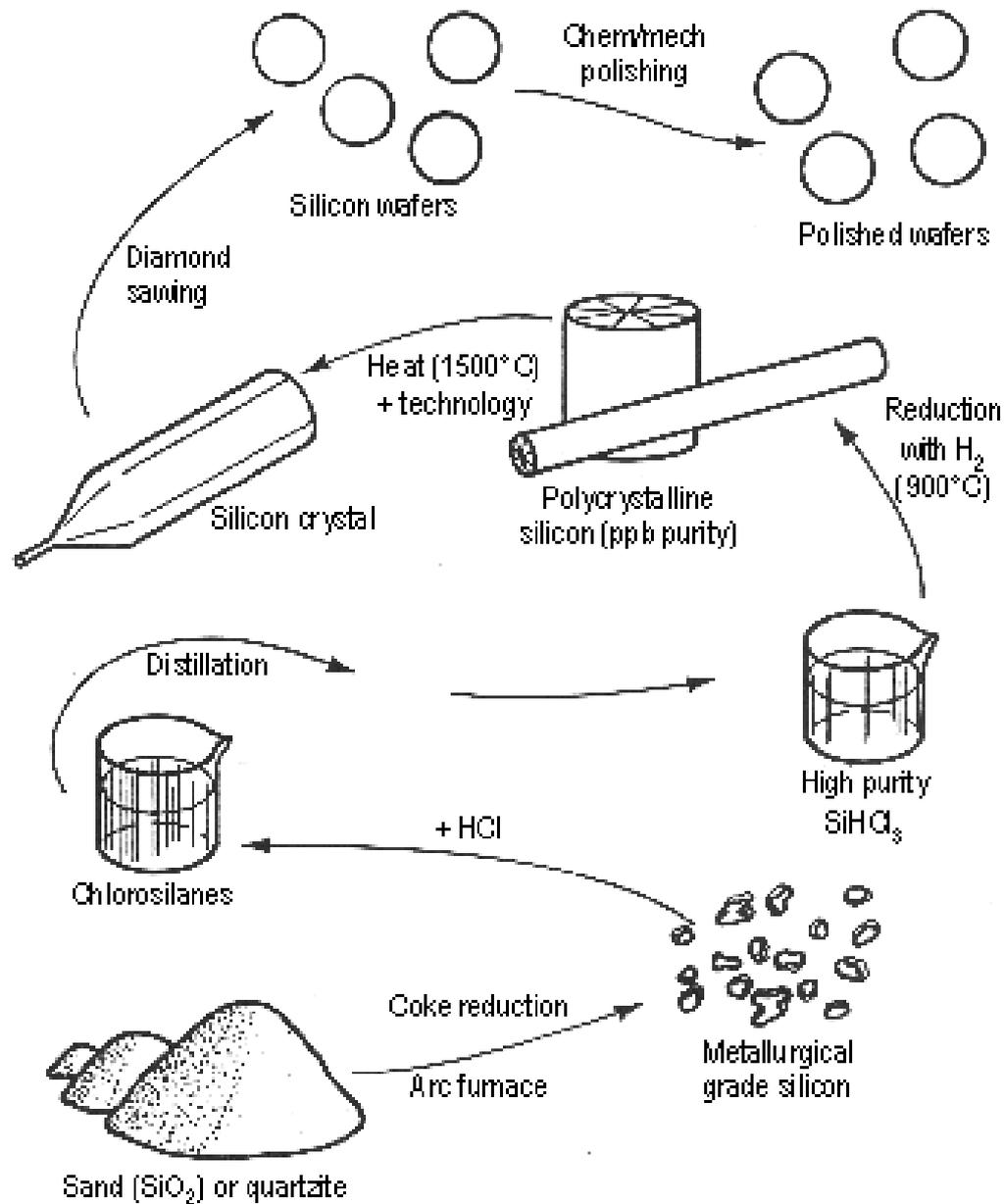
- ❑ The starting form of silicon, which manufacturers of devices and integrated circuits use, is a circular slice known as a *wafer*.
- ❑ These wafer diameters vary from 10-20 cms with maximum up to 30 cms.
- ❑ Silicon is found in abundance in nature as an oxide in sand and quartz.
- ❑ Silicon must be in
 - ✓ Crystalline form,
 - ✓ Very pure,
 - ✓ Free of defects, and
 - ✓ Uncontaminated.

Silicon From Sand



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The Czochralski Process

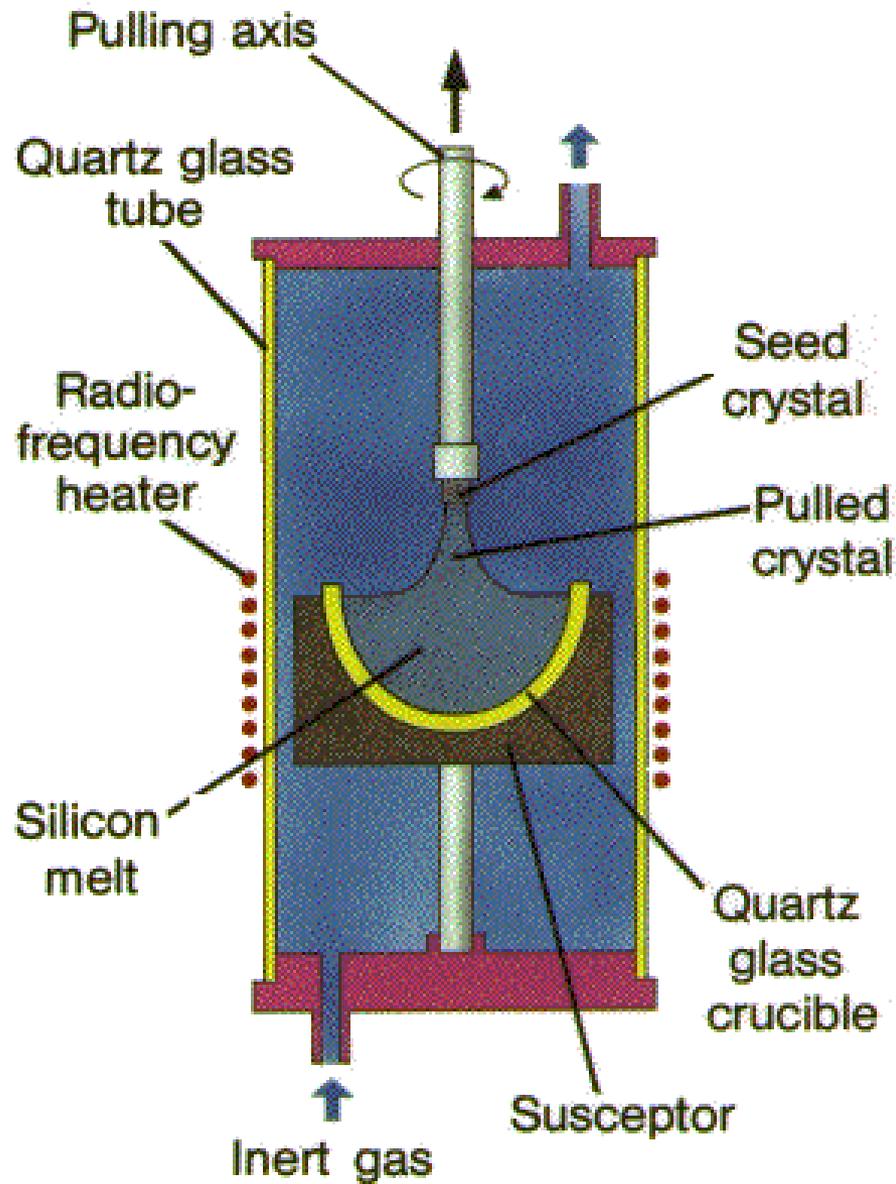
- ❑ To grow crystals, one starts with very pure semiconductor grade silicon, which is melted in a quartz-lined graphite crucible. The melt is held at a temperature of 1690K, which is slightly greater than the melting point (1685K) of silicon.
- ❑ A precisely controlled quantity of the dopant is added to the melt
- ❑ The ratio of the concentration of impurities in the solid, C_o to that in the liquid, C_l is known as the equilibrium segregation coefficient k_o

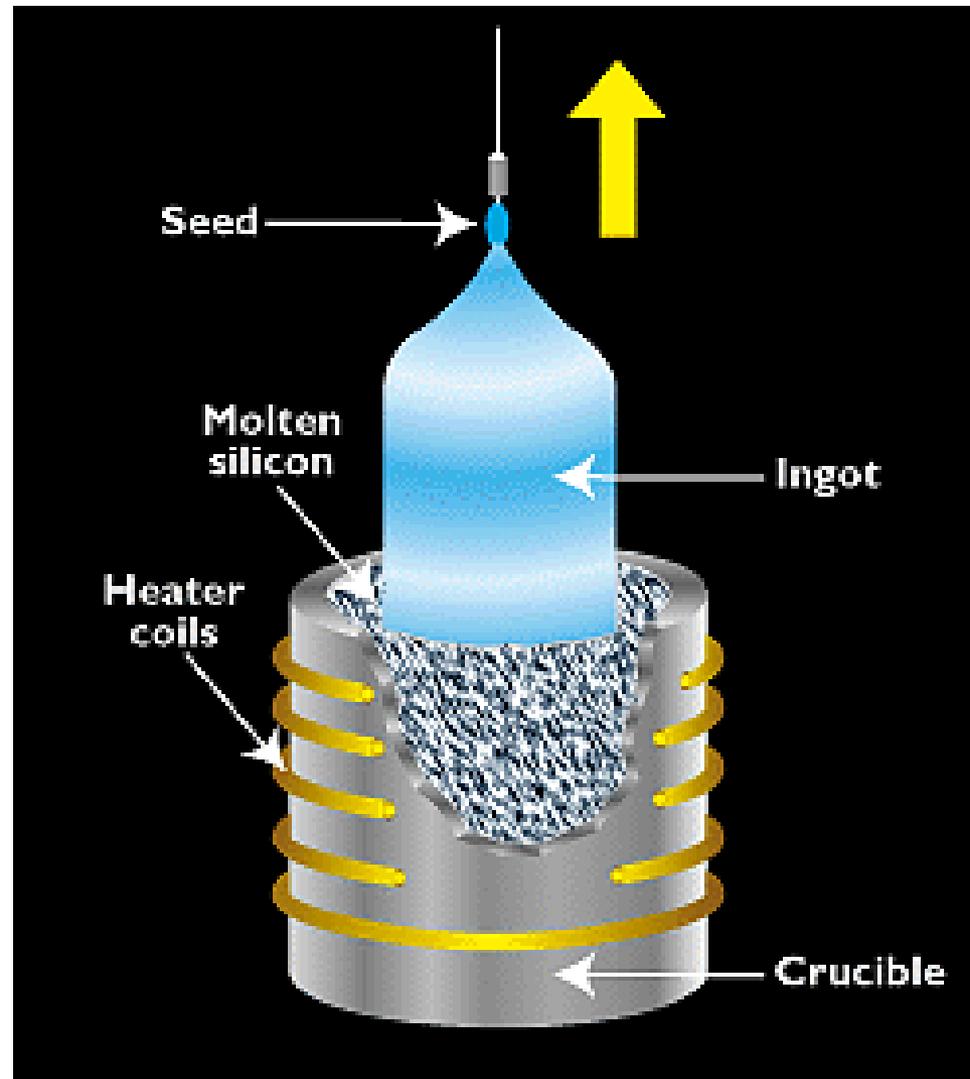
$$k_o = C_o / C_l$$

Seed Crystal

After having set up the melt, a seed crystal (a small highly perfect crystal), attached to a holder and possessing the desired crystal orientation, is dipped into the melt and a small portion is allowed to melt.



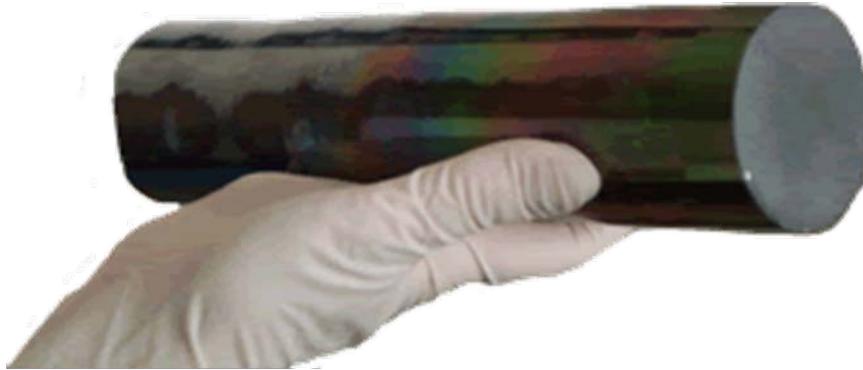




Here is a picture of a state-of-the-art **200 mm Si** crystal as they are grown by the thousands for present day (2000) chip manufacture.



Ingot Slicing and Wafer Preparation



- ❖ In the final process, when the bulk of the melt has been grown, the crystal diameter is decreased until there is a point contact with the melt.
- ❖ The resulting ingot is cooled and removed to be made into wafers. The ingots have diameters as large as 200mm, with latest ones approaching 300mm. The ingot length is of the order of 100cm.

- ❑ Slicing the wafers to be used in the fabrication of integrated circuits is a procedure that requires precision equipment.
- ❑ The object is to produce slices that are perfectly flat and as smooth as possible, with no damage to the crystal structure.
- ❑ The wafers need to be subjected to a number of steps known as lapping, polishing, and chemical etching.
- ❑ The wafers are cleaned, rinsed, and dried for use in the fabrication of discrete devices and integrated circuits



FABRICATION PROCESS

Oxidation

The process of oxidation consists of growing a thin film of silicon dioxide on the surface of the silicon wafer.

Diffusion

This process consists of the introduction of a few tenths to several micrometers of impurities by the solid-state diffusion of dopants into selected regions of a wafer to form junctions.

Ion Implantation

This is a process of introducing dopants into selected areas of the surface of the wafer by bombarding the surface with high-energy ions of the particular dopant.

Photolithography

In this process, the image on the reticle is transferred to the surface of the wafer.

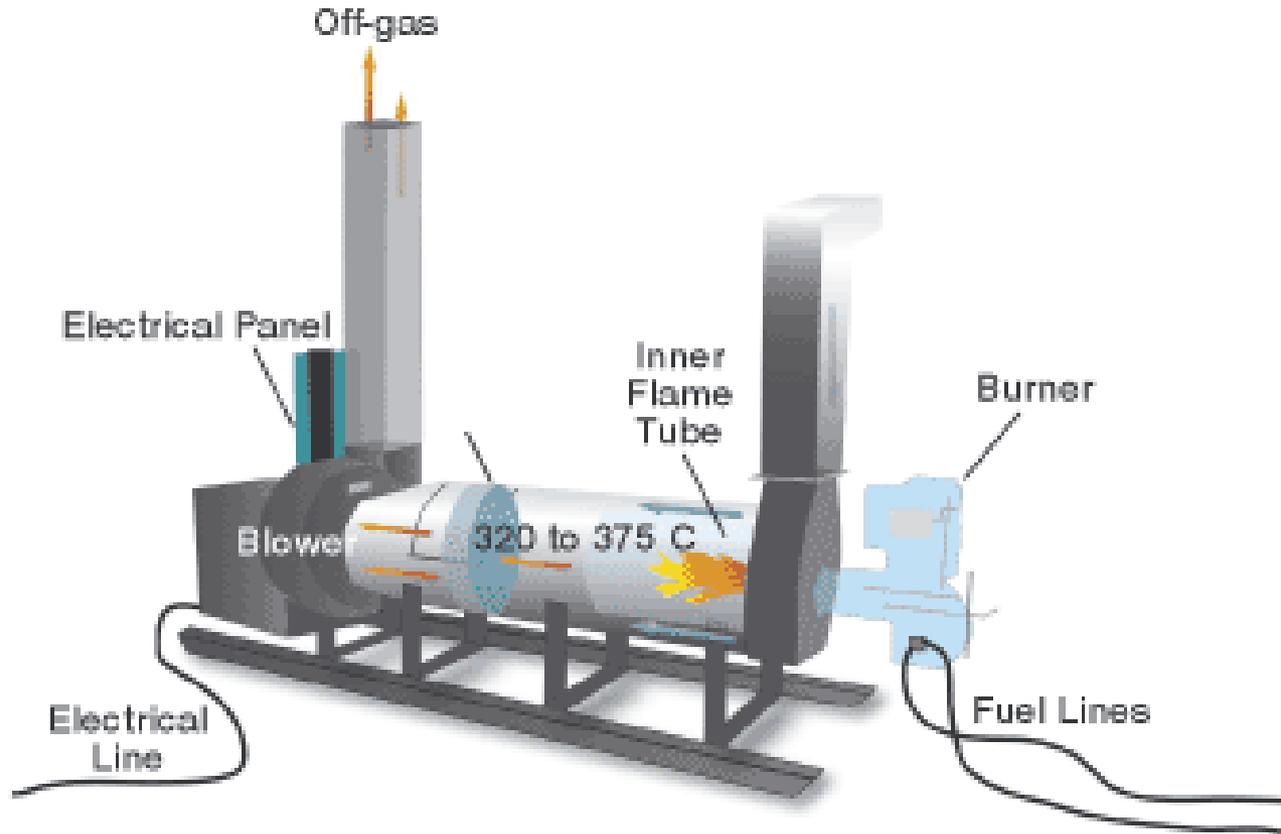
Epitaxy

Epitaxy is the process of the *controlled growth* of a crystalline doped layer of silicon on a single crystal substrate.

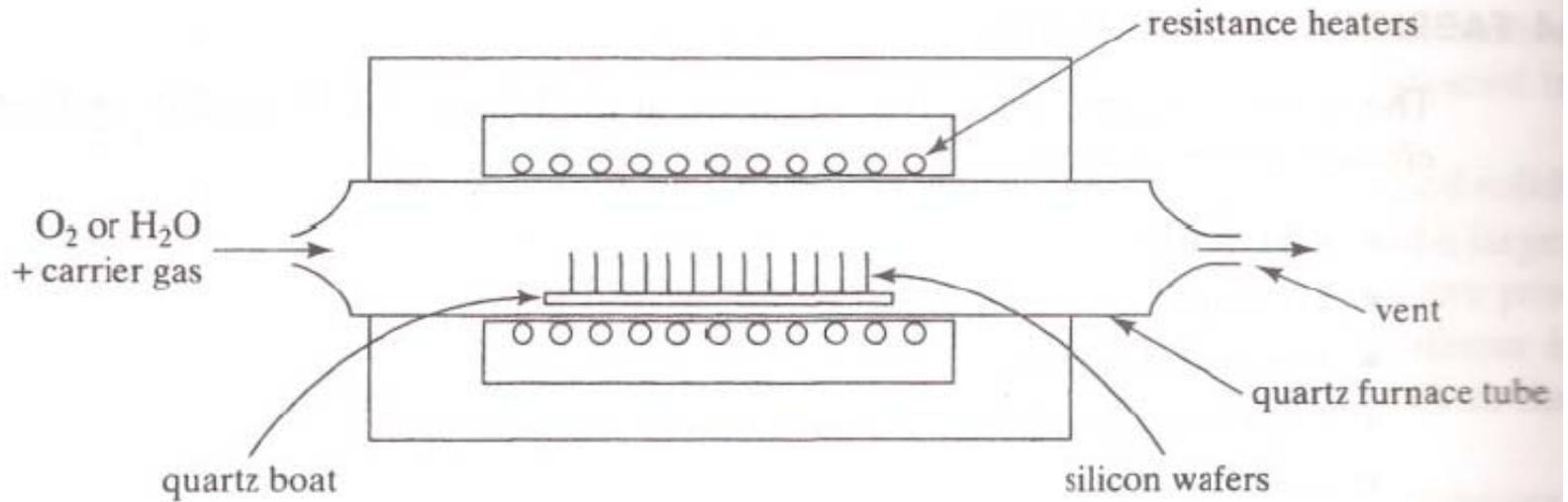
Metallization and interconnections

After all semiconductor fabrication steps of a device or of an integrated circuit are completed, it becomes necessary to provide metallic interconnections for the integrated circuit and for external connections to both the device and to the IC.

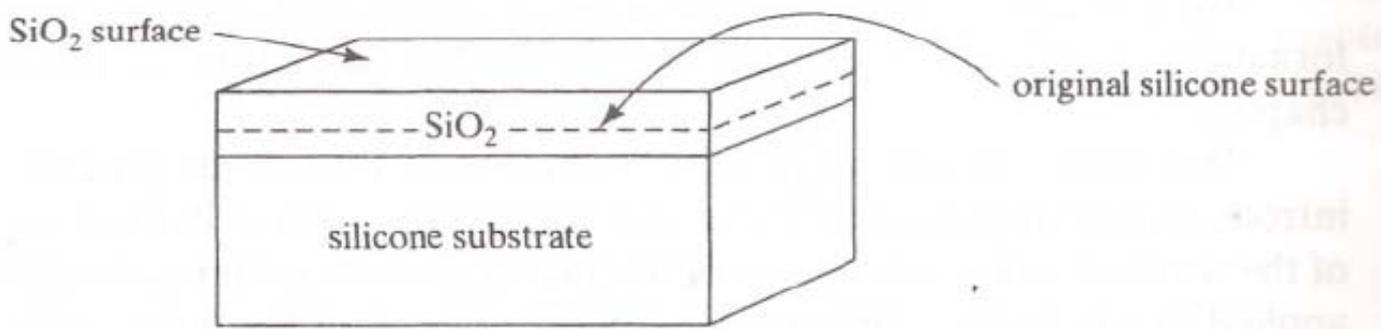
Thermal Oxidation



Silicon dioxide, as we shall see later, plays an important role in shielding of the surface so that dopant atoms, by diffusion or ion implantation, may be driven into other selected regions



(a)



(b)

Etching Techniques

Etching is the process of selective removal of regions of a semiconductor, metal, or silicon dioxide.

There are two types of etchings: *wet* and *dry*

In wet etching, the wafers are immersed in a chemical solution at a predetermined temperature. In this process, the material to be etched is removed equally in all directions so that some material is etched from regions where it is to be left. This becomes a serious problem when dealing with small dimensions.

In dry (or plasma) etching, the wafers are immersed in a gaseous plasma created by a radio-frequency electric field applied to a gas such as argon. Electrons are initially released by field emission from an electrode. These electrodes gain kinetic energy from the field, collide with, and transfer energy to the gas molecules, which results in generating ions and electrons. The newly generated electrons collide with other gas molecules and the avalanche process continues throughout the gas, forming a plasma. The wafer to be etched is placed on an electrode and is subjected to the bombardment of its surface by gas ions. As a result, atoms at or near the surface to be etched are removed by the transfer of momentum from the ions to the atoms.

Diffusion

- Most of these diffusion processes occur in two steps: the *predeposition* and the *drive-in* diffusion.
- In the *pre deposition step*, a high concentration of dopant atoms are introduced at the silicon surface by a vapor that contains the dopant at a temperature of about 1000°C. In recent years Ion Implantation is used.
- At the temperature of 1000°C, silicon atoms move out of their lattice sites creating a high density of vacancies and breaking the bond with the neighboring atoms.
- The second step is drive in process, used to drive the impurities deeper into the surface without adding anymore impurities.
- Common dopants are boron for P-type layers and phosphorus, antimony, and arsenic for N-type layers.
- A typical arrangement of the process of diffusion is shown in Figure.
- The wafers are placed in a quartz furnace tube that is heated by resistance heaters surrounding it. So that the wafers may be inserted and removed easily from the furnace, they are placed in a slotted quartz carrier known as a boat. To introduce a phosphorus dopant, as an example, phosphorus oxychloride

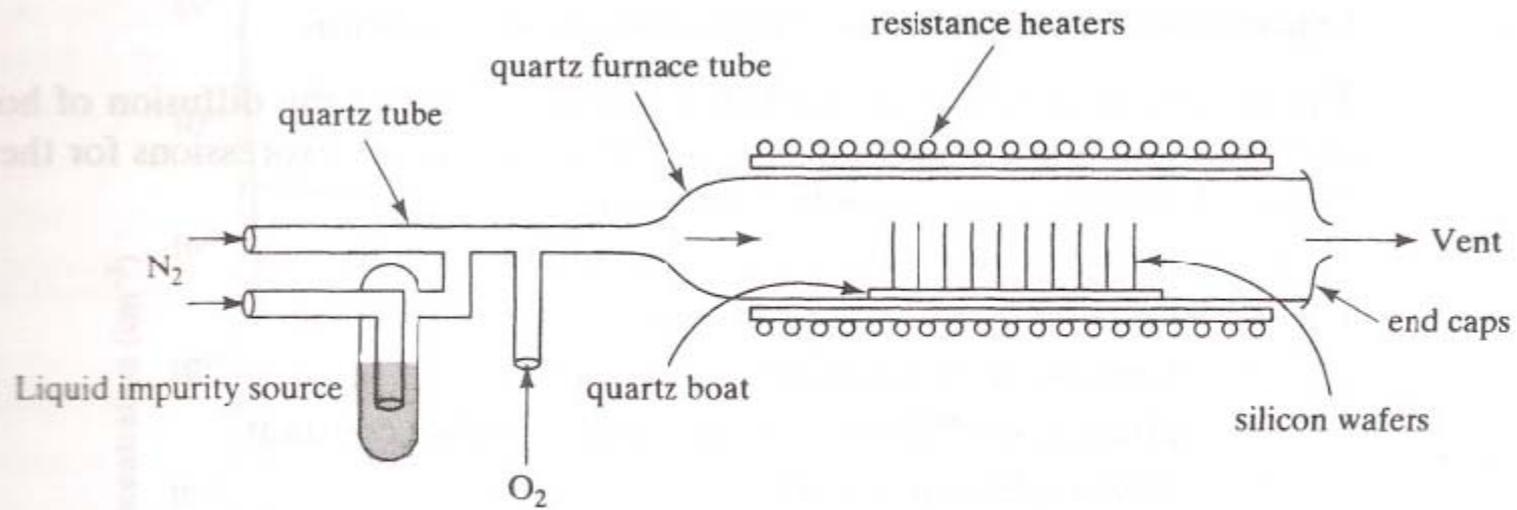
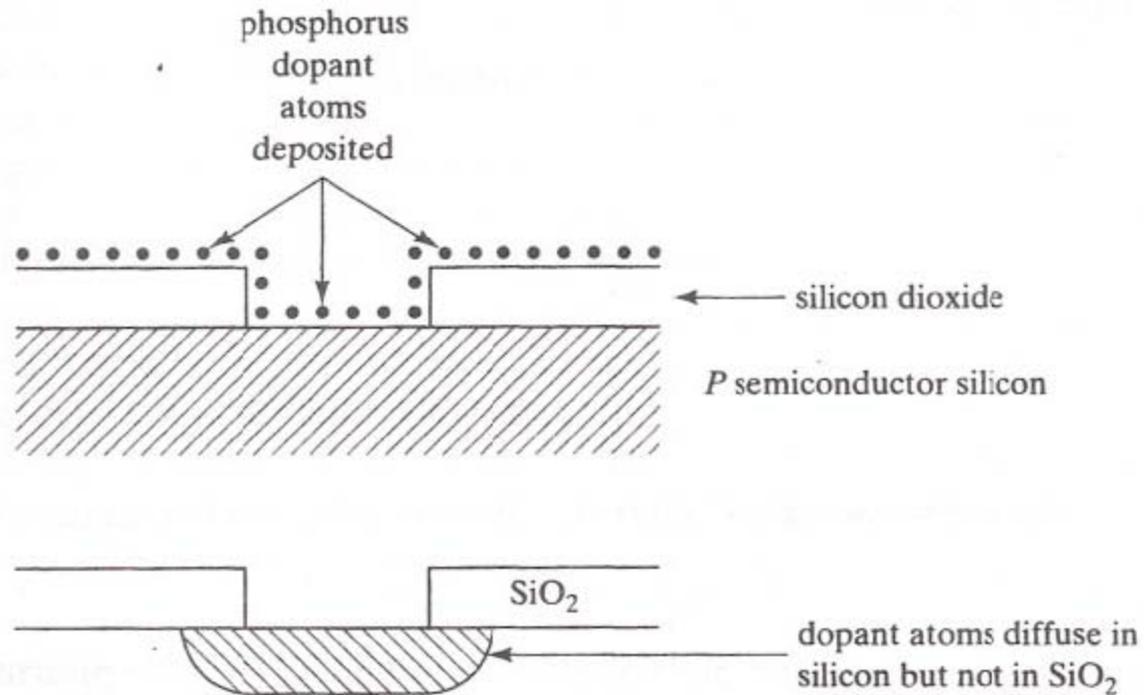


Figure 6.5 Physical layout of equipment used in diffusion.



- (POCl₃) is placed in a container either inside the quartz tube, in a region of relatively low temperature, or in a container outside the furnace at a temperature that helps maintain its liquid form.
- Nitrogen and oxygen gas are made to pass over the container. These gases
- carry the dopant vapor into the furnace, where the gases are deposited on the surface of the wafers. These gases react with the silicon, forming a layer on the surface of the wafer that contains silicon, oxygen, and phosphorus. At the high temperature of the furnace, phosphorus diffuses easily into the silicon.
- Diffusion depth is controlled by the time and temperature of the drive-in process.
- By precise control of the time and temperature (to within 0.25°C), accurate junction depths of fraction of a micron can be obtained.

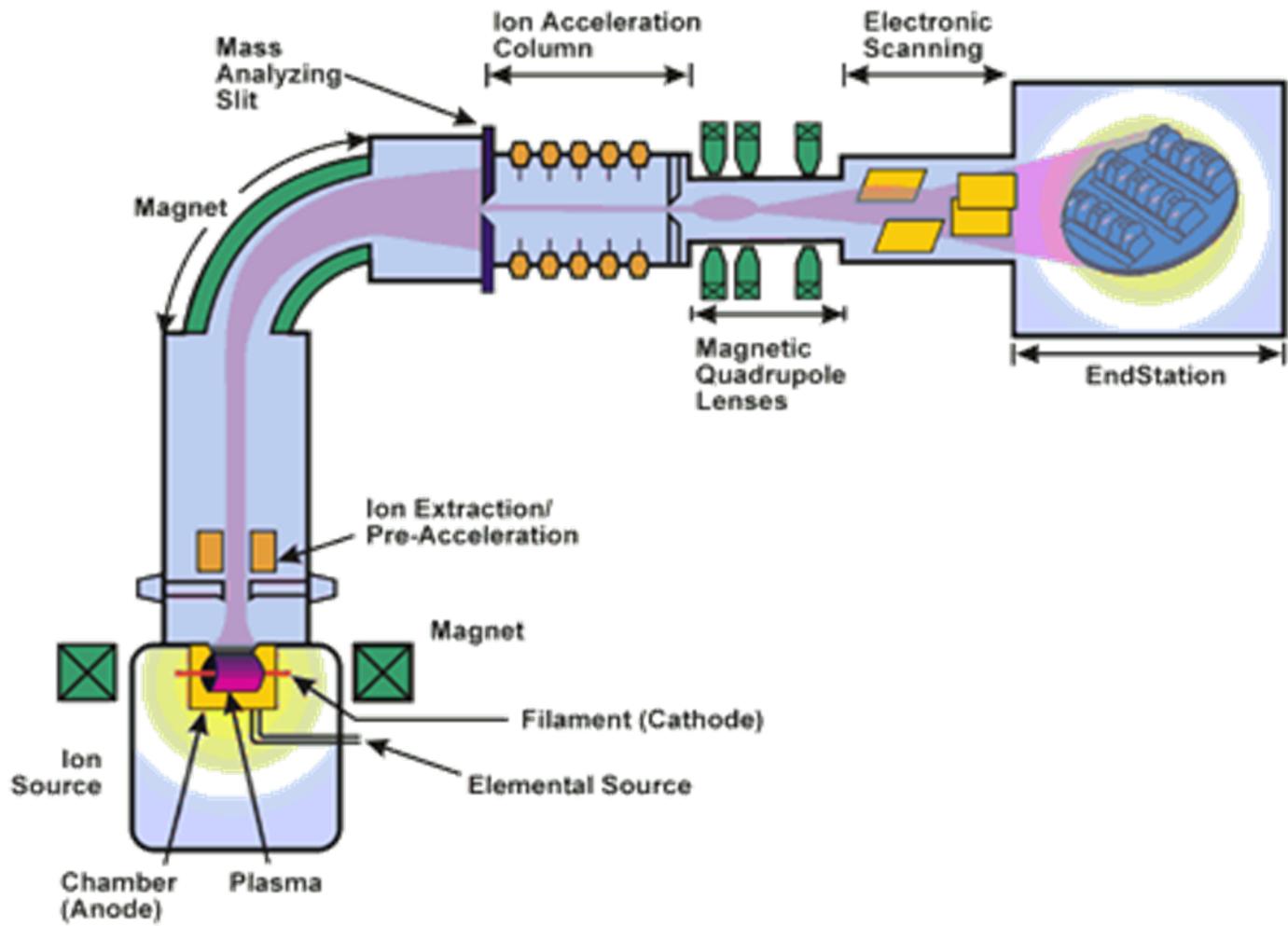
Ion Implantation

To generate ions, such as those of phosphorus, an arc discharge is made to occur in a gas, such as phosphine (PH_3), that contains the dopant.

The ions are then accelerated in an electric field so that they acquire an energy of about 20keV and are passed through a strong magnetic field.

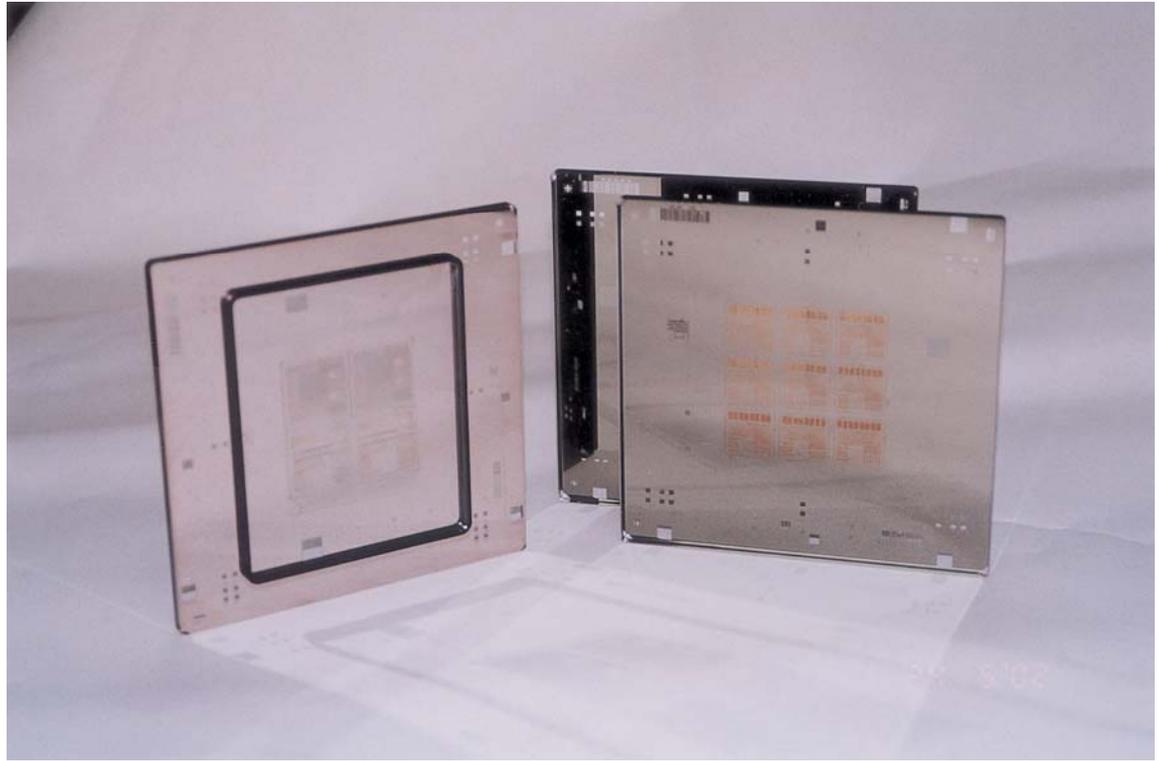
Because during the arc discharge unwanted impurities may have been generated, the magnetic field acts to separate these impurities from the dopant ions based on the fact that the amount of deflection of a particle in a magnetic field depends on its mass.

Following the action of the magnetic field, the ions are further accelerated so that their energy reaches several hundred keV, whereupon they are focused on and strike the surface of the silicon wafer.



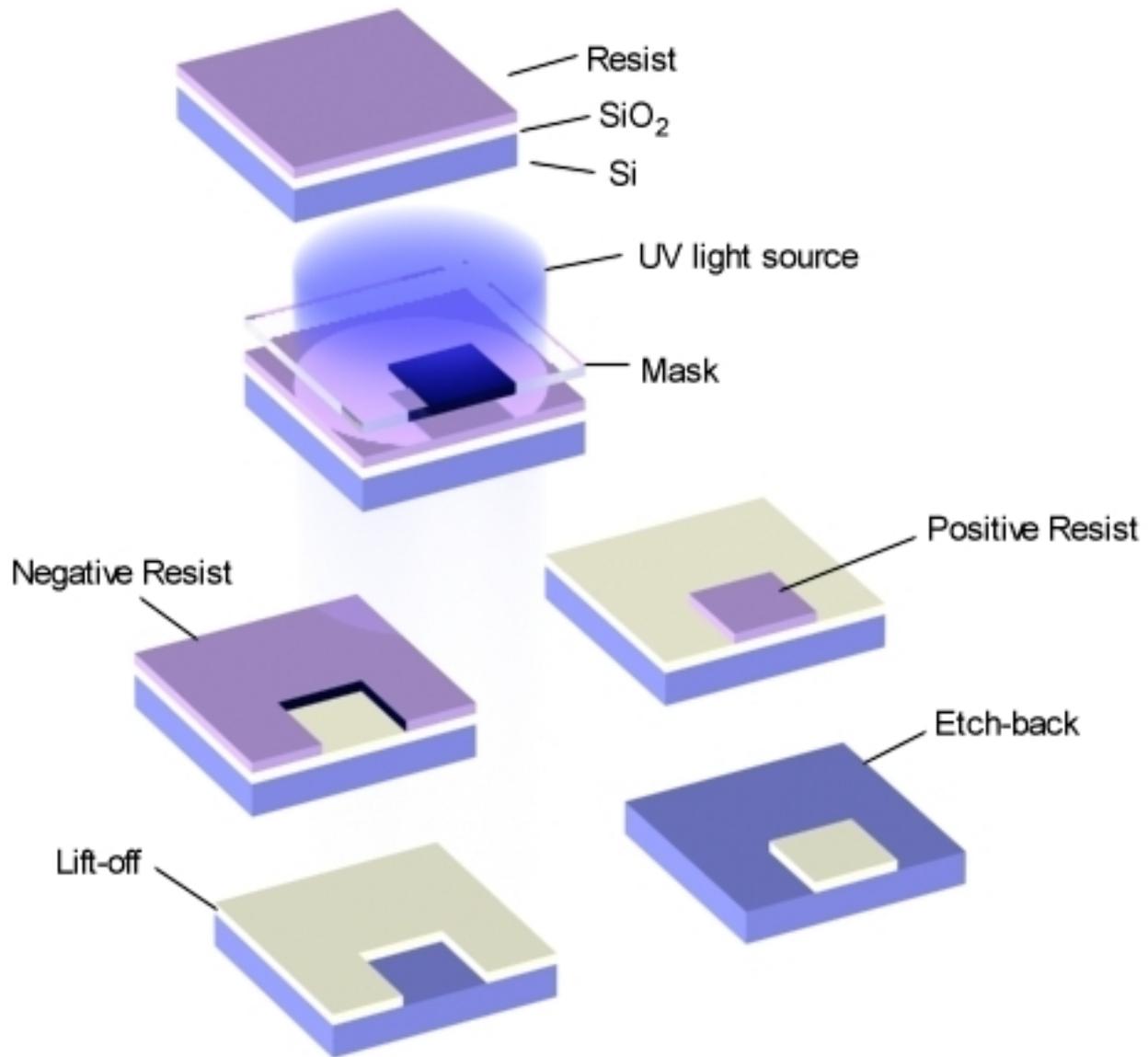
Advantages of Ion Implantation

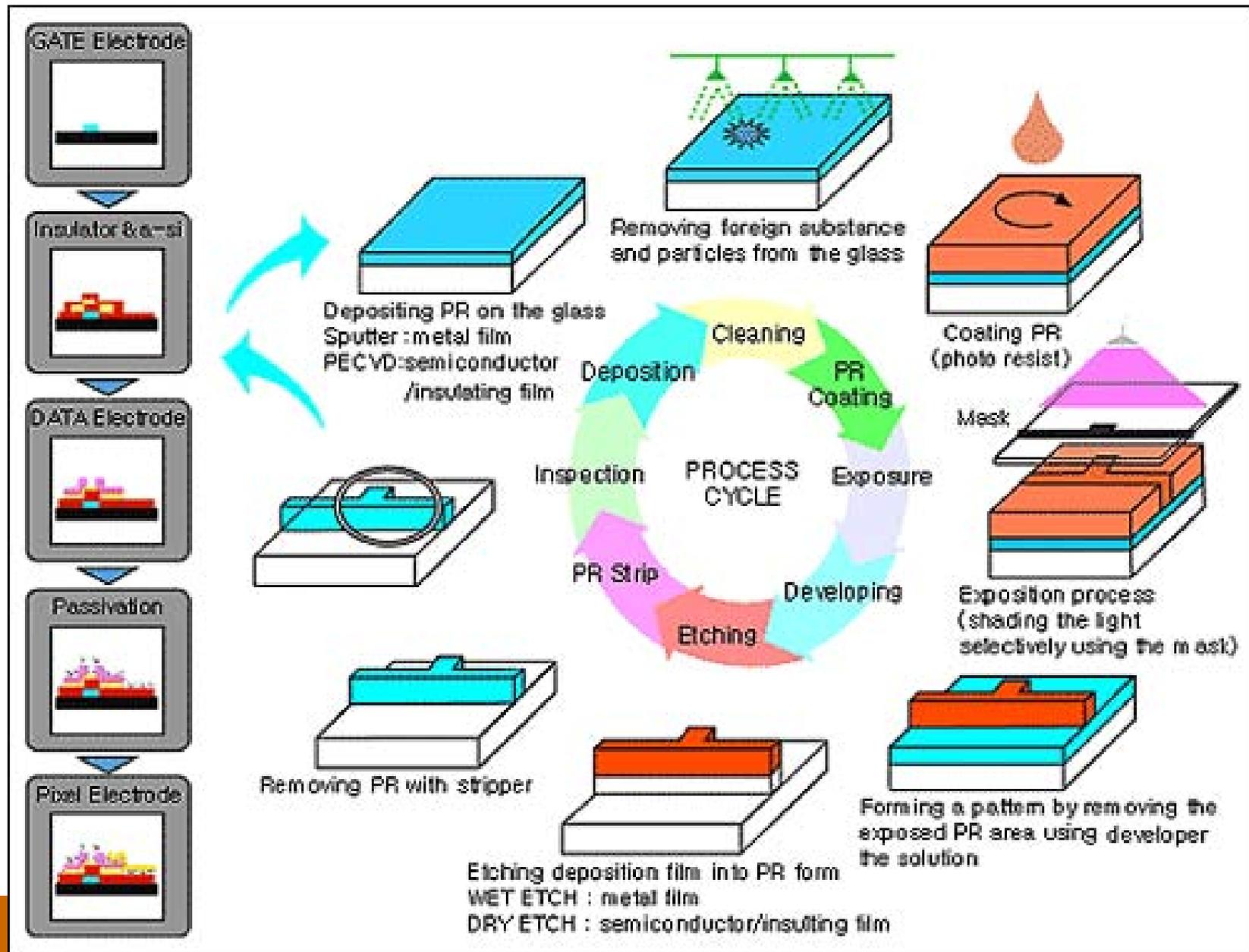
1. Doping levels can be precisely controlled since the incident ion beam can be accurately measured as an electric current.
2. The depth of the dopant can be easily regulated by control of the incident ion velocity. It is capable of very shallow penetrations.
3. Extreme purity of the dopant is guaranteed.
4. The doping uniformity across the surface can be accurately controlled.
5. Because the ions enter the solid as a directed beam, there is very little spread of the beam, thus the doping area can be clearly defined.
6. Since this is a low-temperature process, the movement of impurities is minimized.

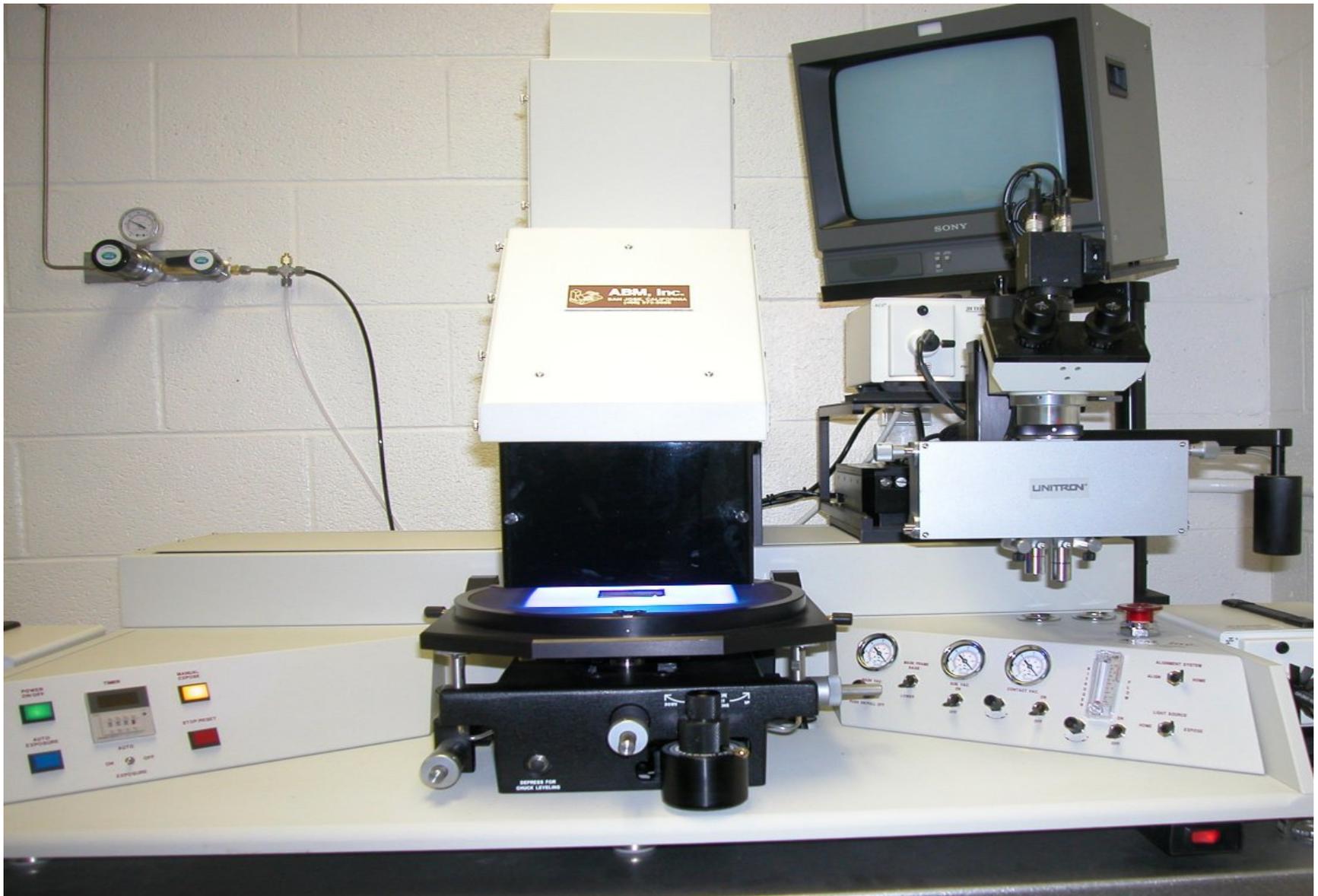


Photolithography

1. The wafer is baked at 100°C to solidify the resist on the wafer.
2. The reticle is placed on the wafer and aligned by computer control.
3. The reticle is exposed to ultraviolet light with the transparent parts of the reticle passing the light onto the wafer. The photoresist under the opaque regions of the reticle is unaffected.
4. The exposed photoresist is chemically removed by dissolving it in an organic solvent and exposing the silicon dioxide underneath. This is a process very similar to that used in developing photographic film.
 - The exposed silicon dioxide is then etched away using hydrofluoric acid, which
 - dissolves silicon dioxide and not silicon. The regions under the opaque part of
 - the reticle are still covered by the silicon dioxide and the photoresist.
 - The photoresist under the opaque regions of the reticle is stripped using a
 - proper solvent and the silicon dioxide is exposed.







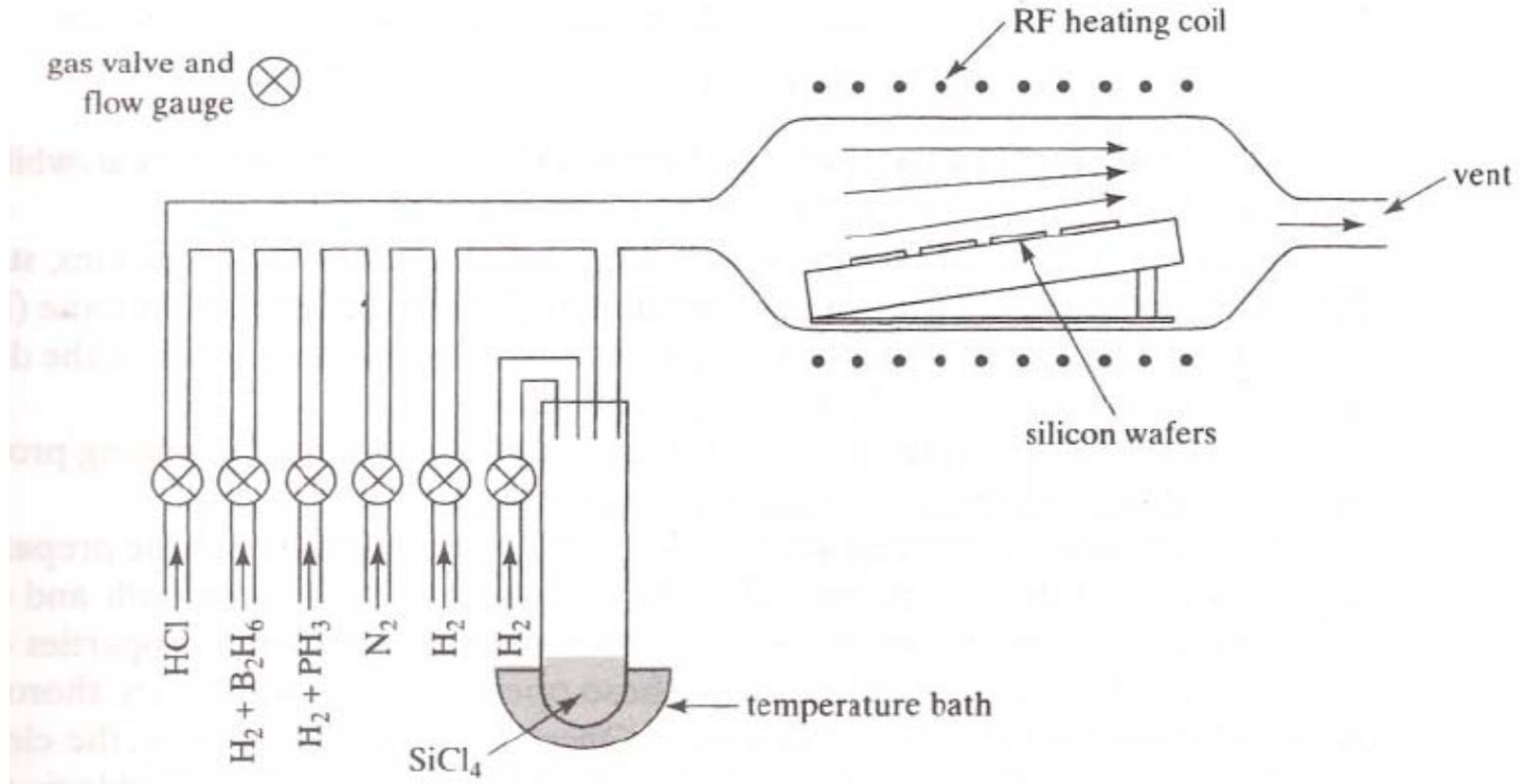
Deep UV Photolithography

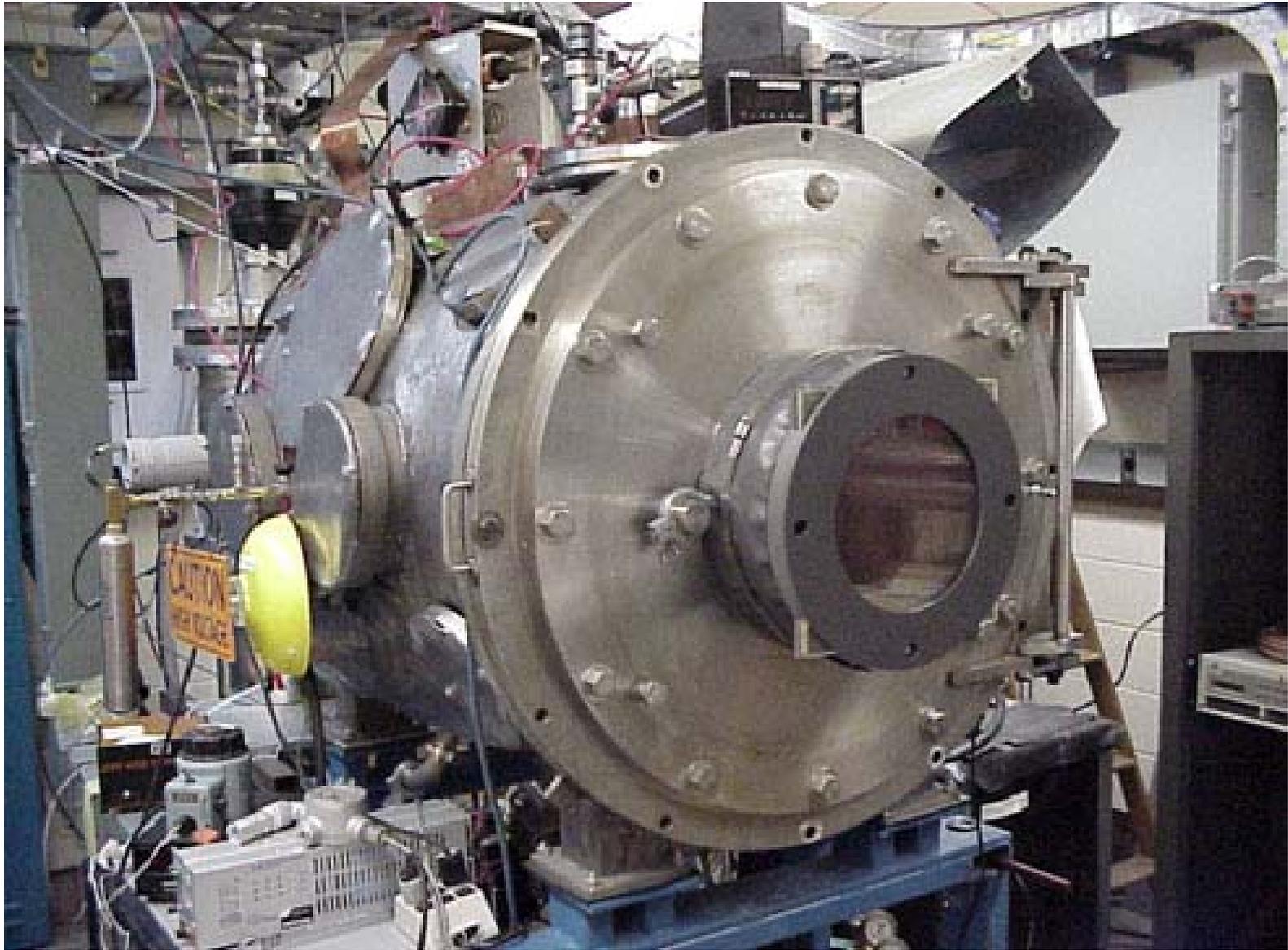
Epitaxial Growth

Epitaxy is used to deposit N on N⁺ silicon, which is impossible to accomplish by diffusion. It is also used in isolation between bipolar transistors wherein N⁻ is deposited on P.

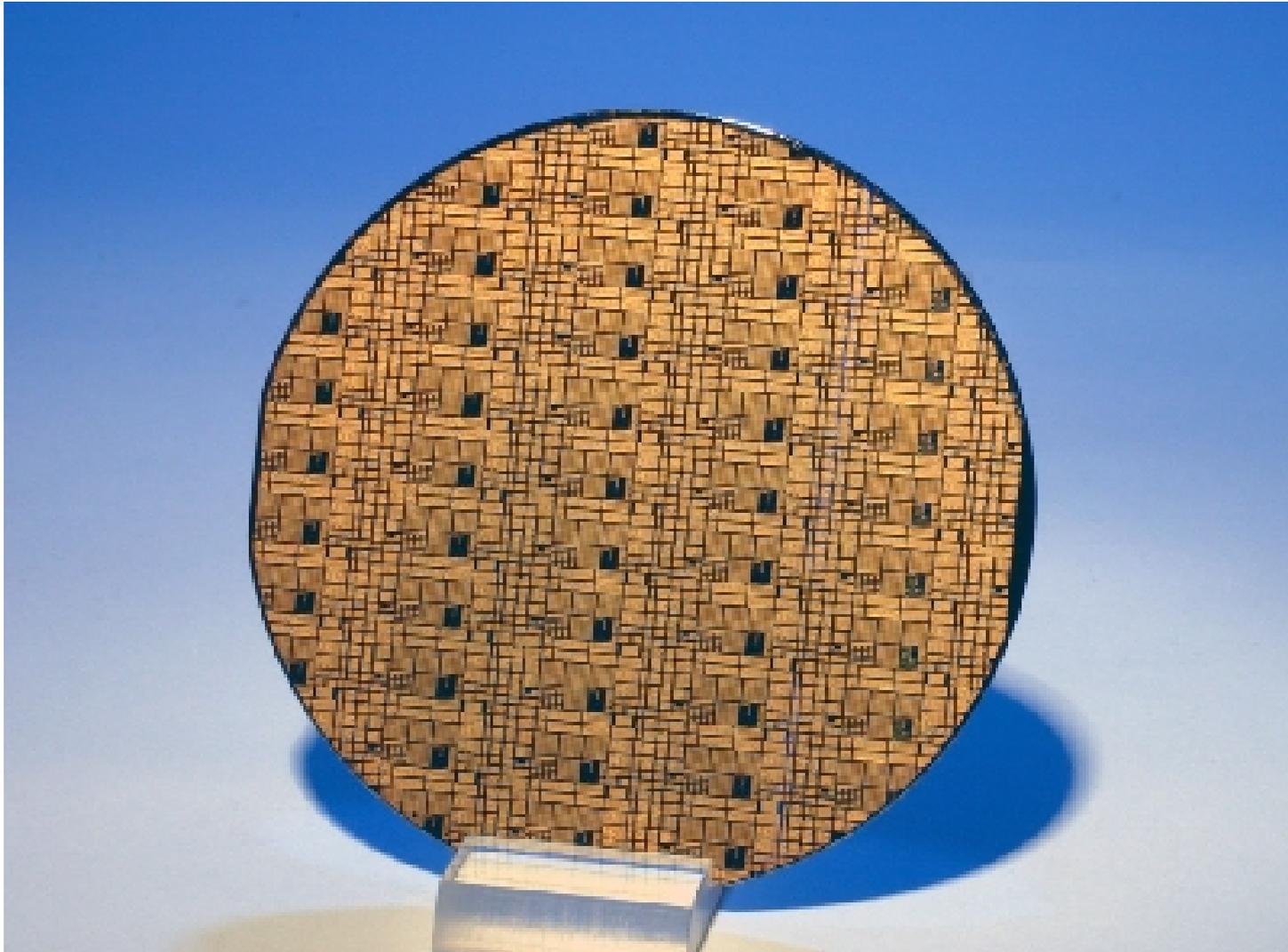
We list below, and with reference to Figure, the sequence of operation involved in the process:

1. Heat wafer to 1200°C.
2. Turn on H₂ to reduce the SiO₂ on the wafer surface.
3. Turn on anhydrous *HCl* to vapor-etch the surface of the wafer. This removes a small amount of silicon and other contaminants.
4. Turn off *HCl*.
5. Drop temperature to 1100°C.
6. Turn on silicon tetrachloride (*SiCl₄*).
7. Introduce dopant.

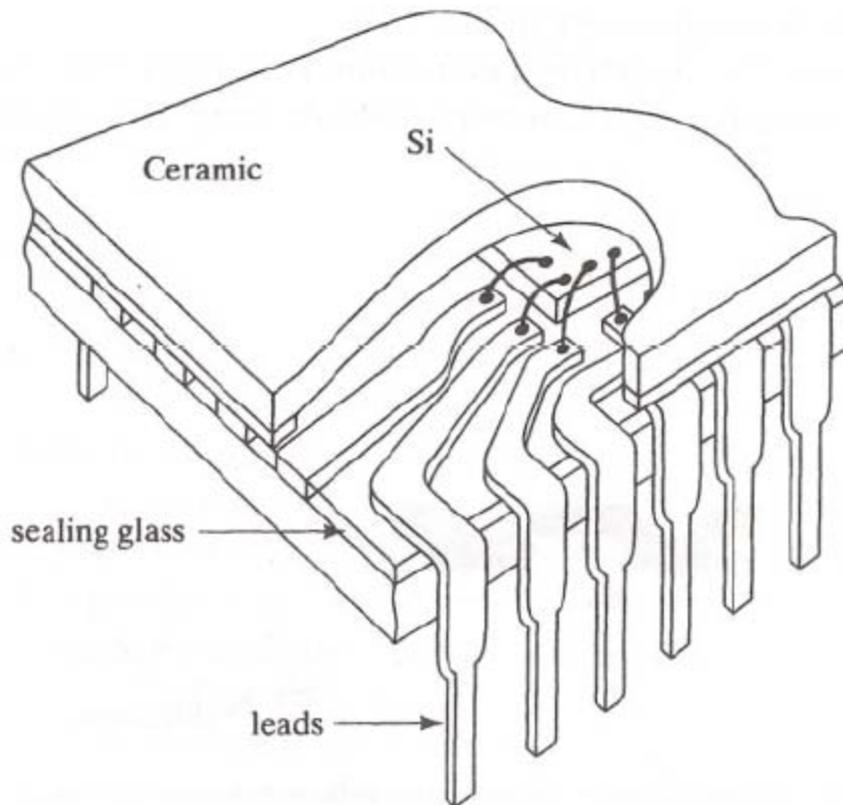
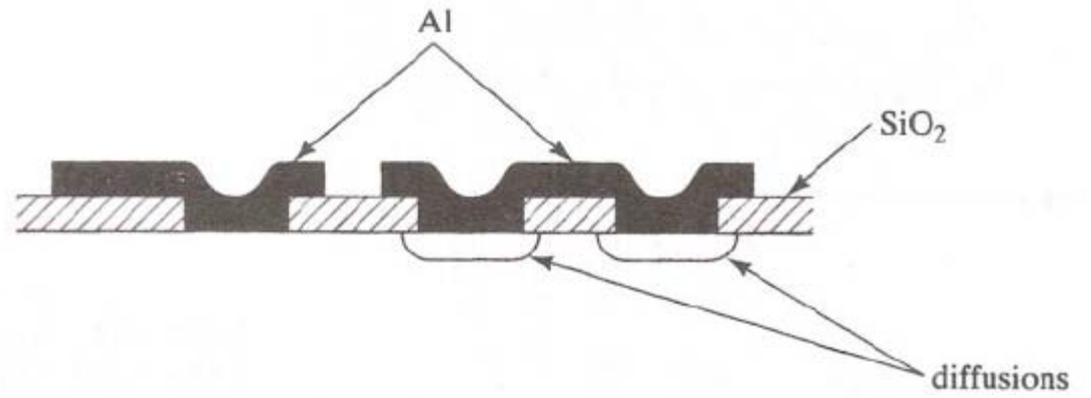




Plasma- based ion implantation and film deposition system



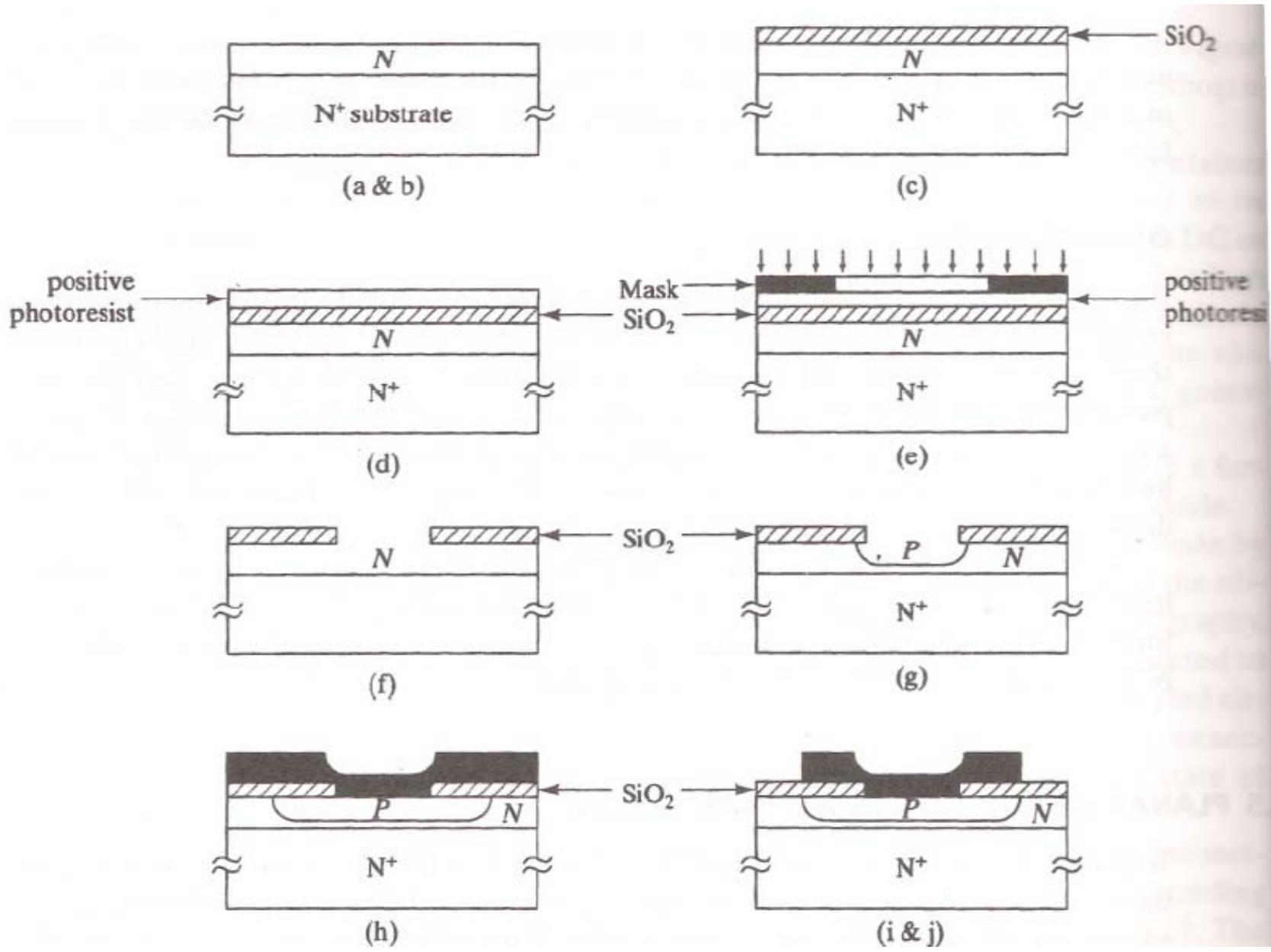
4" Wafer after Metallization

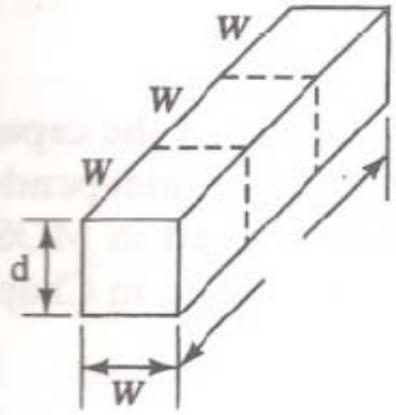
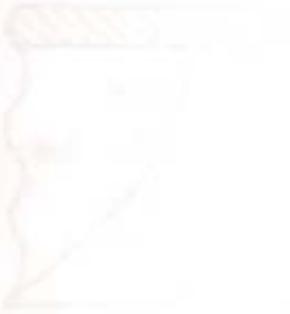


Planar PN Junction Diode Fabrication

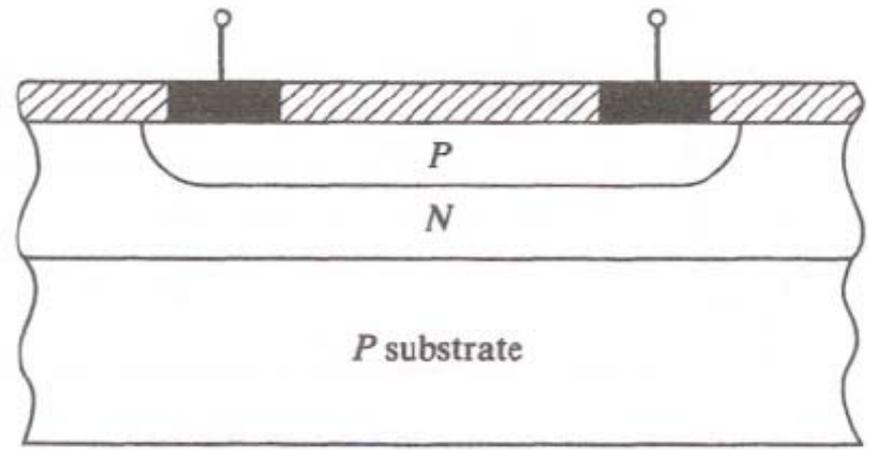
Figure Process Description

1. An N⁺ substrate grown by the Czochralski process is the starting metal of approximately 150 μ m thick.
2. A layer of N-type silicon (1-5 μ m) is grown on the substrate by epitaxy.
3. Silicon dioxide layer deposited by oxidation.
4. Surface is coated with photoresist (positive).
5. Mask is placed on surface of silicon, aligned, and exposed to UV light.
6. Mask is removed, resist is removed, and SiO₂ under the exposed resist is etched.
7. Boron is diffused to form P region. Boron diffuses easily in silicon but not in SiO₂.
8. Thin aluminum film is deposited over surface.
9. Metallized area is covered with resist and another mask is used to identify areas where metal is to be preserved. Wafer is etched to remove unwanted metal. Resist is then dissolved.
10. Contact metal is deposited on the back surface and ohmic contacts are made by heat treatment.

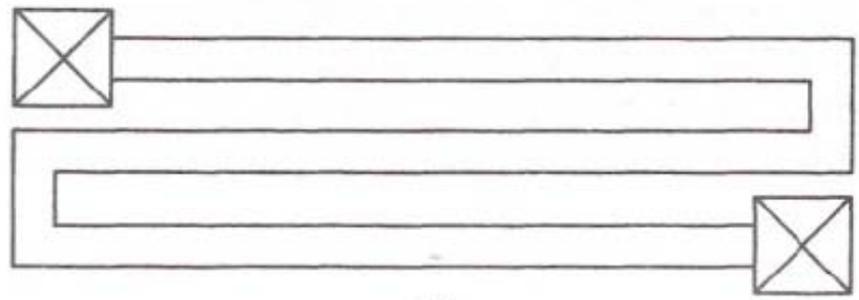




(b)



(a)



(c)

