10 Gb/s Error-Free Operation of All-Silicon Ion-Implanted-Waveguide Photodiodes at 1.55 μm

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***Abstract*— The error-free operation of an all-Si ion-implanted CMOS-compatible waveguide *p-i-n* photodiode (PD) is experimentally demonstrated at 1.55 μm with 2.5 and 10 Gb/s data rates. Detector sensitivity as a function of bias voltage is measured for PDs of two different lengths, 250 μm and 3 mm. The photocurrent increase caused by bringing the PD into a highly absorbing state *via* forward biasing is also measured, and it is shown that a resulting 15 dB improvement in receiver sensitivity can be expected. The limiting factors of the device frequency response are analyzed, and the measured PDs are shown to have comparable dark currents, responsivities, and sensitivities to reported Ge PDs.**

***Index Terms*— Integrated optoelectronics, optical receivers, photodiodes, silicon.**

I. Introduction

INTEGRATED photodiodes (PDs) operating in the C-band are of paramount importance for the realization of on-chip optical links as they enable the terminal optical-to-electronic (OE) data conversion required for Si photonics. These PDs, as realized on the silicon-on-insulator (SOI) platform, must be high-speed and CMOS-compatible to support the high-data-rate conversion of optical signals in highly confined single-mode Si-"wire" waveguides (SiWG) to the electrical data signals that can be processed by monolithically integrated electronics. However, there exists an inherent difficulty in integrating a material that absorbs in the C-band into a CMOS-compatible SOI-based process due to material constraints. Recently, there has been significant progress towards this goal with the hybrid integration of III-V materials [1], and with the integration of Ge [2]–[4]. Although these solutions have produced high-performance devices, Ge integration requires a large number of fabrication steps, a high thermal budget, and the need for a Ge back-end process to produce low dislocation density devices [2], while hybrid III-V integration requires modifications to the standard CMOS process.

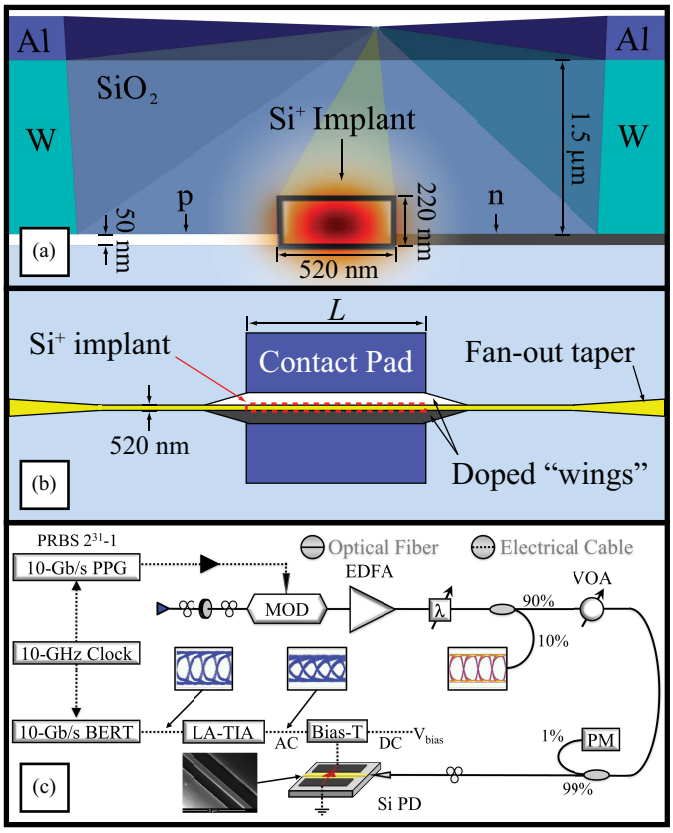

Fig. 1. (a) Cross section of the SiWG PD. The channel waveguide section is Si^+ ion implanted, while the wings are doped *p* and *n* to form a *p-i-n* photodiode. The fundamental quasi-TE mode is overlaid. (b) Top view of the device (not drawn to scale), showing the PD region with $L = 250$ μm or 3 mm, and the cleaved faced fan-out tapers used for input coupling from the lensed tapered fiber (LTF). (c) Experimental setup for measuring detector sensitivity.

Devices that use methods other than intrinsic material absorption for photodetection, referred to as *extrinsic* PDs, have been demonstrated, including: internal photoemission PDs utilizing a SiWG-Schottky contact [5], [6], surface-state absorption in both crystalline [7] and deposited poly-Si PDs [8], and PDs that utilize sub-bandgap-defect-state absorption *via* ion implantation of the SiWG [9]–[21]. Although these extrinsic SiWG PDs are simpler to fabricate, they typically have much lower responsivities (~mA/W) as compared to intrinsic PDs (0.8 to 1 A/W for Ge [2]) as well as lower absorption coefficients which require a substantially longer

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device length. Ion-implanted PDs have shown the best overall performance of these extrinsic SiWG PDs, while only requiring one additional implantation step and no high-temperature processing. Various implantation species have been used to induce absorption, including H^+ [9], He^+ [10], Ar^+ [11], Se^+ [12], and B^+ [21]; however, Si^+ implanted SiWG PDs [13]–[21] have the largest reported responsivities of these ion-implanted PDs. Recently, Si^+ ion-implanted SiWG *p-i-n* PDs have been demonstrated with a bandwidth of > 35 GHz and responsivities of 0.5 to 10 A/W [16]. These devices are fully CMOS-compatible, and have responsivities which are comparable to intrinsic PDs. Due to their weak absorption coefficient of 8–23 dB/cm, Si^+ implanted SiWG PDs have recently found use as in-line power monitors because of their ability to generate photocurrent without attenuating a large fraction of the optical power [19]; resonant cavity enhancement (RCE) has also been employed to decrease the device footprint while maintaining a large external quantum efficiency [17], [20]–[23].

In this letter, error-free operation [bit-error-rate (BER) $\leq 10^{-12}$] is demonstrated for Si^+ ion-implanted SiWG *p-i-n* PDs at 2.5 Gb/s for 250 μm and 3 mm device lengths L and at 10 Gb/s for the 250 μm device length [18]. The sensitivity as a function of bias voltage is measured, and the frequency response limitations of the device are investigated. It is shown that, by decreasing the device capacitance, 40 Gb/s operation is achievable. Additionally, the photocurrent increase caused by bringing the diode into a highly absorbing state *via* forward biasing, as reported in [15]–[17], is measured and it is shown that a 15 dB improvement in receiver sensitivity can be expected. To the best of our knowledge, this is the first systems level exploration of an extrinsic SiWG PD on the SOI platform, as well as the first demonstration of error-free operation of such a device.

II. Measurements and Results

A. Experimental Setup

The measured Si^+ ion-implanted SiWG *p-i-n* PDs were fabricated on the CMOS line at MIT Lincoln Laboratory, as described in [15], with dimensions given in Fig. 1. The experimental setup for measuring the sensitivity of these PDs is shown in Fig. 1(c), with a 10 Gb/s or 2.5 Gb/s $2^{31}-1$ pseudorandom bit sequence (PRBS) of non-return-to-zero (NRZ) data being generated by a pulse-pattern generator (PPG). The PPG is then used to drive a $LiNbO_3$ modulator (MOD), which imprints the electrical signal onto a 1.55 μm optical carrier. The modulated light signal is sent to an erbium-doped fiber amplifier (EDFA) followed by a square passband filter, to reduce the amplified spontaneous emission noise. The optical eye is monitored through a 10/90 tap on a digital communications analyzer (DCA), and a variable optical attenuator (VOA) is used to attenuate the power being launched on-chip for BER measurements. Another tap, with a 1/99 split, sends the signal to an optical power meter (PM) to accurately monitor the power being launched on chip from the lensed-tapered fiber (LTF). The PD is electrically contacted with 40-GHz

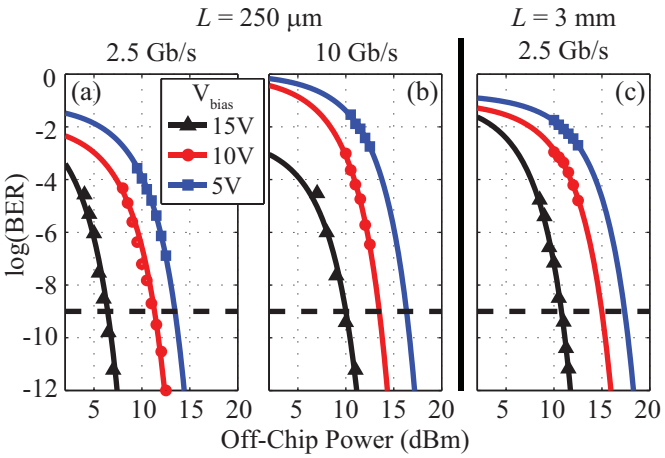

Fig. 2. Receiver sensitivity curves for (a) the $L = 250$ μm device at 2.5 Gb/s, (b) the $L = 250$ μm device at 10 Gb/s, and (c) the $L = 3$ mm device at 2.5 Gb/s. The launch power shown in dBm is the power launched on-chip from the LTF, not including facet loss.

rated probes, and a bias tee is utilized to apply a DC bias. The demodulated electrical data signal is sent to a transimpedance amplifier (TIA), followed by a limiting amplifier (LA), and the signal from the LA is sent to either a bit-error-rate tester (BERT) (for BER measurements, shown in Fig. 2) or a DCA (for eye diagram measurements, shown in Fig. 3).

B. Detector Sensitivity

The receiver sensitivity curves for the $L = 250$ μm device at 5 V, 10 V, and 15 V biases are shown in Fig. 2(a)–(b) for 2.5 Gb/s and 10 Gb/s data reception, respectively. Receiver sensitivity curves for the $L = 3$ mm device at 2.5 Gb/s are shown in Fig. 2(c). The power shown in Fig. 2 is *the power being launched on-chip from the LTF* (measured on the 1/99 tap), and does not take into account facet loss from the fan-out tapers [Fig. 1(b)]. The facet loss is estimated to be 15 dB/facet for our devices based on measurements of the total fiber-to-fiber insertion loss. However, since the facet loss has previously been reported to be as low as 7 dB $\pm$ 2 dB/facet [14], the sensitivity of the device is conservatively estimated to be decreased by 7 to 15 dB from the on-chip launch power. The discrepancy between our measured facet loss and the previously reported value is believed to be due to imperfections in the facet caused by polishing.

Error-free operation is demonstrated at 10 Gb/s for a 15 V bias, and at 2.5 Gb/s at 15 V and 10 V biases. For the $L = 250$ μm device the sensitivity at 2.5 Gb/s is measured to be 7.4 dBm and 12.3 dBm for the 15 V and 10 V biases, respectively. At 10 Gb/s, the sensitivity is 11.1 dBm when biased at 15 V. For the $L = 3$ mm device, the sensitivity at 2.5 Gb/s is measured to be 11.7 dBm at 15 V bias. The data points in Fig. 2 have been fit with the complimentary error function [24] using nonlinear least-squares curve fitting.

The eye diagrams for the detected signal after the TIA-LA are shown in Fig. 3, with the error-free cases shown in a red outline. Error-free operation is achievable at lower bias voltages; however, a number of improvements in the device geometry are required, as discussed in the following sections.

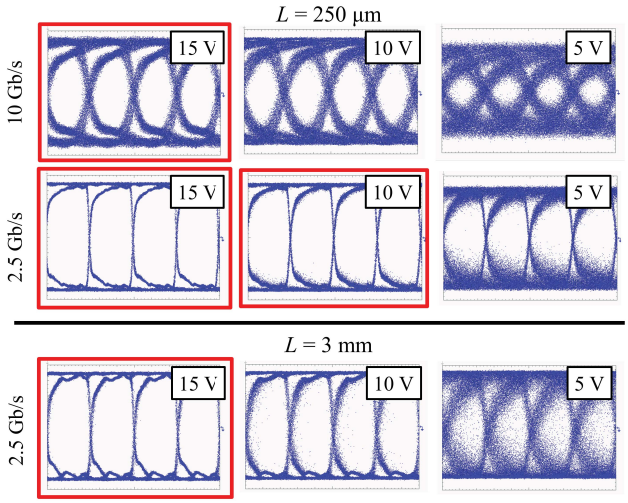

Fig. 3. Eye Diagrams for the $L = 250$ μm and $L = 3$ mm devices for 5 V, 10 V, and 15 V reverse biases, taken after the TIA-LA. Red outlines signify error-free operation.

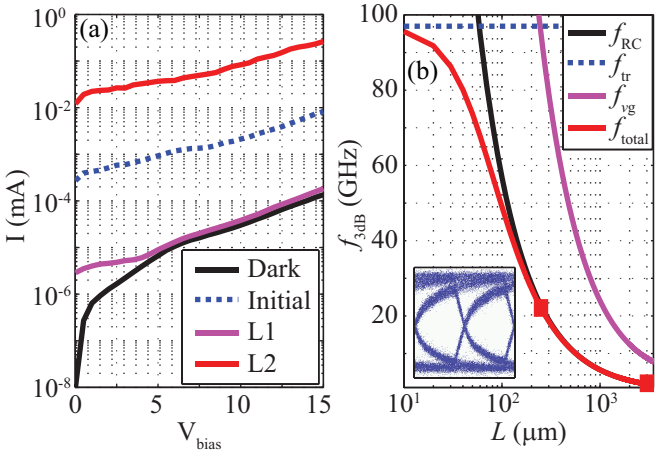

Fig. 4. (a) Measured photocurrent for the $L = 250$ μm device in the initial, L1, and L2 states plotted on a log scale as a function of V_{bias} at $\lambda = 1.55$ μm. (b) Calculated 3-dB frequency of the PD as a function of device length L (on a log scale), decomposed into its constituent components. The two points indicate the time responses of the $L = 250$ μm and $L = 3$ mm devices. Inset: The eye diagram of the $L = 3$ mm device shows that the PD is RC-time-constant limited.

C. L1, L2, and Initial State Photocurrent

The photocurrent generated in the Si^+ implanted PDs is believed to be due to interstitial clusters that form after processing the devices at 475 °C [15], which allow for mid-bandgap transitions of photo-excited carriers. It has previously been shown that these absorbing defects have two stable states, which are labeled L1 and L2 [15]. The PD can be brought into the L1 state, which has a weak absorption coefficient of $\alpha = 8$ dB/cm, by heating at 250 °C for 10 s. Subsequently, the PD can be brought into the L2 state, which has a larger absorption coefficient of $\alpha = 18$–23 dB/cm, by forward biasing the device at 200 mA/cm of device length [16].

The receiver sensitivity measurements presented in the previous section were performed without regard to the absorption state of the PD. Subsequent to these measurements, the photocurrent and dark current versus reverse bias voltage V_{bias} are measured in this unknown "intial" state in Fig. 4(a) for the $L = 250$ μm device. The DC photocurrent is found by launching a 17 dBm CW signal on-chip from a LTF and measuring the generated photocurrent on a picoammeter as a function of V_{bias}. These measurements are repeated for the L1 and L2 state with the results shown in Fig. 4(a). It is noted that the photocurrent in the L1 state is ≈ 5 nA, which is smaller than the dark current for $V_{bias} > 5$ V, and thus the curve follows the dark current very closely. The photocurrent measurements show that a > 15 dB receiver sensitivity improvement at all measured bias voltages can be expected by operating the PDs in the L2 state as compared to the initial state.

The dark current shown in Fig. 4(a) ranges from 6.7 nA at 5 V reverse bias to 136.2 nA at 15 V reverse bias, which is substantially less than the 10's of μAs reported for typical Ge PDs [2], [3]. The dark current in Ge PDs results from dislocation defects in the Ge layer; however, CMOS-compatible Ge PDs fabricated by selective-area deposition have recently been demonstrated with 3 nA of dark current at 1V bias [4]. These devices require a large number of fabrication steps, back-end Ge integration, and a thermal budget of 630 °C, while achieving comparable dark current and responsivity to the simpler-to-fabricate Si^+ ion implanted SiWG PDs.

III. Discussion

Assuming that the PD is being operated in the L2 state, and taking into account the 7 to 15 dB facet loss, the on-chip sensitivity for the SiWG PD is predicted to be between -20 and -12 dBm for BER $= 10^{-9}$ at 10 Gb/s with 15 V bias. Thus, the Si^+ implanted SiWG PD on-chip sensitivity is comparable to the -14 dBm sensitivity of the Ge PD measured in [3] for BER $= 10^{-9}$ at 10 Gb/s with 3.2 V bias. While the device footprint and bias voltage required for the Si^+ implanted SiWG PD are large compared to the Ge PD for a comparable sensitivity, the footprint can be decreased by utilizing RCE [17], [20]–[23] and the required bias voltage can be lowered by redesigning *p-n* doped wings, or by using a metal-semiconductor-metal (MSM) configuration to achieve a larger internal field for the same applied bias.

The calculated 3 dB frequency of the diode as a function of L is shown in Fig. 4(b), where the 3 dB frequency has been decomposed into its constituent components: the transit-time-limited bandwidth f_{tr}, the group-velocity-limited bandwidth f_{vg}, and the RC-time-constant limited bandwidth f_{RC}. The f_{tr} limit is calculated to be ≈ 97 GHz with an assumed carrier saturation velocity of intrinsic Si ($v_{sat} = 1 \times 10^7$ cm/s). This calculation is performed using the LaserMOD software package from RSoft Design Group, Inc. [25], which numerically solves the Boltzmann transport and Poisson equations for a two-dimensional cross-section of the PD [Fig. 1(a)]. The group velocity limited bandwidth is calculated using $v_g = 7 \times 10^9$ cm/s and the method given in refs. [16], [24], while the RC-time-constant-limited bandwidth is found by linearly fitting the measured device capacitance values for the $L = 250$ μm and $L = 3$ mm devices [15] to find a capacitance per unit length of 0.53 fF/μm, and assuming

a 50 Ω load. The total frequency response is approximated by $f_{total} \approx \left(f_{RC}^{-2} + f_{v\mathrm{g}}^{-2} + f_{tr}^{-2}\right)^{-1/2}$.

It can be seen from Fig. 4(b) that the total electrical bandwidth of this device geometry follows the RC-time-constant-limit, deviating only at short devices lengths of $L < 200$ μm. The RC-time-constant limits the PD electrical response to $\approx$21 GHz for the $L = 250$ μm device, and $\approx$2.1 GHz for the $L = 3$ mm device. The eye diagram of the $L = 3$ mm device before the TIA-LA is shown in Fig. 4(*inset*), where it can be seen that the decay time of the signal is longer than the bit slot. For a 2.5 Gb/s signal, the bit slot is 400 ps, while the decay time for a 2.1 GHz RC-limited device corresponds to $\approx$470 ps. Thus, the device-geometry tested is RC-time-constant-limited. At $L = 3$ mm the frequency response limitation causes a sensitivity penalty as compared to the $L = 250$ μm device which outweighs the increase in responsivity gained by increasing L. Device capacitance must be minimized to overcome this sensitivity penalty for the $L = 3$ mm device, and for the $L = 250$ μm device to operate at higher data rates.

Towards this effort, the frequency response of these devices can be increased by optimizing the device geometry to decrease the total device capacitance. If the capacitance of the $L = 3$ mm device is decreased to ≤ 0.362 pF, the frequency response is limited to 8.8 GHz by v_{g}, resulting in receiver sensitivity improvement for 2.5 Gb/s operation. Similarly, the $L = 250$ μm capacitance must be decreased to 70.7 fF for a 50 GHz frequency response, which is sufficient for 40 Gb/s operation. The absolute limit for the frequency response of the $L = 250$ μm device is the transit time limit, which requires $C \leq 35.4$ fF. Devices capacitances of $\sim$1 fF have been reported for Ge PDs [4], while similar capacitances are achievable for Si^+ implanted PDs.

IV. Conclusion

Error-free operation of an all-Si ion-implanted PD operating at 1.55 μm has been demonstrated for 2.5 Gb/s and 10 Gb/s data reception. For the $L = 250$ μm device error-free operation was achieved with 15 V bias at 10 Gb/s and with 15 V and 10 V biases at 2.5 Gb/s, while error-free operation for the $L = 3$ mm device was shown with 15 V bias at 2.5 Gb/s.

Present Ge PDs generally offer better performance; however, they impose the significant burden of a challenging materials system. It has been shown that Si^+ implanted PDs have dark currents, responsivities, and sensitivities comparable to those of reported Ge devices. A significant improvement in frequency response can be achieved by reducing device capacitance and a $>$ 15 dB improvement in receiver sensitivity can be expected by operating the PDs in the L2 state, which will make Si^+ implanted PDs competitive with Ge PDs. The performance of Si^+ implanted PDs, and the ease with which they can be integrated into a standard CMOS process flow, makes them an excellent candidate for usage as receivers and in-line power monitors in the Si photonics platform.

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