Broadband Silicon Photonic Electrooptic Switch for Photonic Interconnection Networks

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***Abstract*—We present a silicon photonic microring resonator electrooptic switch, demonstrate error-free switching of single-channel data rates up to 40 Gb/s, and characterize the device using bit-error-rate and power penalty metrics. We experimentally verify penalty-free switching of single-channel data rates up to 10 Gb/s, and low-penalty switching up to 40 Gb/s, firmly establishing the feasibility of this switch for high-performance photonic networks-on-chip.**

***Index Terms*—Multiprocessor interconnection networks, nanophotonics, optical resonators, optical switches, photonic integrated circuits.**

I. Introduction

THE enduring pursuit of performance gains in computing, combined with stringent power constraints, has fostered the ever-growing computational parallelism associated with chip multiprocessors (CMPs). Sustaining this parallelism growth introduces unique challenges for on- and off-chip communications, shifting the focus toward novel and fundamentally different communication approaches. The chip-scale photonic interconnection network, enabled by high-performance silicon photonic devices, offers a clear path toward bandwidth scalability with reduced power consumption [1]. Leveraging compatibility with complementary metal-oxide-semiconductor (CMOS) fabrication processes and capability of dense integration, the silicon-on-insulator (SOI) platform has already facilitated the high-performance photonic devices required for these networks, including waveguides, filters, modulators, switches, and photodetectors [2]–[9].

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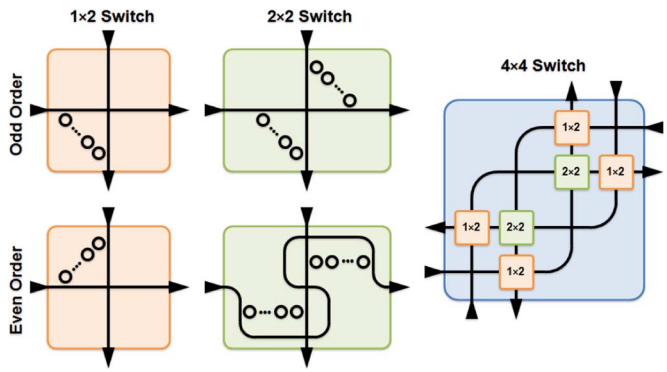

Fig. 1. Elementary models for 1×2 and 2×2 switching building blocks, implemented with both odd- and even-order microring resonators (left), as well as the nonblocking 4×4 switch constructed using these models (right).

Within the photonic interconnection networks, broadband electrooptic switches route high-bandwidth wavelength-parallel optical messages throughout the dynamic circuit-switched paths with ultrafast reconfiguration times [1]. Combining the functional ubiquity of the silicon photonic resonator with the advantages of higher-order configurations [2]–[5], we are able to realize broadband switching devices with massive switching bandwidths and short switching transitions. We first define the critical elementary models for 1×2 [2]–[6], and 2×2 [7], switching building blocks, implemented using arbitrary-order resonators, noting that different configurations are required for odd [5]–[8], and even [2]–[4], number of resonators (Fig. 1). These elementary models combine to form more complex switching subsystems, such as the nonblocking 4×4 switch (Fig. 1), a critical building block in many photonic interconnection networks [8]. In this work, we demonstrate experimentally a silicon photonic microring resonator electrooptic switch dynamically routing single-channel data rates up to 40 Gb/s, showcasing high bandwidth, short switching transitions, high extinction ratios, and low driving voltage. The device is a second-order 1×2 switch, consisting of two coupled microring resonators each coupled to a waveguide (Fig. 2). We validate this switch in a high-performance communication system environment, and characterize bit-error-rate (BER) and power penalty metrics up to 40 Gb/s.

II. Experiments and Passive Results

The microring resonators in the 1×2 switch are designed with both racetrack and ring features (Fig. 2), with $2\pi \times 10$-μm cavity lengths [3]. The waveguides are 450-nm wide and

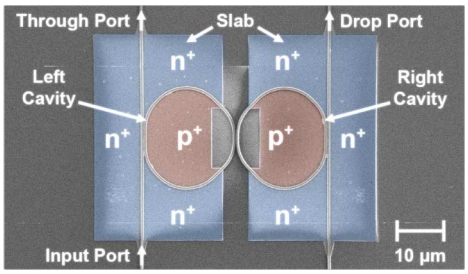

Fig. 2. Top-view scanning-electron-microscope (SEM) image of the silicon photonic microring resonator electrooptic switch.

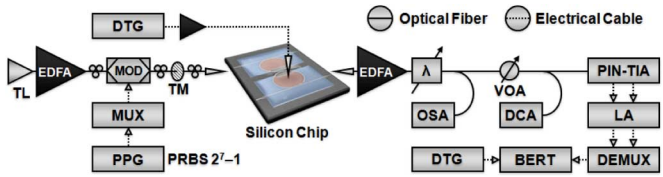

Fig. 3. Diagram of the experimental setup used for spectral and temporal evaluations, as well as BER and power penalty characterizations, using the silicon photonic microring resonator electrooptic second-order 1×2 switch.

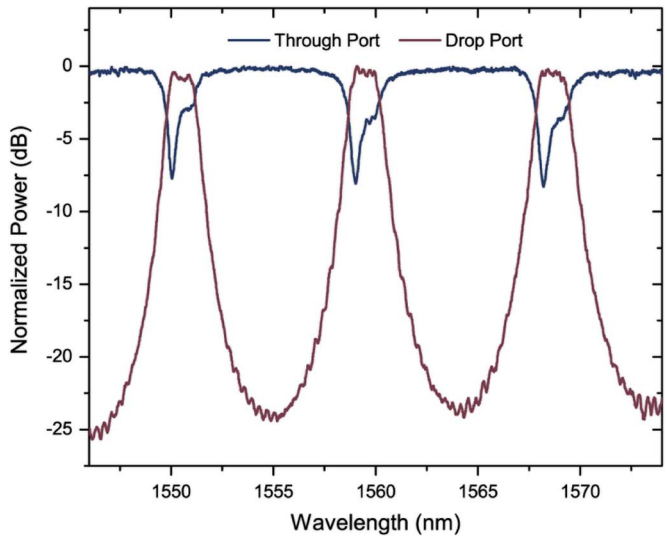

Fig. 4. Spectra of the silicon photonic microring resonator electrooptic switch for both output ports in the passive state.

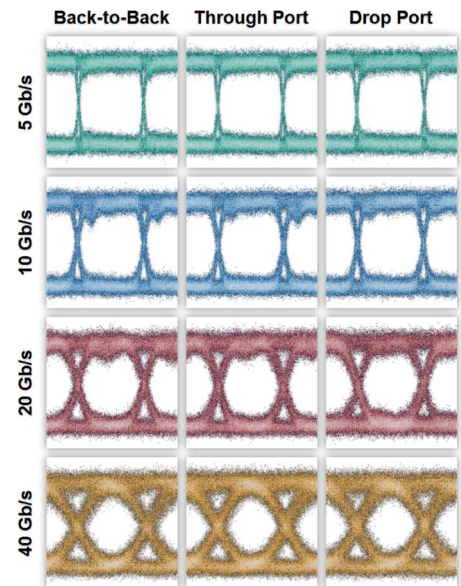

Fig. 5. Output eye diagrams for optical signals with 5-, 10-, 20-, and 40-Gb/s data rates, egressing from both output ports of the silicon photonic microring resonator electrooptic switch, as well bypassing the silicon chip in the back-to-back case.

250-nm tall; there is a 40-nm slab near the microrings that is doped to form the PIN diode structures. Switching an optical signal between the through port and the drop port is accomplished with the detuning of the right cavity resonance using the free-carrier dispersion effect arising from injecting and extracting electrical carriers through the PIN diode. Electrooptic control of these switches enables a more scalable and energy-efficient interconnection network compared to the all-optical switching methods demonstrated in previous work [5]–[7].

The experimental setup (Fig. 3) comprises a tunable laser (TL) source generating continuous-wave light, which is amplified (EDFA) and modulated (MOD) with a nonreturn-to-zero on-off-keyed (NRZ-OOK) signal encoded using a $2^7 - 1$ pseudorandom bit sequence (PRBS), generated by a pulse pattern generator (PPG) and an electrical multiplexer (MUX). The optical signal passes through a fiber polarizer, selecting the quasi-TM propagation mode, and couples into the on-chip nanotapered silicon waveguide using a tapered fiber. The device is switched using a data timing generator (DTG), contacting the silicon chip using high-speed electrical probes. Off chip, the optical signal passes through an EDFA, a filter (λ) with a 0.22-nm 3-dB bandwidth, and a variable optical attenuator (VOA). The signal is detected using a high-speed PIN photodiode and transimpedance amplifier (PIN-TIA) receiver followed by a limiting amplifier (LA). The received data is demultiplexed (DEMUX), and evaluated using a BER tester (BERT). The DTG gates the BERT over the duration of each optical packet. The DTG, PPG, MUX, DEMUX, and BERT are synchronized to the same clock. An optical spectrum analyzer (OSA) and a digital communications analyzer (DCA) are used to evaluate the spectral and temporal performance, respectively. The average optical power injected into the silicon chip is 3 dBm.

Before electrically driving the switch, we record the spectra of this device for both output ports in the passive state (Fig. 4), observing a 9-nm free-spectral range (FSR) and through port passbands with 70-GHz 3-dB bandwidths. The passbands of the two cavities are not perfectly overlapping in this passive state; these passbands are aligned with the applied voltage bias during active switching, and have been shown to achieve depths greater than 20 dB [3]. We then inject a high-speed data signal at the input port of the switch with 5-, 10-, 20-, and 40-Gb/s data rates, and record eye diagrams of the optical signal egressing from the through port (at 1561.5 nm) and drop port (at 1559.5 nm) of the switch (Fig. 5). We compare these eye diagrams with the back-to-back case, in which we bypass the silicon chip and replace it with a VOA set to mimic the fiber-to-fiber insertion loss of the silicon chip (about 17 dB).

III. Active Results and Discussion

For active switching, we first align the optical signal to be on resonance at 1559.5 nm. When the voltage signal is set high (low), the signal is switched to the through port (drop port). We

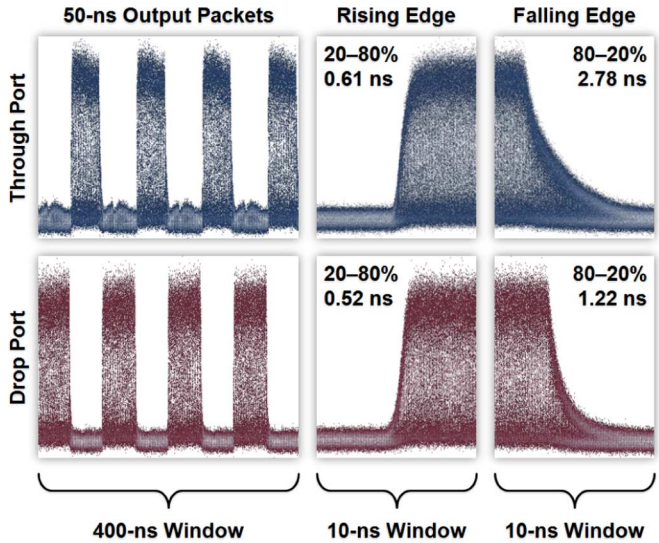

Fig. 6. Output optical packets encoded with 40-Gb/s data for both output ports of the silicon photonic microring resonator electrooptic switch in the active state, with rising and falling edges.

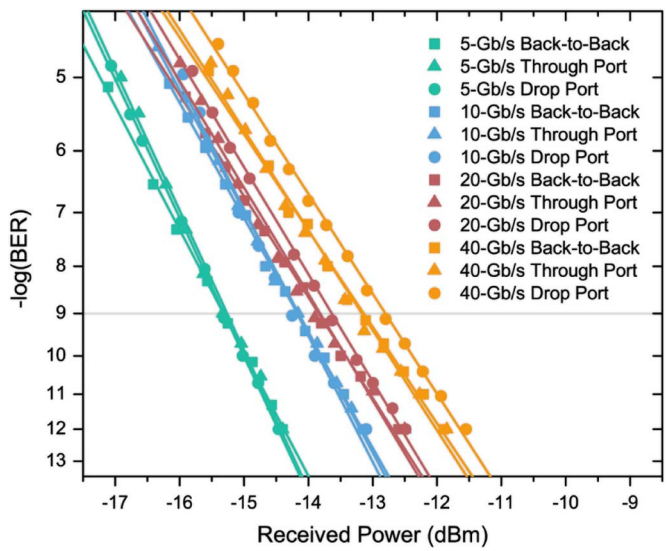

Fig. 7. Experimentally measured BER curves for packetized optical signals with 5-, 10-, 20-, and 40-Gb/s data rates, egressing from both output ports of the silicon photonic microring resonator electrooptic switch, as well bypassing the silicon chip in the back-to-back case.

actively switch the device with a 1.3-V_{PP} square wave with a 0.5-V voltage bias, and a 100-ns period with a 50% duty cycle, producing 50-ns optical data packets alternately egressing from each output port. We switch an optical signal encoded with 40-Gb/s data, and record these optical data packets, including their rising and falling edges, at each output port of the switch (Fig. 6), observing greater than 12-dB extinction ratios at both output ports. The subnanosecond rising edges are achieved using the PIN diode structure. The falling edges are typically limited by carrier lifetimes, and can be further improved using the pre-emphasis method [9].

We switch the optical signal encoded with 5-, 10-, 20-, and 40-Gb/s data, and perform BER measurements on the packetized data for each data rate at each output port of the switch. We observe error-free operation (defined as having BERs less than 10^{-12}), and subsequently record the BER curve, for every configuration including the back-to-back case bypassing the silicon chip (Fig. 7). For the through port, the resulting measured power penalties are negligible up to 40 Gb/s. For the drop port, the power penalties are negligible up to 10 Gb/s, and are 0.2 and 0.35 dB for 20 and 40 Gb/s, respectively. These results are summarized in Fig. 8. The power penalties at the drop port for the higher data rates are likely resulting from spectral filtering of the signal sidebands.

Single-Channel Data Rate (Gb/s)	Through Port Power Penalty (dB)	Drop Port Power Penalty (dB)
5	0	0
10	0	0
20	0	0.2
40	0	0.35

Fig. 8. Summary of power penalty results for both output ports of the silicon photonic microring resonator electrooptic switch.

IV. Conclusion

We have presented and experimentally characterized a high-performance silicon photonic electrooptic switch, capable of routing single-channel data rates up to 40-Gb/s with low power penalty. The ability to support ultrahigh bandwidth, short switching transitions, and high extinction ratios, with low driving voltage, firmly places this device as a key building block for next-generation high-performance chip-scale photonic interconnection networks.

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