Etching Titanium Nitride gate stacked on high-k dielectric

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Research in the field of CMOS devices has shown a constant improvement for the last 40 years. To continue with this progress strained silicon is a prominent candidate to enhance properties of silicon devices furthermore. One promising transistor concept utilizing strained silicon is the DotFET (1) and its upgrade: The disposable DotFET (dDotFET). Both concepts are applying template assisted growth of Silicon-Germanium-Dots and overgrowth with a thin silicon layer (2). This layer is biaxialy strained by the buried SiGe-dot and the transistor channel is integrated on top of the dot making use of this strain. In this work the gate stack for the dDotFET device was developed to fulfill the requirements for transistor processing:

- To prevent interdiffusion of Germanium and Silicon after epitaxy, the whole process for the transistor must not exceed 700°C (3). After the disposal of the SiGe higher temperatures are necessary to activate dopants. Hence, building up the gate-stack has to be done at low temperature but the materials themselves have to resist much higher temperatures.
- The gate-stack has to be finished before the removal of the SiGe-Dot happens. This sequence is essential to prevent the silicon channel from relaxing (4).
- Formation of the gate-stack must not affect the ultra thin silicon capping layer.
- Mesa-Etching has to be possible to get access to the SiGe-Dot after the formation of the gate.
- Gate-width and length should not exceed 150 nm. For larger W_G or L_G the gate covers the SiGe-dot and it becomes more challenging to get access to SiGe for the removal step. To large Channels will also not benefit from increased carrier mobility.

The process presented in this work is compatible to these requirements. Two layers have been deposited to form a gate-stack: 5 nm of Gadolinium-Scandate ($GdScO_3$) is working as the gate dielectric and the gate metal is made of Titanium Nitride (TiN). The TiN is etched in a reactive ion etch chamber with chlorine plasma at 10 Watts RIE-Power and 1000 Watts ICP-Power. The resulting bias-voltage is 6 Volt and therefore the etching is chemically dominated. Due to the low sputtering contribution, the etching stops at the dielectric (Fig. 1). For the columnar structure of TiN, whereas the shells of the columns consist of TiO_x, this procedure prefers to remove the TiN core of the columns and the more robust TiO_x hulls are remaining (Fig. 2). They have to be etched separately by a short dip in Hydrofluoric Acid. To get the $GdScO_3$ off the source- and drain-regions, it has to be chlorinated in RIE. The resulting layer is not volatile in the vacuum-chamber but it can be dissolved in DI-Water (5). For chlorination a 20 s treatment in a RIE-chamber at 150 W RIE-Power without ICP-power is sufficient. Because of the high bias-voltage this step is self-aligned and does not affect the insulator in the MOS-Cap. Self aligned shallow implantation and Mesa-Etching (Fig. 3) will finish the transistor. For the dDotFET a stack of 100 nm TiN on 5 nm $GdScO_3$ is used. The gate is masked by HSQ-resist which is exposed by electron beam lithography. The areas for the mesa etching are masked by ZEP520A7-resist which is also patterned by e-beam. The final transistor has a gate-width of 50 nm and a gate-length of 60 nm (Fig. 4).

Nano-patterning TiN using HSQ-mask and low-bias-voltage chlorine-plasma is a known application (6). The process in this work is designed to be selective to ultra thin high-k dielectrics and capable to remove it right next to the gate. The etched flanks are nearly perpendicular in addition.

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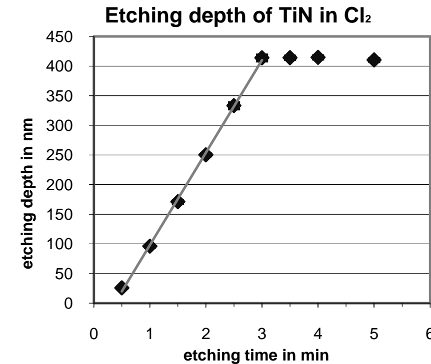

Figure 1: Etching-depths of 410nm TiN on 5nm GSO, etching-rate is 180nm/min

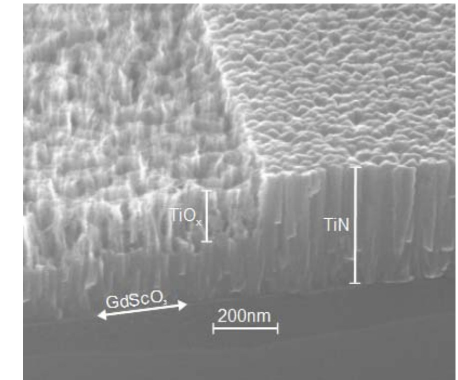

Figure 2: SEM image of crosscut of half etched TiN-thin-film before HF-dip

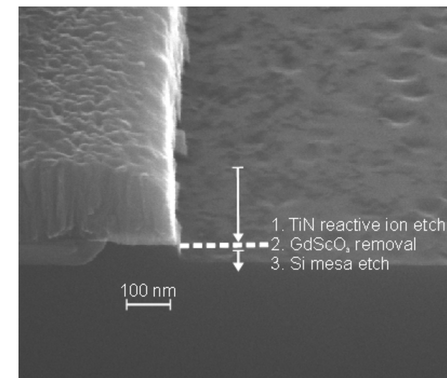

Figure 3: SEM-image of crosscut of sample after self aligned Si mesa etching

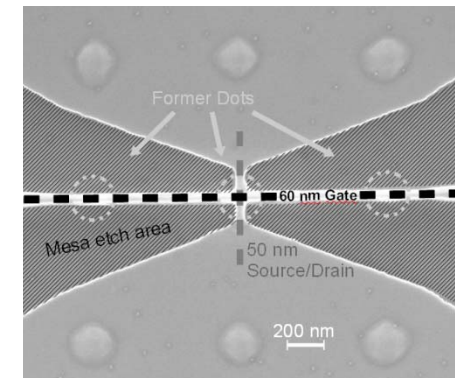

Figure 4: SEM-image of finished dDotFET