10-Gb/s WDM Optically-Connected Memory System using Silicon Microring Modulators

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Abstract *We report on the first silicon photonic modulator-based optically-connected memory system. An FPGA-based processor generates a 4×2.5-Gb/s WDM memory link via an array of silicon microring modulators, achieving error-free (BERs<10^{-12}) performance using several standard line coding schemes.*

Introduction

The growing performance gap between processors and memory in contemporary computing systems necessitates a shift in the way data is moved on and off chip. Electronic interconnects limit computational performance due to their low bandwidth-density and distance- and data-rate-dependent energy dissipation, resulting in processor-memory communication bottlenecks and a phenomenon known as the Memory Wall[1]. It is therefore necessary to redesign the processor-memory interconnect to create a novel memory system that can meet the energy and performance requirements of next-generation computers.

Optically-connected memory (OCM) is a potentially attractive solution to the Memory Wall due to its high bandwidth density and distance independence across computer system scales. These advantages enable the scalability of high-performance memory systems[2]. Capitalising on wavelength-division multiplexing (WDM), a single optical link can provide terabits of memory bandwidth, further mitigating the aforementioned bandwidth limitations. Additionally, compared with traditional electronic interconnects, a longer physical link is achievable using optics, with lower energy consumptions, which allows access to a greater number of OCM devices for increased total memory capacity.

Close integration of photonic and processor/memory hardware is essential to realising the full potential benefits of OCM. Recent advances in silicon photonics have yielded high-performance, compact, energy-efficient, CMOS-compatible nanophotonic devices[3]. Integrating these silicon photonic components with the proposed OCM system (Fig. 1) will eliminate the need for power-hungry off-chip electronic wires, alleviate pin-count constraints, and maximise memory bandwidth with WDM. The resulting alignment of off-chip memory bandwidth with on-chip bandwidth enables processors to access remote memory as if it were local, which is unachievable with electronic interconnects due to pinout limitations.

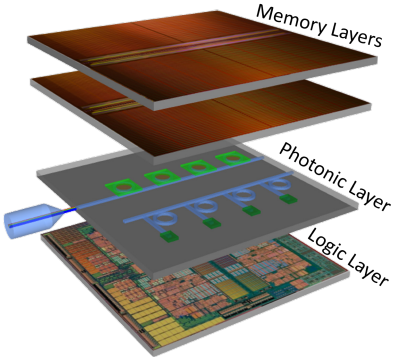

Fig. 1: Illustration of 3D-stacked OCM node. The high-speed logic layer interfaces with the memory layers to drive the photonic components.

In this work, we experimentally demonstrate for the first time an OCM system that leverages integrated silicon photonic microring modulators. The OCM module consists of a circuit board containing Micron DDR2 memory and an Altera Stratix II GX field-programmable gate array (FPGA). The FPGA contains a 4×2.5-Gb/s bidirectional transceiver bank that is used to drive a modulator array of four microrings, which in turn modulates four separate wavelength channels to create an aggregate 10-Gb/s WDM memory link. A second, identical circuit board uses its FPGA to implement a microprocessor that accesses the OCM module across the 10-Gb/s optical memory link. We evaluate the OCM link using several accepted line codes from computing (8b/10b and 64b/66b encoding schemes) to showcase the system's support of diverse memory traffic within future computing systems.

Silicon microring modulators

The microring modulator array (Fig. 2) utilised in this experiment was fabricated at the Cornell Nanofabrication Facility[3]. Each ring radius differs

Fig. 2: SEM image of microring modulator array.

such that the circumferences differ by 20, 40, and 60 nm, which allows the four rings to modulate four independent wavelength channels. Each ring is driven by a 1.2 V_{pp} signal and biased at 0.6-0.8 V. This drive voltage conforms to electronic transceiver standards, such as those supported by the Altera Stratix II GX FPGA[4], thus eliminating the need for high-power amplifier circuitry typically required by the large V_π of $LiNbO_3$ modulators.

Experimental Setup and Results

The experimental setup creates an OCM system by using the microring modulators to replace the electronic bus between a microprocessor and its main memory. The OCM module consists of four Micron DDR2 SDRAM devices electrically connected to the Altera FPGA, which reformats the memory communication into four 2.5-Gb/s data streams to modulate four independent wavelength channels. A second Stratix II GX FPGA implements an emulated microprocessor, along with a custom memory controller[2], which must access the OCM module for all its data. The memory controller optimises communication across the optical memory link and enables customised communication patterns.

In the first stage of the experiment, the microprocessor's 4×2.5-Gb/s transceivers modulate the four-microring modulator array. The return path from the OCM board is performed electrically. In the second stage of the experiment, the OCM node's transceivers drive the microring modulator array while the microprocessor-to-OCM path is performed electrically. On the receive side, for both stages of the experiment, four PIN-TIA photodetectors with limiting amplifiers (LA) are connected to each FPGA to electrically receive the 4×2.5-Gb/s optical data. This process allows us to characterise the overall performance of our OCM system in which both processors and memory benefit from integrated nanophotonics. Fig. 3 shows the experimental setup for one stage with an FPGA-based circuit board, either the processor or memory board, modulating the microring resonator array. Each microring is directly modulated by the FPGA's high-speed transceivers at 1.2 V_{pp} per channel without pre-emphasis. Four independent wavelength channels (1539.85, 1542.6, 1547.28, and 1551.63 nm) are combined with WDM, amplified by an erbium-doped fibre amplifier (EDFA), and launched into the chip with an average power of 10 dB per wavelength. Each microring modulates a separate wavelength channel with 2.5-Gb/s on-off keyed (OOK) data from the FPGA's 4×2.5-Gb/s transceivers. The ring-modulated, WDM memory data exits the chip with an average power of -20 dB before being amplified with an EDFA. The WDM memory data is then demultiplexed to allow each wavelength channel to be electrically received by a separate PIN-TIA-LA for use at the destination processor or memory module.

To characterise the complete OCM system with the microring modulators, our processor and memory nodes execute a program to repeatedly transmit either 8b/10b- or 64b/66b-encoded memory traffic across the optical memory link. While both line codes guarantee a minimum number of state changes per data block, only 8b/10b is designed to maintain DC balance. Therefore, depending on the memory data, any 64b/66b transmission can contain strings of 65 zeroes or 65 ones for a duration of 26 ns at 2.5 Gb/s. The resulting heating of the microring can potentially impact link performance and necessitate dynamic stabilisation techniques[4]; however, these were not demonstrated here. Since 64b/66b encoding requires only 3% communication overhead

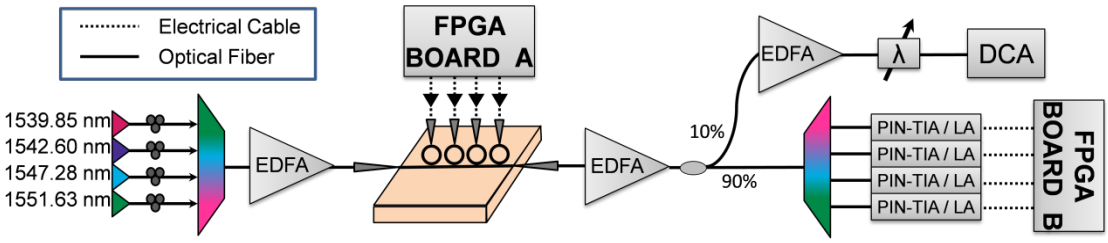

Fig. 3: Experimental setup.

Tab. 1: Comparison of microring-modulated 8b/10b memory data, 64b/66b memory data, and 2^{31}-1 PRBS.

Measurement	Data Type					
	8b/10b memory		64b/66b memory		2^{31}-1 PRBS	
	Best (1551.63 nm)	Worst (1539.85 nm)	Best (1551.63 nm)	Worst (1539.85 nm)	Best (1551.63 nm)	Worst (1539.85 nm)
Extinction ratio	6.52 dB	5.63 dB	5.97 dB	5.78 dB	6.10 dB	6.46 dB
Rise time	106 ps	222 ps	111 ps	311 ps	124 ps	147 ps
Fall time	95 ps	100 ps	102 ps	304 ps	100 ps	104 ps
Jitter (RMS)	20 ps	32 ps	144 ps	169 ps	32 ps	42 ps

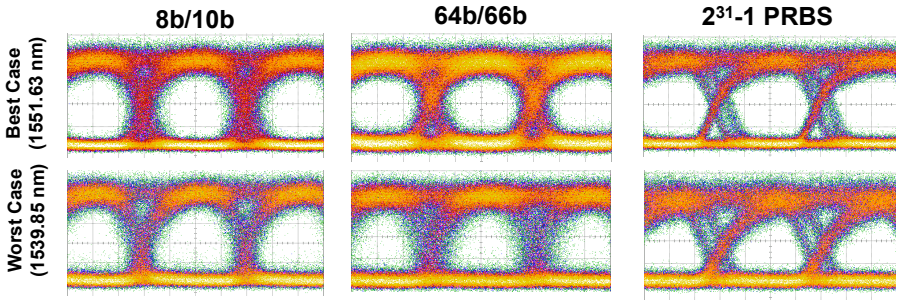

Fig. 4: Optical eye diagrams of the 4×2.5-Gb/s wavelength channels showing microring-modulated modulated 8b/10 and 64b/66b memory communication and 2^{31}-1 PRBS (100 ps/div).

compared with 25% for 8b/10b encoding, 64b/66b is more desirable and a requirement for any high-performance optical interconnect.

The microprocessor is programmed to generate memory traffic by repeatedly writing to the OCM module with predictable data patterns: all zeroes, all ones, or 2^{31}-1 pseudorandom binary sequence (PRBS). These data patterns are chosen from tests used to verify electrically-connected memory systems as well as those for characterising optical systems. This memory data passes through either 8b/10b or 64b/66b encode/decode hardware at each end of the memory link. Next, after filling the OCM with data, the microprocessor initiates a series of 'read from memory' operations to stream all previously stored data back from the OCM while verifying the data for bit errors. This process repeats for both line codes until one terabit of data has been verified to demonstrate an effective memory-bit-error rate (EMBER) less than 10^{-12}.

Fig. 4 shows the 2.5-Gb/s optical eye diagrams for the 8b/10b and 64b/66b optical memory traffic, as well as for the 2^{31}-1 PRBS pattern for comparison. To generate the PRBS eyes, a pulse-pattern generator (PPG) replaces the FPGA for modulating the four microrings. Table 1 contains the measured eye parameters using a digital communications analyser (DCA) to compare the 8b/10b- and 64b/66b-encoded memory data and the PPG-generated 2^{31}-1 PRBS. The 8b/10b memory data, with its comparatively short consecutive runs of 0's or 1's, results in the overall best performance. The 64b/66b memory data suffers the worst performance, with significantly worse rise/fall times and jitter, due to longer runs of 0's or 1's and resulting microring thermal instability. The performance differences across wavelengths using the 8b/10b or 64b/66b data are attributed to each channel being modulated with different bit patterns (each 2.5-Gb/s data stream is modulating a wavelength as a portion of the total 10-Gb/s memory link). In contrast, each PRBS wavelength contains identical data (2^{31}-1 PRBS) and the measured performance is nearly identical for each wavelength.

Conclusions

We experimentally demonstrate the integration of silicon photonic microring modulators with off-the-shelf FPGAs and SDRAM modules to create an energy-efficient 4×2.5-Gb/s WDM optically-connected memory system. The microring-modulated optical memory link is shown to achieve error-free operation (EMBERs < 10^{-12}) for all communication patterns; however, slight signal degradation was observed for 64b/66b-encoded data. This work illustrates the energy and performance benefits of close integration of silicon photonics with next-generation memory systems, the flexibility of silicon microrings to operate under the unpredictable communication patterns of large-scale memory systems, and the potential need for thermal stabilisation within future silicon photonic transceivers.

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