10 Gb/s Error-Free Operation of an All-Silicon C-band Waveguide Photodiode

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Abstract: We experimentally demonstrate error-free operation of an all Si ion implanted CMOS compatible PIN photodiode at 1.55 μm with 2.5-Gb/s and 10-Gb/s data rates. Detector sensitivity as a function of bias voltage is measured.

OCIS codes: (040.6040) Silicon; (040.5160) Photodetectors; (250.3140) Integrated optoelectronic circuits

1. Introduction

Silicon photonics, as realized on the silicon-on-insulator (SOI) platform, shows the potential to manifest optical communications within on-chip applications, alleviating the bandwidth bottleneck faced by contemporary microelectronics. Integrated C-band photodetectors (PDs) are of paramount importance in realizing these types of optical links, as they enable the end optical-to-electronic data conversion. These detectors must be high-speed, and CMOS-compatible to support the high data rate conversion of optical signals in highly confined Si "wire" waveguides (SiWG) to the electrical data signals that can be processed by monolithically integrated electronics. However, there exists an inherent difficulty in integrating a material that absorbs in the C-band into a CMOS-compatible SOI based process. Recently, there has been significant progress towards this goal with hybrid integration of III-V materials [1], and also with the integration of Ge [2-4]; albeit, both of these techniques have significant challenges. Hybrid integration is performed as a serial backend process, and does not provide integration into the CMOS line. Similarly, large area growth of crystalline Ge is not possible on a Si substrate due to the intrinsic 4% lattice mismatch between Ge and Si [2]. Various techniques to mitigate this problem have been employed, including small area growth with a SiGe buffer layer and high temperature annealing [2], low temperature growth of a sacrificial high defect Ge layer, followed by a high temperature growth of crystalline Ge [3], and wafer bonding of Ge onto SOI [4]. Although these solutions have produced high performance devices, they require difficult fabrication procedures, and a high thermal budget along with modifications to the standard CMOS process.

Alternatively, absorption can be induced in the SiWG itself by creating sub-bandgap defect states *via* ion implantation. Si^+ ion implanted SiWG PIN photodiodes have been demonstrated with a bandwidth of > 35GHz and responsivities of 0.8 A/W [5]. These devices are fully CMOS compatible, and do not require any additional high temperature processing. Here we demonstrate error-free data transmission [bit-error-rate (BER) $\leq 10^{-12}$] of a 250-μm long Si^+ ion implanted SiWG PIN PD at 2.5 Gb/s and 10 Gb/s. The sensitivity as a function of bias voltage is also measured.

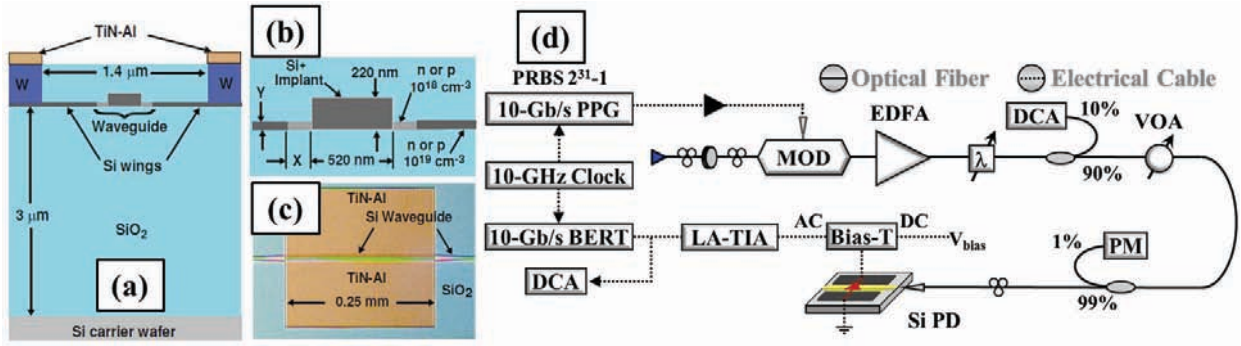

Fig. 1. (a) Cross-Section of a Si^+ ion implanted Si PIN PD, (b) close up of (a) with WG measurements and doping profiles, (c) top-view optical microscope image, (d) experimental setup. (a)-(c) reprinted from [5].

2. Experiments and Results

The Si^+ ion implanted SiWG PIN PDs were fabricated on the CMOS line at MIT Lincoln Laboratory, as described in [5-7], with dimensions given in Fig. 1(a) and Fig. 1(b). Figure 1(c) shows a top view of the tested photodiode

taken with an optical microscope. As shown in Fig. 1(d), 10-Gb/s non-return-to-zero (NRZ) data is generated by a pulse pattern generator (PPG), and used to drive a $LiNbO_3$ modulator, which imprints the electrical signal onto a 1.55-μm optical carrier. The modulated light signal is then sent to an erbium-doped fiber amplifier (EDFA) followed by a square passband filter, to reduce the amplified spontaneous emission (ASE) noise. The optical eye is monitored through a 10/90 tap on a digital communications analyzer (DCA), and a variable optical attenuator (VOA) is used to attenuate the power being launched on-chip for BER measurements. Another tap, with a 1/99 split, sends the signal to an optical power meter (PM) to accurately monitor the power being launched on-chip. The PD is contacted with 40-GHz rated electrical probes, and a bias tee is utilized to apply a DC bias. The demodulated electrical data signal is sent to a transimpedance amplifier (TIA), followed by a limiting amplifier (LA), and the signal from the LA is sent to either a bit-error-rate tester (BERT) [for BER measurements, shown in Fig. 2(a) and 2(b)] or a DCA [for eye diagram measurements, shown in Fig. 2(c)]. The BER curves for 2.5-Gb/s data reception are shown in Fig. 2(a) for 5V, 10V, and 15V biases, while the BER curves for 10-Gb/s data reception are shown in Fig. 2(b) for the same bias voltages. The received power is calculated as $P_{rec} = P_{launch}$-P_{loss}, where P_{launch} is the power being launched on chip as measured by the PM, and P_{loss} is the fan-out taper facet loss of approximately -15dB. The facet loss is estimated by measuring the total insertion loss of a straight waveguide and compensating for the propagation loss of 3 dB/cm. We demonstrate error-free operation at 10 Gb/s for a 15V bias, and at 2.5 Gb/s at 15V and 10V biases. At 2.5 Gb/s, we measure the PD sensitivity to be -8 dBm and -2.5 dBm for the 15V and 10V bias, respectively, and at 10 Gb/s, the sensitivity is -4 dBm when biased at 15V.

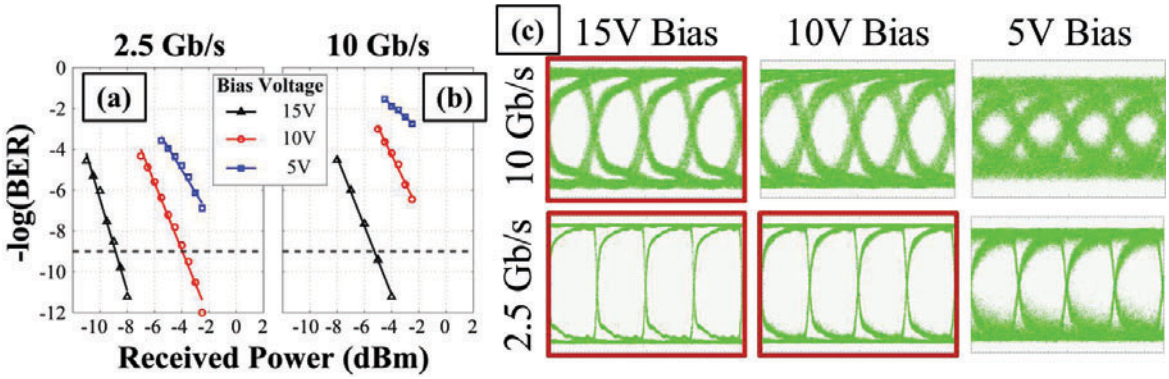

Fig. 2. BER curves for (a) 2.5 Gb/s and (b) 10 Gb/s, (c) electrical eye diagrams taken after the TIA-LA for 2.5 Gb/s and 10 Gb/s data at 15V, 10V and 5V detector bias. Error-free eyes are shown with red outline.

The eye diagrams for the detected signal after the TIA-LA are shown in Fig 2(c), with the error-free cases shown in a red outline. Error-free operation is achievable at lower bias voltages; however a redesigned coupler is required to decrease the necessary launch power.

3. Conclusion

Error-free operation of an all-Si ion implanted PD operating at 1.55 μm has been demonstrated for 2.5-Gb/s and 10-Gb/s data reception. For the 250-μm long oxide clad devices error-free operation was achieved for 15V bias at 10 Gb/s and for 15V and 10V bias at 2.5 Gb/s. It should be noted that the bias voltage required for error-free operation could potentially be reduced by optimizing the contacts to have a smaller spacing. Furthermore, error-free operation at lower bias voltages is possible with either increased launch powers, or by employing improved coupler designs.

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