Broadband CMOS-Compatible Silicon Photonic Electro-Optic Switch for Photonic Networks-on-Chip

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Abstract: Error-free switching of up to 40-Gb/s data using a silicon photonic microring resonator electro-optic switch is demonstrated for the first time, with bit-error-rate and power penalty characterizations firmly establishing its feasibility for high-performance photonic networks-on-chip.

OCIS codes: (200.4650) Optical interconnects; (250.6715) Switching

1. Introduction

Imminent performance scalability challenges associated with high-performance chip multiprocessors (CMPs) are shifting focus toward novel and fundamentally different approaches to on- and off-chip communications. Chip-scale silicon photonic devices enabling photonic networks-on-chip (NoCs) offer an attractive solution for bandwidth scalability with reduced power consumption for these interconnection networks [1]. Leveraging compatibility with CMOS and capability of dense integration, as well as the functional ubiquity of the silicon photonic microring resonator, the silicon-on-insulator (SOI) platform has enabled devices such as waveguides, filters, modulators, switches, and photodetectors [2–6]. The broadband electro-optic switch routes high-bandwidth wavelength-parallel optical messages through the interconnection network, enabling high-performance circuit-switched photonic NoCs with ultrafast dynamic path reconfiguration [1]. Electro-optic control of these broadband switches enables a more scalable and energy efficient interconnection network compared to the all-optical switching methods demonstrated in previous work [2,3]. In this work, we demonstrate experimentally for the first time a silicon photonic microring resonator electro-optic switch dynamically routing up to 40-Gb/s data rates, showcasing high bandwidth, short switching transitions, high extinction ratios, and low driving voltage. We validate this switch in a high-performance communication system environment, and characterize bit-error-rate (BER) and power penalty metrics up to 40 Gb/s.

The device discussed here is a 1×2 switch consisting of two coupled microring resonators each coupled to a waveguide (Fig. 1). The microring resonators are designed with both racetrack and ring features, with 2π×10-μm cavity lengths [4]. The waveguides are 450-nm wide and 250-nm tall; there is a 40-nm slab near the microrings that is doped to form the PIN diode structures. Switching an optical signal between the through port and the drop port is accomplished with the detuning of the right cavity resonance using the free carrier dispersion effect arising from injecting and extracting electrical carriers through the PIN diode. This switch exhibits a hitless behavior, able to switch optical data at one wavelength channel without interfering with neighboring wavelength channels [4].

2. Experiments and results

The experimental setup (Fig. 1) comprises a tunable laser (TL) source generating CW light, which is amplified (EDFA) and modulated (MOD) with a non-return-to-zero on-off-keyed (NRZ-OOK) signal, encoded using a 2^7–1 pseudo-random bit sequence (PRBS) generated by a pulse pattern generator (PPG) and electrical multiplexer (MUX). The optical signal passes through a fiber polarizer, selecting the quasi-TM propagation mode, and couples into the on-chip nanotapered silicon waveguide using a tapered fiber. The device is switched using a data timing generator (DTG), contacting the silicon chip using high-speed electrical probes. Off chip, the optical signal passes through an EDFA, filter (λ), and variable optical attenuator (VOA). The signal is detected using a high-speed PIN photodiode and transimpedance amplifier (PIN-TIA) receiver and a limiting amplifier (LA). The received data is demultiplexed (DEMUX), and evaluated using a BER tester (BERT). The DTG gates the BERT over the duration of each optical packet. The DTG, PPG, MUX, DEMUX, and BERT are synchronized to the same clock source. An optical spectrum analyzer (OSA) and a digital communications analyzer (DCA) are used to evaluate the spectral and temporal performance, respectively. The average optical power injected into the silicon chip is 3 dBm.

Before electrically driving the switch, we first record the spectrum of this device for both output ports in the passive state (Fig. 2a), observing a 9-nm free-spectral range (FSR) and through port passbands with 70-GHz 3-dB bandwidths. The passbands of the two cavities are not perfectly overlapping in this passive state; these passbands are

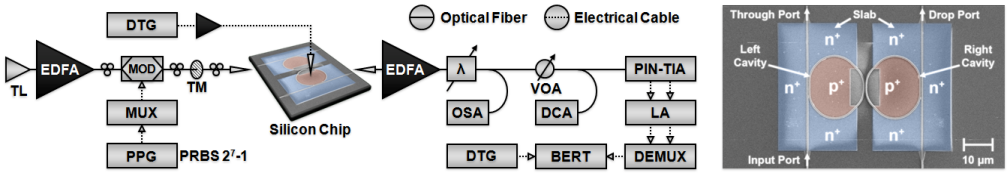

Fig. 1. Diagram of the experimental setup used for BER measurements using the silicon photonic microring resonator electro-optic switch, and top-view scanning-electron-microscope (SEM) image of the device.

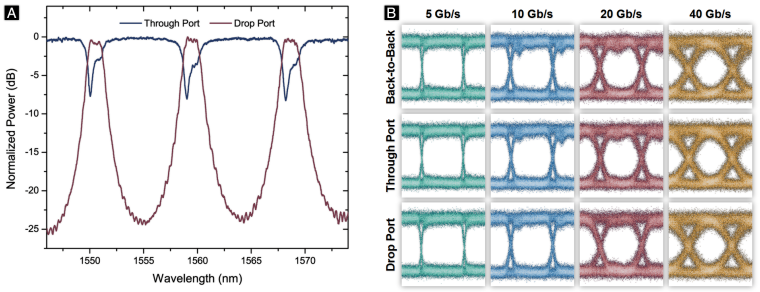

Fig. 2. (a) Spectrum of the silicon photonic microring resonator electro-optic switch for both output ports in the passive state, and (b) output eye diagrams for optical signals with 5-, 10-, 20-, and 40-Gb/s data rates, egressing from both output ports of the switch, as well bypassing the silicon chip in the back-to-back case.

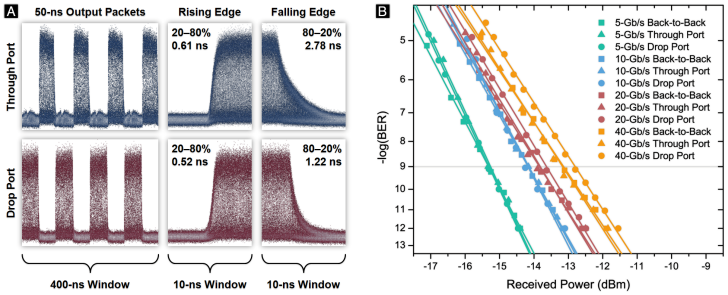

Fig. 3. (a) Output optical packets encoded with 40-Gb/s data for both output ports in the active state, with rising and falling edges, and (b) measured BER curves for packetized optical signals with 5-, 10-, 20-, and 40-Gb/s data rates, egressing from both output ports of the switch, as well bypassing the silicon chip in the back-to-back case.

aligned with the applied voltage bias during active switching, and have been shown to achieve depths greater than 20 dB [4]. We then inject a high-speed data signal at the input port of the switch with 5-, 10-, 20-, and 40-Gb/s data rates, and record eye diagrams of the optical signal egressing from the through port (at 1561.5 nm) and drop port (at 1559.5 nm) of the switch (Fig. 2b). We compare these eye diagrams with the back-to-back case, where we bypass the chip and replace it with a VOA set to mimic the fiber-to-fiber insertion loss of the silicon chip (about 17 dB).

For active switching, we first align the optical signal to be on resonance at 1559.5 nm. When the voltage signal is set high (low), the signal is switched to the through port (drop port). We actively switch the device with a 1.3-V_{PP} square wave with a 0.5-V voltage bias, and a 100-ns period with a 50% duty cycle, producing 50-ns optical data packets alternately egressing from each output port. We switch an optical signal encoded with 40-Gb/s data, and record these optical data packets, including their rising and falling edges, at each output port of the switch (Fig. 3a), observing greater than 12-dB extinction ratios at both output ports. The sub-nanosecond rising edges are achieved with direct free carrier injection using the PIN diode structure. The falling edges are typically limited by carrier lifetimes, and can be further improved using the pre-emphasis method [6].

We switch the optical signal encoded with 5-, 10-, 20-, and 40-Gb/s data, and perform BER measurements on the packetized data for each data rate at each output port of the switch. We observe error-free operation (defined as having BERs less than 10^{-12}), and subsequently record the BER curve, for every configuration including the back-to-back case bypassing the silicon chip (Fig. 3b). For the through port, the resulting measured power penalties are negligible for every measured data rate up to 40 Gb/s. For the drop port, the power penalties are negligible up to 10 Gb/s, and are 0.2 and 0.35 dB for 20 and 40 Gb/s, respectively. The observed power penalties at the drop port for the higher data rates are likely resulting from spectral filtering of the signal sidebands.

3. Conclusions

The success of large-scale on-chip systems, such as photonic NoCs, is determined by the performance of its individual devices. Here, we demonstrate and characterize a novel electro-optic switching building block exhibiting unprecedented performance, establishing its feasibility for next-generation high-performance photonic NoCs.

4. References

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