IEEE SSCS Taipei Chapter Short Courses



1 of 1 12/23/2005 10:26 PM





1 of 1 12/23/2005 10:26 PM

0.5V Analog Integrated Circuits for Nanoscale CMOS Technologies



Peter Kinget, Associate Professor Columbia University, New York, NY, USA

Date: Dec. 14, 2005 (Wed) 3:00~4:00 PM

Place: 電機二館105教室

Abstract

Semiconductor technology scaling a.k.a. 'Moore's Law' has enabled function density increases and cost reductions by orders of magnitudes, but for shrinking device sizes the operating voltages have to be reduced. As we move into the nanoscale semiconductor technologies, power supply voltages well below 1 V are projected. The design of MOS analog circuits operating from a power supply voltage of 0.5 V is discussed in this talk. The scaling of traditional circuit topologies is not possible anymore and new circuit topologies and biasing strategies have to developed. Several design examples are presented. The circuit implementations of gate and body-input 0.5~V operational transconductance amplifiers and their robust biasing are discussed. These building blocks are combined for the realization of active varactor-tuned RC filters operating from 0.5 V using standard devices with a |VT| of 0.5 V in a standard 0.18 um CMOS technology.

Peter R. Kinget received the engineering degree in electrical and mechanical engineering and the Ph.D. in electrical engineering from the Katholieke Universiteit Leuven, Belgium, in 1990 and 1996, respectively.

From 1991 to 1995, he received a fellowship from the Belgian National Fund for Scientific Research (NFWO) to work as a Research Assistant at the ESAT-MICAS Laboratory of the Katholieke Universiteit Leuven. From 1996 to 1999 he was at Bell Laboratories, Lucent Technologies, in Murray Hill, NJ, as a Member of Technical Staff in the Design Principles Department. From 1999 to 2002 he held various technical and management positions in IC design and development at Broadcom, CeLight and MultiLink. In the summer of 2002 he joined the faculty of the Department of Electrical Engineering, Columbia University, NY.

He is a Senior Member of the IEEE and Associate Editor of the IEEE Journal of Solid State Circuits (2003-). He serves as a member of the Technical Program Committee of the IEEE Custom Integrated Circuits Conference (CICC) (2000-); Symposium on VLSI Circuits (2003-); International Solid-State Circuits Conference (2005-).

主辦單位: IEEE SSCS Taipei Chapter 協辦單位: 國立台灣大學電子工程學研究所 國立台灣大學系統晶片中心

1 of 1