Designing Analog and RF Circuits for Ultra-low Supply Voltages

Peter Kinget

COLUMBIA UNIVERSITY IN THE CITY OF NEW YORK
Nano CMOS : Supply Voltage

[ITRS'05]

–O– High Perf.
–Δ– Low Standby
–V– Low Power

Thick oxide $V_{DD}$
Thin oxide $V_{DD}$
Thin oxide $V_T$

Technology node [nm]

Supply Voltage
Ultra-low Voltage Analog/RF

• What analog/RF is possible in core nanoscale digital?
• Scavenging applications
  – E.g., single solar cell $V_{DD} \ 0.4-0.5V$
• Ultra-low energy digital systems
  – Optimal $DV_{DD}$ is 0.3-0.5V
  – Analog support functions for digital
• SOC designs
  – Analog/RF powered from on-chip LDO
  – $AV_{DD}$ is 0.2V below $DV_{DD}$
• Interesting research...
  – Explore boundaries, develop design techniques
MOST Biasing: CS or VCCS

- Transconductor or Current Source
  \( V_{DS} > 0.15 \text{ V} \) (for \( V_{GS} - V_T \leq 0.2 \text{ V} \))

- Moderate to Strong Inversion
  \((V_{GS} - V_T) \approx 0.15 \text{ V} \) & \( V_T = 0.15 \text{ V} \) \( \Rightarrow \) \( V_{GS} = 0.3 \text{ V} \)
Ultra-LV Challenges in OTAs
Device Level

- RSCE

- Forward Body-Bias

\[ V_{BS} = 0.5V \quad \Delta V_T \sim -50mV \]
0.5 V Gate-input OTA stage

\[ \text{V}_{\text{out-}} \quad \text{V}_{\text{out+}} \]

\[ \text{V}_{\text{bn}} \quad \text{V}_{\text{NR}} \]

\[ \text{V}_{\text{in+}} \quad \text{V}_{\text{in-}} \]
0.5 V OTA in 0.18um CMOS
On-chip biasing circuits

Level shift biasing circuit

$V_{bn}$ generating circuit

(Simplified OTA)
Error amplifier for biasing

- 20 kHz GBW for 1 pF load
- 2 µA current
- Controlled body voltage sets the amplifier threshold
OTA DC transfer characteristics and $V_{NR}$ generation

$V_{NR}$ generating circuit

Replica of OTA stage 1

<table>
<thead>
<tr>
<th>Input differential voltage [mV]</th>
<th>Output diff voltage [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>-2</td>
<td>0</td>
</tr>
<tr>
<td>-1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0.5</td>
</tr>
<tr>
<td>2</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Increasing $V_{NR}$
Open loop performance (meas.)

Gain [dB]

Frequency [Hz]

C_L = 10 pF (diff.)
R_L = 50 kΩ
I_{DD} = 150 µA

62 dB
350 mV; automatic bias

42 dB

Increasing gain—boosting bias

GBW: 10 MHz
Low-voltage tunable integrator

\[ V_{DD} \]

\[ \frac{2}{3} \cdot R_1 \parallel R_2 \]

\[ V_{in} \]

\[ V_{DD} \]

\[ \frac{2}{3} \cdot R_1 \parallel R_2 \]

\[ 0.25 \, V \]

\[ 0.4 \, V \]

\[ C \]

\[ 0.25 \, V \]

\[ V_{out} \]

\[ C_{fixed} \]

\[ C_{var} \]

\[ V_{tune} \]
0.5 V Fully integrated 5th order LPF

- Operation at 0.45 V to 0.6 V
- 1.1 mW power dissipation
- 57 dB dynamic range

[Chatterjee, ISSCC05, JSSC05]
Performance summary at 27C

<table>
<thead>
<tr>
<th>Parameter</th>
<th>0.45</th>
<th>0.50</th>
<th>0.55</th>
<th>0.60</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$ [V]</td>
<td>0.45</td>
<td>0.50</td>
<td>0.55</td>
<td>0.60</td>
</tr>
<tr>
<td>-3 dB cut-off frequency [kHz]</td>
<td>135.0</td>
<td>135.0</td>
<td>135.0</td>
<td>135.0</td>
</tr>
<tr>
<td>Total current [mA]</td>
<td>1.5</td>
<td>2.2</td>
<td>3.3</td>
<td>4.3</td>
</tr>
<tr>
<td>Noise [μV rms]</td>
<td>87</td>
<td>74</td>
<td>68</td>
<td>65</td>
</tr>
<tr>
<td>Input [mV rms] (100kHz / 1% THD)</td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>In-band IIP$_3$ [dBV]</td>
<td>-5</td>
<td>-3</td>
<td>-3</td>
<td>-3</td>
</tr>
<tr>
<td>Out-of-band IIP$_3$ [dBV]</td>
<td>3</td>
<td>5</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>Dynamic range [dB]</td>
<td>55</td>
<td>57</td>
<td>57</td>
<td>58</td>
</tr>
<tr>
<td>Tuning range [kHz]</td>
<td>$V_{tune} = V_{DD}$</td>
<td>96.5</td>
<td>88.0</td>
<td>84.5</td>
</tr>
<tr>
<td></td>
<td>$V_{tune} = 0.0$ V</td>
<td>153.0</td>
<td>154.5</td>
<td>148.0</td>
</tr>
<tr>
<td>VCO feed-thru @280kHz [μV rms]</td>
<td>104</td>
<td>85</td>
<td>72</td>
<td>72</td>
</tr>
</tbody>
</table>

- Measured CMRR (10 kHz common mode tone): 65 dB
- Measured PSRR (10 kHz tone on power supply): 43 dB

Functionality tested from 5C to 85C at 0.5 V
0.5V 1Msps 60dB T/H amplifier

- 0.25μm CMOS
- $|V_t| = 0.6V$
- 60dB SNDR
- 1Msps
- 0.6mA at 0.5V

- True low voltage
- No clk boosting
- [Chatterjee, VLSI 06, JSSC07]

Input amplitude [dBV]  
SNDR
0.5V Differential Track and Hold

- Gate-input OTA used.
- Track phase during $\phi_1$, hold phase during $\phi_2$.
- During track phase, pole and zero cancel out to enable fast response.
- pMOS switches have $V_T$ of about 0.5V.
Track mode operation

- Resistors to 0.5V maintain required OTA input CM voltage of 0.4V.
- To enable better switching, both gate and body of the switch are used.
- No voltage swing on either side of the switches.
Hold mode operation

- Gate and body of the switch used for better switching.
- No signal swing on both sides of the switches.
- OTA input voltages held constant.
Measured SNDR

<table>
<thead>
<tr>
<th>Frequency (kHz)</th>
<th>SNDR [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td></td>
</tr>
<tr>
<td>50</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td></td>
</tr>
<tr>
<td>205</td>
<td></td>
</tr>
<tr>
<td>305</td>
<td></td>
</tr>
<tr>
<td>405</td>
<td></td>
</tr>
<tr>
<td>495</td>
<td></td>
</tr>
</tbody>
</table>

Input differential rms [dBV]
# Measured performance

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>0.5V</td>
</tr>
<tr>
<td>Current consumption</td>
<td>600µA</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>1Msps</td>
</tr>
<tr>
<td>Diff. input refd. integrated noise</td>
<td>188µV&lt;sub&gt;RMS&lt;/sub&gt;</td>
</tr>
<tr>
<td>Peak SNDR f&lt;sub&gt;IN&lt;/sub&gt;=50kHz; V&lt;sub&gt;in,diff&lt;/sub&gt;=178mV&lt;sub&gt;RMS&lt;/sub&gt;</td>
<td>60dB</td>
</tr>
<tr>
<td>Peak SNDR f&lt;sub&gt;IN&lt;/sub&gt;=495kHz; V&lt;sub&gt;in,diff&lt;/sub&gt;=100mV&lt;sub&gt;RMS&lt;/sub&gt;</td>
<td>57dB</td>
</tr>
<tr>
<td>Hold mode droop rate on diff. output</td>
<td>7.6µV/µV</td>
</tr>
<tr>
<td>Pedestal on diff. output</td>
<td>0.8mV</td>
</tr>
<tr>
<td>Track mode bandwidth</td>
<td>3.9MHz</td>
</tr>
</tbody>
</table>
0.5 V 74 dB SNDR 25kHz ΣΔ Modulator

- 0.18 μm CMOS
- MIM caps
- Triple-well devices
- High-res resistors

- Body-input, gate-clocked logic
- Return-to-open feedback

- [Pun, Chatterjee, Kinget, ISSCC 06]

© Peter Kinget
3rd order CT ΣΔ Modulator

Using Active RC integrators
3rd order CT ΣΔ Modulator

Using Active RC integrators

Using Body-Input OTAs (2stages)

Using Active RC integrators

Using Body-Input OTAs (2stages)
3\textsuperscript{rd} order CT $\Sigma\Delta$ Modulator

Using Active RC integrators

Gate-clocked Body-input Comparator
$3^{rd}$ order CT $\Sigma\Delta$ Modulator

Using Active RC integrators
RZ Challenge: Switches at $V_{DD}/2$

0.25 V

Switch Conductance

$G_{\text{min}}$

nMOS

pMOS

nMOS swing

pMOS swing

$V_{DD}$

$V_{IN}$

$V_D$
Solution: Return-to-Open

When RZ: (Q=1)

Problem switches removed

0.25 V
Solution: Return-to-Open

When RZ: (Q=1)

Problem switches removed
Return-to-open CT SDM

Split Return-to-open DAC

Only switches to VDD or VSS

BW = 25kHz, fs = 3.2MHz, Vin,max = 1Vppdiff.
## Performance Summary at 25°C

<table>
<thead>
<tr>
<th>Modulator type</th>
<th>1-bit, 3rd order, continuous-time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal bandwidth</td>
<td>25 kHz</td>
</tr>
<tr>
<td>Sampling frequency / OSR</td>
<td>3.2 MHz / 64</td>
</tr>
<tr>
<td>Input range</td>
<td>1 Vppdiff.</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>0.45V</td>
</tr>
<tr>
<td>SNDR @ Vin = 1Vppdiff.</td>
<td>71 dB</td>
</tr>
<tr>
<td>SNR @ Vin = 1Vppdiff.</td>
<td>76 dB</td>
</tr>
<tr>
<td>Power consumption (total)</td>
<td></td>
</tr>
<tr>
<td>Sigma Delta Modulator Output buffers</td>
<td></td>
</tr>
<tr>
<td>Active die area</td>
<td>0.6 mm²</td>
</tr>
<tr>
<td>Technology</td>
<td>0.18 µm CMOS</td>
</tr>
<tr>
<td></td>
<td>(standard V&lt;sub&gt;T&lt;/sub&gt;, triple-well, MIM, and HiRes Poly)</td>
</tr>
</tbody>
</table>
Recent Work in 90nm CMOS

- 0.65/0.5V 2.4-2.6GHz Fractional N Freq. Synthesizer
- 0.5V 2.4GHz Sliding-IF Receiver + I/Q Baseband
- 0.5V 10Msps 8bit Pipelined ADC
0.65V/0.5V 2.4-2.6GHz Fractional-N Synthesizer

- Swings on all VCO nodes are kept within the supply rails for reliability.
- Forward body bias to enhance the divider speed.
- Fractional-N DSM dithering shifted to later divider stages to prevent noise injection into forward biased body.
- Staggered clock to prevent jittering caused by simultaneous switching.
- 90nm CMOS
- [S. Yu & P. Kinget, ISSC07]
Performance Summary

- AVDD 0.5V - 2.5mW
- DVDD 0.65V - 3.5mW
- 0.14mm$^2$ - 90nm CMOS
- RVT devices
- 2.4-2.6GHz
- Phase noise: -120dBc/Hz @ 3MHz
- Spurs: -52dBc
A 0.5V 8bit 10Mmps Pipelined ADC in 90nm CMOS

- No internal voltage or clock boosting
- Regular devices
- Cascaded sampling technique to reduce the channel leakage of the switches
- 1.5bit/stage (remark: stages identical, stages scaling not exploited)
- Front-end S/H amplifier eliminated by with an S/H for the sub-ADC.
- 0.5V OTAs with local CMFB
- 90nm CMOS
- [J. Shen & P. Kinget, VLSI07]
A 0.5V 2.4GHz Receiver

- ISM band applications
- Sliding IF topology
- LNA, Mixers, VGA + on chip RF, IF & BB filtering

[Stanic, Balankutty, Kinget, Tsividis, RFIC07] © Peter Kinget 53
0.5V Analog Roadmap

- **Body-input OTA**
- **Gate-input OTA & Biasing**
- **0.5V Varactor**
- **Comparators**
- **135kHz LPF + Tuning**
- **CT 74dB 25kHz ΣΔ A/D**
- **10b 1Ms THA**
- **900MHz RF Front-end**

Basic blocks

- 2004
- 2005
- 2006
- 2007

Complexity

- 90nm
- 180nm
- 250nm

Basic blocks
Where do we go from here...

- Other nanoscale challenges:
  - Gate & subthreshold (OFF) leakage,
  - Smaller $g_m/g_o$,
  - Reduced body effect.

- Opportunities
  - Device speed significantly improves:
    - Scale device operating points for larger $(g_m/I_D)$,
    - FinFETs, dual gate devices, ....
    - Calibrate using abundant digital gates.

- But, some fundamental limitations are against us...
Power Dissipation Limits

- Noise limited circuits [Vittoz90]:
  \[ SNR = \frac{V_{RMS}}{\sqrt{\frac{kT}{C}}} \]
  \[ \sigma^2(V_{os}) = \frac{C_{ox}A_{VT}^2}{C} \]
  \[ I_{DC} = 2fC\sqrt{2V_{RMS}} \]
  \[ P \geq 8kTfSNR^2 \]

- Mismatch limited circuits [Kinget96]:
  \[ Acc = \frac{V_{RMS}}{3\sigma(V_{os})} \]
  \[ I_{DC} = 2fC\sqrt{2V_{RMS}} \]
  \[ P \geq 24C_{ox}A_{VT}^2fAcc^2 \]

\[ V_{DD} = 2\sqrt{2}V_{RMS} \]
Low Voltage Power Penalty

- Finite $V_{DSsat}$:

$$V_{DD} = 2\sqrt{2} V_{RMS} + 2 V_{DSsat}$$

**Penalty factor**

$$= 1 + \frac{2V_{DSsat}}{V_{DD} - 2V_{DSsat}}$$

Graph showing supply voltage vs. penalty factor.
LV Challenge: Interfaces

0.5 - 1.0V

4dBm (2.5mW) @ 1.0Vpp
-2dBm (0.625mW) @ 0.5Vpp

Z Transf.

Filt./Z Match

© Peter Kinget
Ultra Low Voltage Analog Design Techniques

• Device Level:
  – Use body terminal for bias control or signal,
  – Use RSCE, optimize L to reduce $V_T$.

• Building Block Level:
  – Eliminate transistor stacks,
  – Use LCMFB, CMFF & Neg. G.

• Functional Level:
  – Revise signaling & architecture,
  – New tuning & biasing strategies.

• Demonstrated in 0.5V analog & RF building blocks & systems:
  – filters, THA, ADCs, RF front-ends, freq. synthesizers,
  – in 0.18um CMOS ($|V_T|=V_{DD}$) & 90nm CMOS.
Selection of Recent Publications

0.5V Analog/RF Integrated Circuits:


RF Integrated Oscillators:


Ultra-wideband Pulse Radio:


Injection-locking:


Device Mismatch:

Acknowledgments

• Collaborators:
  – Y. Tsividis (Columbia), K. P. Pun (City Univ. Hong Kong), S. Chatterjee (now IIT Delhi), B. Soltanian (now LSI)

• Analog Devices, Bell Labs, Intel, NSF, Realtek, Silicon Labs, SRC for financial support.

• Europractice, Philips (now NXP) and UMC for fabrication support.
Thank you for your attention

Any Questions, contact:

kinget@ee.columbia.edu

http://www.ee.columbia.edu/~kinget