0.5V Analog integrated circuits for nanoscale CMOS technologies

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Ultra-low voltage circuits: 0.5V
RF integrated oscillators
Ultra-wideband RF circuits
RF Passives
Injection locked circuits
Device mismatch & its influence on Analog & RF ICs

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Outline

• Do we need Analog Integrated Circuits in nanometer CMOS?

• Design Challenges & Opportunities.

• 0.5 V Operational Transconductance Amplifiers & Biasing Circuits.

• 0.5 V Fully Integrated Active RC Filter with on-chip Automatic Tuning.

• A 0.5V 74dB SNDR 25kHz CT $\Sigma\Delta$ Modulator with Return-to-open DAC

• Conclusions.
Analog in a *Mixed Signal* World

- Sounds, images, EM waves, …. are **ANALOG**.
- Information processing & storage are **DIGITAL**.
- System-on-chip is powerful **economic** paradigm.

Digital **drives** technology development & choice.

*Most Digital ICs need some Analog!*  

If Analog can be done in a digital technology, it **will** be done.
CMOS trends: Supply voltage

[Graph showing trends in supply voltage (Analog $V_{DD}$, Digital $V_{DD}$, and Digital $V_T$) over technology node (nm) from 1995 to 2015.]

- High Perf.
- Low Standby
- Low Power

[ITRS'04]
MOST biasing: CS or VCCS

- Transconductor or Current Source
  \[ V_{DS} > 0.15V \]  (for \( V_{GS} - V_T \leq 0.2 \))

0.24µm/0.36µm nMOS in 0.18µm CMOS

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Switches at 0.5 V

Large $V_{DD}$

Enough headroom

Small $V_{DD}$

No headroom
Common source amplifier

\[ V_{in,pp} \]

\[ V_T + (V_{GS} - V_T) \]

\[ 0.5 + 0.15 \text{ V} \]

\[ V_T = 0.5 \text{ V} \]

\[ V_{DS,sat} = 0.15 \text{ V} \]

\[ V_{out,pp} \]

\[ 0.2 \text{ V}_{pp} \]

\[ 0.5 \text{ V} \]

\[ V_{DS,sat} = 0.15 \text{ V} \]

\[ 0.15 \text{ V} \]
Common drain buffer

\[ V_{T} + (V_{GS} - V_{T}) + V_{in,p} + V_{DS,sat} \]

\[ 0.5 + 0.15 + 0.1 + 0.15 \text{ V} \]

\[ V_{T} = 0.5 \text{ V} \]

\[ V_{DS,sat} = 0.15 \text{ V} \]
Common gate amplifier / Cascode

\[ V_T + (V_{GS} - V_T) + V_{in.p} + V_{DS,sat} \]

\[ V_T = 0.5 \text{ V} \]

\[ V_{DS,sat} = 0.15 \text{ V} \]
Differential OTA design challenges

\[ V_T = 0.5 \text{ V} \]

\[ V_{DS,sat} = 0.15 \text{ V} \]
CMFB for fully differential OTAs

Common Mode Feedback requires ‘fast’
amplifier operating from $V_{out,CM} = \frac{V_{DD}}{2}$ !?
Challenges at 0.5 V

- $V_{DS,sat}$ related challenges:
  - Independent of region of operation!
  - Independent of $V_T$!
  - Signal swings are limited:
    - Use differential circuits.
  - Avoid transistor stacks:
    - No tail current source: How to achieve CM rejection?
    - No cascodes: How to increase DC gain?

- $V_{GS}$ related challenges:
  - Depend on region of operation & ($V_{GS}$-$V_T$).
  - Depend on $V_T$!
  - Avoid signal swing on gate:
    - How to do overall CMFB?
    - How to achieve strong inversion operation?
Opportunities at 0.5 V: MOST has 4-terminals

nMOS circuit equivalent (deep n-well process)

nMOS cross section (deep n-well process)
Opportunities at 0.5 V

- Body terminal
  - Signal input: [Guz87]
  - $V_T$ reduction & control
    [Kob94], [Von94]
  - Bias control
- Latch-up not an issue
  - Assuming $V_{DD}$ and GND are ‘well behaved’.
- Techniques can be ported to ‘double gate’ devices

0.24µm/0.36µm nMOS in 0.18µm CMOS
0.5 V Gate-input OTA
0.5 V Gate-input OTA stage

\[ V_{\text{in}+} \]

\[ V_{\text{in}-} \]

\[ V_{\text{out}+} \]

\[ V_{\text{out}-} \]

\[ V_{\text{bn}} \]

\[ V_{\text{NR}} \]
Two stage OTA

- Common-mode output of first stage is 0.4 V
Two-stage fully differential 0.5 V OTA with Miller compensation
Setting common-mode voltages

\[ R_b = \frac{2}{3} \cdot R_i \parallel R_f \]
Open loop performance (meas.)

- Gain [dB]: 62 dB
- Frequency [Hz]: 10 MHz
- GBW: 10 MHz
- 350mV; automatic bias
- \( C_L = 10\text{pF (diff.)} \)
- \( R_L = 50\text{k}\Omega \)
- \( I_{DD} = 150\ \mu\text{A} \)

Increasing gain—boosting bias
On-chip automatic biasing circuits
On-chip biasing circuits

V_{bn} generating circuit

Level shift biasing circuit

(Simplified OTA)
Error amplifier for biasing

- 20 kHz GBW for 1 pF load
- 2 μA current
- Controlled body voltage sets the amplifier threshold
OTA DC transfer characteristics and $V_{NR}$ generation

- **Input differential voltage [mV]**
  - $V_{NR}$ generating circuit
  - Replica of OTA stage 1

Graph showing the relationship between input differential voltage and output differential voltage, with arrows indicating the increasing $V_{NR}$.
Open loop performance (meas.)

Gain [dB]:
- 62 dB
- 42 dB

Frequency [Hz]:
- 350mV; automatic bias
- GBW: 10 MHz

Component values:
- $C_L = 10\text{pF (diff.)}$
- $R_L = 50\Omega$
- $I_{DD} = 150\ \mu\text{A}$
0.5 V Continuous time tunable active RC Filter
0.5 V 5th order elliptic LPF

Gain [dB]

Frequency [Hz]

135 kHz
280 kHz
Filter tuning challenges at 0.5 V

- Gm-C
- MOSFET-C
- Switching banks of R’s and C’s
- Varactor-R techniques

\[ \frac{C_{gs}}{C_{ox}} \]

\[ V_{tune} \]
Low-voltage tunable integrator

\[ V_{in} \]

\[ V_{out} \]

\[ C_{fixed} \]

\[ C_{var} \]

\[ V_{tune} \]

\[ 2/3 \cdot R_1\|R_2 \]

\[ 0.25 \text{ V} \]

\[ 0.4 \text{ V} \]

\[ R_1 \]

\[ R_2 \]

\[ V_{DD} \]

\[ V_{DD} \]
Die photograph

- 0.18 µm CMOS
- MIM capacitors
- High-res resistors
- Standard $V_T$
- Triple well devices

Measured filter response for different supply voltages
Measured filter response for different chips

1.3 % std dev in cut-off frequency for 20 samples
Measured filter response for different tuning voltages

88 - 154 kHz (1.75x)
Measured 3rd order intermodulation

Output differential rms amplitude [V]

Input differential rms amplitude [V]

- 15 kHz
- 20 kHz
- 25 kHz
- 30 kHz
- 40 dB
Effect of gain enhancement

Graph showing the comparison of gain with and without gain enhancement over a range of frequencies. The graph indicates that gain enhancement significantly improves the performance at higher frequencies.
# Performance summary at 27°C

<table>
<thead>
<tr>
<th></th>
<th>$V_{DD}$ [V]</th>
<th>0.45</th>
<th>0.50</th>
<th>0.55</th>
<th>0.60</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3 dB cut-off frequency [kHz]</td>
<td></td>
<td>135.0</td>
<td>135.0</td>
<td>135.0</td>
<td>135.0</td>
</tr>
<tr>
<td>Total current [mA]</td>
<td></td>
<td>1.5</td>
<td>2.2</td>
<td>3.3</td>
<td>4.3</td>
</tr>
<tr>
<td>Noise [μV rms]</td>
<td></td>
<td>87</td>
<td>74</td>
<td>68</td>
<td>65</td>
</tr>
<tr>
<td>Input [mV rms] (100kHz / 1% THD)</td>
<td></td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>In-band IIP$_3$ [dBV]</td>
<td></td>
<td>-5</td>
<td>-3</td>
<td>-3</td>
<td>-3</td>
</tr>
<tr>
<td>Out-of-band IIP$_3$ [dBV]</td>
<td></td>
<td>3</td>
<td>5</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>Dynamic range [dB]</td>
<td></td>
<td>55</td>
<td>57</td>
<td>57</td>
<td>58</td>
</tr>
<tr>
<td>Tuning range [kHz]</td>
<td>$V_{tune} = V_{DD}$</td>
<td>96.5</td>
<td>88.0</td>
<td>84.5</td>
<td>69.0</td>
</tr>
<tr>
<td></td>
<td>$V_{tune} = 0.0$ V</td>
<td>153.0</td>
<td>154.5</td>
<td>148.0</td>
<td>150.5</td>
</tr>
<tr>
<td>VCO feed-thru @280kHz [μV rms]</td>
<td></td>
<td>104</td>
<td>85</td>
<td>72</td>
<td>72</td>
</tr>
</tbody>
</table>

- Measured CMRR (10 kHz common mode tone): 65 dB
- Measured PSRR (10 kHz tone on power supply): 43 dB

Functionality tested from 5°C to 85°C at 0.5 V
0.5 V Body-input OTA
0.5 V Body-input OTA stage
Two-stage fully-differential OTA


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Open loop frequency response

- DC gain: 52 dB
- GBW: 2.5 MHz
- Phase Margin: 45°

Simulation
Measurement

Frequency [Hz]

Gain (dB)
Phase (degrees)
<table>
<thead>
<tr>
<th></th>
<th>[Bla 98]</th>
<th>[Las 00]</th>
<th>[Leh 01]</th>
<th>[Sto 02]</th>
<th>[Fer 96]</th>
<th>[Pel 98]</th>
<th>B-I</th>
<th>G-I</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$ [V]</td>
<td>1</td>
<td>1</td>
<td>0.8</td>
<td>0.9</td>
<td>1.3</td>
<td>0.9</td>
<td>0.5</td>
<td>0.5</td>
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<tr>
<td>$A_{DC}$ [dB]</td>
<td>49</td>
<td>70</td>
<td>53</td>
<td>70</td>
<td>84</td>
<td>59</td>
<td>52</td>
<td>50/62</td>
</tr>
<tr>
<td>GBW [MHz]</td>
<td>1.3</td>
<td>0.2</td>
<td>1.3</td>
<td>6e-3</td>
<td>1.3</td>
<td>4</td>
<td>2.5</td>
<td>10</td>
</tr>
<tr>
<td>Power [uW]</td>
<td>300</td>
<td>5</td>
<td>-</td>
<td>0.5</td>
<td>460</td>
<td>-</td>
<td>110</td>
<td>75</td>
</tr>
<tr>
<td>$C_L$ [pF]</td>
<td>22</td>
<td>7</td>
<td>20</td>
<td>12</td>
<td>-</td>
<td>14</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>SE/Diff.</td>
<td>S</td>
<td>S</td>
<td>S</td>
<td>S</td>
<td>S</td>
<td>D</td>
<td>D</td>
<td>D</td>
</tr>
<tr>
<td>Techn. [um]</td>
<td>2</td>
<td>0.35</td>
<td>0.5</td>
<td>2.5</td>
<td>0.7</td>
<td>0.5</td>
<td>0.18</td>
<td>0.18</td>
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<tr>
<td>Special Devices</td>
<td>Lat. BJT</td>
<td>Lat. BJT</td>
<td>Depl. MOS</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$100 \eta$ [1/V]</td>
<td>9.5</td>
<td>28</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
<td>11.4</td>
<td>66.7</td>
</tr>
</tbody>
</table>

A 0.5V 74dB SNDR 25kHz
CT ΣΔ Modulator
with Return-to-open DAC
3\textsuperscript{rd} order CT $\Sigma\Delta$ Modulator

Using Active RC integrators

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Continuous-time $\Sigma\Delta$ Modulator: Need of Return-to-zero DAC

**ISI exists**: area for each “1” depends on its previous symbol.

**No ISI**: same area for all “1”s.

A typical active-RC CT SDM stage
RZ Challenge: Switches at $V_{DD}/2$

- $0.25$ V
- $0.5V_{VCM}$
- $0V$
- RZ DAC_n
- Rdac
- C
- Vin
- Ri
- Rdac
- C
- D0
- $\phi_{RZ}$
- D1
- $0.25$ V

\[ Q = 0 \quad 1 \quad 1 \quad 0 \quad 0 \quad 1 \]

\[ \phi_{RZ} \]

\[ D0 = \overline{Q} \cdot \overline{\phi_{RZ}} \]

\[ D1 = Q \cdot \overline{\phi_{RZ}} \]
Solution: Return-to-open

Before RZ: (Q=1)

Problem switches removed

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Solution: Return-to-open

When RZ:
\( Q = 1 \)

```
0.5V  0V
D0    D1
```

RTO DAC_n

```
V1
0.5V  0V
```

```
Vin
Ri
```

```
Rdac
```

```
+  -
```

```
C
```

```
V2
```

```
D1
0.5V  0V
D0
```

RTO DAC_p

```
RZ
```

```
D0
```

```
Q
```

```
Ts
t
```

```
V_{cm,ota}
```

```
V_{dac}
```

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Solution: Return-to-open

When RZ:
\[ Q = 1 \]

0.25 V

"floats"

RTO DAC_n

RTO DAC_p

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RTO SDM: Inter-stage Coupling

Unwanted signal paths when DAC floats
Split RTO SDM Architecture

Split RTO DAC
Modulator Details

Modulator Details

- **50% duty cycle**
- **BW = 25kHz, fs = 3.2MHz, Vin,max = 1Vppdiff.**
- **10%Ts delay**: to allow the comparator outputs to fully settle before the DACs become active.
$\phi_{DAC}$ High:

```
RTO DAC Circuit

$\phi_{DAC}$

Q
M1
M2
M3
M4
M5
M6
M7
VREFN
VREFP
Vbp
Vbp
Vbp
Vbp
Vbp
Vbp
Vbp

All the bodies tied to $V_{DD}/2$.

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```
\( \phi_{DAC} \) Low:

All the bodies tied to \( V_{DD}/2 \).

Floating.
RTO DAC Circuit

$\phi_{DAC}$ Low:

- $Q$ invalid for $\phi$ low.
- All the bodies tied to $V_{DD}/2$. (Floating.)
\( \phi_{DAC} \) Low:

- Make charge-injection signal-independent.
- \( Q \) invalid for \( \phi \) low.
- Floating.
- All the bodies tied to \( V_{DD}/2 \).
RTO DAC Circuit

Just split M5-M7 for each FB path.

All the bodies tied to $V_{DD}/2$. 

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Waveform of RTO DAC

- Same shape for all “1”s
- No ISI

Simulated output waveform of 1st DAC

- DAC floating
- DAC active

OTA input
0.5V Body-input Gate-clocked Comparator

Pre-Amp

Latch

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0.5V Fully Differential OTA

• Measurements on a replica of the 1\textsuperscript{st} OTA:
  – $A_{DC} = 46\text{dB}$, $UGB = 4\text{MHz}$;
  – Input referred noise:
    $33\text{nV}_{rms} @10\text{kHz}$ and $12\text{nV}_{rms} @1\text{MHz}$.
K.P. Pun, S. Chatterjee, and P. Kinget, "A 0.5 V 74dB SNDR 25kHz CT Delta-Sigma Modulator with Return-to-Open DAC" in IEEE International Solid-State Circuits Conference (ISSCC), pp. 72-73, February 2006.

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Measured Output Spectrum

FFT points = 64000
Res. BW = 50 Hz

2^{nd} harmonic < 83dBc
3^{rd} harmonic < 88dBc

@Vin = -4dB Vref, fin = 5kHz
(Vref = 1Vppdiff.)
Measured SNDR versus Vin

Peak SNDR: 74dB

(Vref = 1Vppdiff.)
# Performance Summary at 25°C

<table>
<thead>
<tr>
<th>Modulator type</th>
<th>1-bit, 3rd order, continuous-time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal bandwidth</td>
<td>25 kHz</td>
</tr>
<tr>
<td>Sampling frequency / OSR</td>
<td>3.2 MHz / 64</td>
</tr>
<tr>
<td>Input range</td>
<td>1 Vppdiff.</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>0.45V</td>
</tr>
<tr>
<td>SNDR @ Vin = 1Vppdiff.</td>
<td>71 dB</td>
</tr>
<tr>
<td>SNR @ Vin = 1Vppdiff.</td>
<td>76 dB</td>
</tr>
<tr>
<td>Power consumption (total)</td>
<td></td>
</tr>
<tr>
<td>Sigma Delta Modulator (filter + comparator + DAC)</td>
<td>370 μW</td>
</tr>
<tr>
<td>Output buffers</td>
<td></td>
</tr>
<tr>
<td>Active die area</td>
<td>0.6 mm²</td>
</tr>
<tr>
<td>Technology</td>
<td>0.18 μm CMOS (standard $V_T$, triple-well, MIM, and HiRes Poly)</td>
</tr>
</tbody>
</table>
SNDR versus $V_{DD}$

@25°C and $V_{in} = 1V_{ppdiff}$. 
SNDR versus Temperature

@\(V_{DD} = 0.5V\) and \(Vin = 1V_{ppdiff}\).
# Performance Comparison

<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>Grech 1999</td>
<td>1</td>
<td>SO</td>
<td>56⁺</td>
<td>3.9</td>
<td>1500</td>
<td>0.9⁺⁺</td>
<td>0.8</td>
<td>1.3</td>
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<td>Keskin 2001</td>
<td>1</td>
<td>RO</td>
<td>78</td>
<td>20</td>
<td>5600</td>
<td>0.41</td>
<td>0.35</td>
<td>23</td>
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<td>Matuya 1994</td>
<td>1</td>
<td>CT</td>
<td>51</td>
<td>192</td>
<td>1560</td>
<td>2.53</td>
<td>0.5</td>
<td>Low VT 36</td>
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<td>Dessouky 2000</td>
<td>1</td>
<td>SC</td>
<td>85</td>
<td>25</td>
<td>950</td>
<td>0.63</td>
<td>0.35</td>
<td>Gate boost 381</td>
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<tr>
<td>Yao 2004</td>
<td>1</td>
<td>SC</td>
<td>81</td>
<td>20</td>
<td>140</td>
<td>0.18</td>
<td>0.09</td>
<td>1310</td>
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<tr>
<td>Ueno 2004</td>
<td>0.9</td>
<td>CT</td>
<td>50.9</td>
<td>1920</td>
<td>1500</td>
<td>0.12</td>
<td>0.13</td>
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<td>Peluso 1998</td>
<td>0.9</td>
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<td>62</td>
<td>16</td>
<td>40</td>
<td>0.85</td>
<td>0.5</td>
<td>410</td>
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<td>Sauerbrey 2002</td>
<td>0.7</td>
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<td>67</td>
<td>8</td>
<td>80</td>
<td>0.082</td>
<td>0.18</td>
<td>58</td>
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<tr>
<td>Ahn 2005</td>
<td>0.6</td>
<td>SRC</td>
<td>77</td>
<td>24</td>
<td>1000</td>
<td>2.88</td>
<td>0.35</td>
<td>Low VT 138</td>
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<td>This work</td>
<td>0.5</td>
<td>CT</td>
<td>74</td>
<td>25</td>
<td>300</td>
<td>0.6</td>
<td>0.18</td>
<td>340</td>
</tr>
</tbody>
</table>

⁻⁻SNR only; ** Estimated from die photograph;  
SO = Switched Opamp; CT = Continuous Time;  
SC = Switched Capacitor; RO = Reset Opamp;  
SRC=Switched-RC  
FOM = resolution × \( \frac{BW}{P} \)
Analog design techniques at 0.5 V

• How to do CM rejection?
  Use local CM feedback & rejection
  Use CM feedforward cancellation
  Separate CM signal rejection and CM DC biasing

• How to increase DC gain?
  Use negative load conductance

• How to use strong inversion operation?
  Forward Body Bias to reduce $V_T$

  Extensive use of the body terminal
  Extensive use of on-chip tuning & biasing
  Architectural changes to eliminate signal path switches
Looking ahead
0.5V 900MHz RF Front-end

- 0.18 µm CMOS
- Low-$V_T$ devices
- LNA/MIXER
  - NF 8.8 dB
  - Gain 11.5 or-7 dB
  - ICP -23 dBm
  - 5 mW
  (w/ LO Buffers)

0.5 V 1 Msample/s 60 dB SNDR Track&Hold

- 0.25 µm CMOS
- $|V_T| = 0.6V$
- MIM caps
- High-res resistors
- Triple well nMOS

0.5V Analog Roadmap

- Body-input OTA
- Gate-input OTA & Biasing
- 0.5V Varactor
- LPF + Tuning
- ΔΣ Converter
- THA
- RF Front-ends
- Basic blocks
- Full Interface

Timeline:
- 2004
- 2005
- 2006
- 2007

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Other Challenges in nanometer CMOS

- Gate leakage.
- Sub-threshold leakage.
- Reduced body-effect [VonAmin05]:
  \[ V_T \in \mathbb{F} \quad & \quad t_{ox} \in \mathbb{F} \quad & \quad g_{mb} \in \mathbb{F} \]

Other Opportunities in nanometer CMOS

- Many \( V_T \) choices !
- Novel devices.
- *Extensive* Digital Calibration & Correction.
CMOS Trends: On chip Clock Speed

Technology node [nm]

[ITRS'04]
Acknowledgments

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More details


References


References


