## **R-3: Analog Rump Session**

## Digitizing the Radio to the Antenna - Will Radios Still Need Analog in 2010? [Suzaku III]

Organizer: A. Matsuzawa, Tokyo Institute of Technology

M. Huang, Freescale

Moderator: P. Kinget, *Columbia University* Panelists: T. Arnaud, *STMicroelectronics* 

Q. Huang, Swiss Federal Institute of Technology

C.-M. Hung, *Texas Instruments* H. Kobayashi, *Gunma University* 

I. Mehr, *Analog Devices* S. Tanaka, *Hitachi* 

It is becoming more challenging to maintain analog circuit performance and yield as device technology is scaled. Some scaling trends that significantly impact analog circuits include: reduction in supply voltage, decreased GmRo ratio, increased device leakage, and the impact of high-k gate dielectric materials and non-planar device structures on 1/f noise and transistor matching. Additionally, the inability to scale the area of passive components such as capacitors and inductors makes it progressively more and more expensive to incorporate analog functions on digital heavy mixed signal chips such as communication transceivers.

Recent research on replacing traditional analog and RF functions with digital circuits holds out the promise of a low-cost, single chip, all CMOS digital radio supporting multiple standards. Can the radio function indeed be "digitized" up to the antenna? How to realize such a radio? Or are analog and RF functions such as low noise amplifiers, mixers and filters, irreplaceable by digital circuits?

## Joint Rump Session with Technology

## J-R: Variability Has Stopped Scaling: Who Will Conquer the Issues of Variability?

- -Will Technology People Be Able to Keep the Device Variability?
- -Will Design Technology Take the Further Device Variability into Account?

Organizers: K. Ishibashi, Renesas Technology

H. Masuda, STARC

B. Nikolic, University of California, Berkeley

R. Rakkhit, Cypress Semiconductor

Moderator: H.-S.P. Wong, Stanford University

Panelists: M. Hashimoto, Osaka Univ.

H. Ando, Fujitsu

T. Hiramoto, *Univ. of Tokyo* H. Oyamatsu, *Toshiba* S. Naffziger, *Intel* M. Pelgrom, *Philips* C. Wann, *IBM* 

With further minimization of features in CMOS technology it becomes apparent that the tolerances on minimum features do not track scaling of features. There are increasing wafer-to-wafer, chip-to-chip and within-chip variations due to line-width variations, edge roughness or dopant fluctuations. In order to achieve predictable product performance there is a need for changes in the requirements for new devices, circuit designs or tool flows. Should the technology focus on developing the devices with better control rather than better average performance? Should the designers be those who absorb the variability in their designs? Or, will the problem be solved by the tools that allow for statistical IC design? Our panel of experts will present their opinions on these topics and discuss the breakthrough to overcome the issue.

\*This session will be held at 20:00-22:00 on Wednesday, June 15