





### RF Circuit and System Innovations for a New Generation of Wireless Terminals

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# Analog & RF Design Research

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### Outline

- <u>System</u> problem setting: The RF Spectrum Crunch
- <u>Circuit</u> Solutions enabled by <u>Device</u> Scaling
  - Field Programmable Receivers
  - Getting by with Switches and Capacitors ...
- <u>Circuit</u> Solutions assisted by Digital <u>Signal</u>
   <u>Processing</u>

Compressive Sampling for RF Spectrum Scanning

Conclusions



### "Data Storm"

#### More Devices x More Content = 1,000x Data Storm



#### From: www.qualcomm.com/1000x

#### **Artificial Spectrum Scarcity**

Today's Wireless Communications

Spectrum Mobile frequencies are getting crowded Usage Ambulance Defense Radat マ Source: Nokia Frequency **Spectrum Measurements** Sample Time: 2560n in New York City **Power** -20





#### **Overcoming the Artificial Spectrum Scarcity**

**Today's Wireless Communications** 



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#### **Cognitive Radio**

✓ Dynamic

Source: Nokia

- ✓ Opportunistic
- ✓ Adaptive
- ✓ Spectrum Aware

#### **Modern Mobile Phone**



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#### Examples of Next Generation Wireless Systems



#### "Next-Generation" Receiver



- Next-generation receivers need:
  - Field programmability avoid worst-case design strategy
  - Wideband Operation & out-of-band blocker tolerance with limited off-chip filtering
  - Fast & Low power & Wideband Spectrum Sensing

### **Desired Circuit Innovations**

- Highly Flexible Circuits

   programmable operation:
   f<sub>0</sub>, BW, NF, IIP<sub>3</sub>, P
- Simplified Antenna FEM
   SW-Cap RF Front End
- Spectral Awareness

   Compressive Sampling
   based Spectrum Scanning

Circuit Techniques	Device Scaling	Signal Processin
		sing

### **CMOS Device Scaling**

#### Device Gate Length

#### Device Switching Speed



#### Device density & speed **↑**

From: ITRS CMOS Roadmap

### Field-Programmable Receiver with Hybrid Class-AB-C LNTAs



Rs

- 40nm CMOS LP technology
- 1.8mm x 1.3mm
- Active area: 1.6mm<sup>2</sup>
- Noise canceling Rx
- FP LNTAs and TIAs
- 4 phase passive mixers
- Cartesian based combiner



### Hybrid Class-AB-C: Ultra-Linear LNTA



### Field-Programmability for Hybrid Class-AB-C LNTAs



	C	CG I	LNTA	١s			C	S L	NTA	١s		
		1	2		1	2	3	4	5	6	7	8
Low Noise	P:	AB	С		AB							
Mode	N:	С	AB		AB							
		1	2		1	2	3	4	5	6	7	8
High	P:	AB	С		AB	С	AB	С	AB	С	AB	С
Mode	N:	С	AB		С	AB	С	AB	С	AB	С	AB
		1	2		_1	2	3	4	5	6	7	8
Low	P:	AB	С		OFF							
Mode	N:	С	AB		OFF							

- CG-LNTA has 2 slices
- CS-LNTA has 8 slices
- Cascode transistors are shared
- Each transistor slice can be biased separately into class-AC, class-C or OFF



### Field Programmable Performance Profile

Measurements @f<sub>lo</sub>=900MHz



#### Measured Performance



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Device Scaling Circuit Techniques
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Signal Processing

### RF Front End with Only Switches & Capacitors



#### Switched-Capacitor RX with High Blocker Tolerance



High selectivity linear tunable filter is required for high blocker tolerance in reconfigurable RX



### **Blocker-Tolerant RX Design Solutions**



### **Blocker-Tolerant RX Design Solutions**



### **Blocker-Tolerant RX Design Solutions**



### Switched-Cap. RF Front End



#### Impedance matching Sampling

N-path filtering

Impedance matching and sampling

f<sub>s</sub>=8f<sub>lo</sub>

High order DT IIR filtering Harmonic-rejecting downconversion  $\begin{array}{c} 1/f_{s} \\ p_{1} \\ p_{2} \\ p_{2} \\ \vdots \\ p_{8} \\ \hline p_{8} \\ \hline p_{8} \\ \hline p_{1} \\ \hline p_{2} \\ \hline p_{1} \\ \hline p_{2} \\ \hline p_{1} \\ \hline p_{2} \\ \hline p_{3} \\ \hline p_{4} \\ \hline p_{1} \\ \hline p_{1} \\ \hline p_{1} \\ \hline p_{2} \\ \hline p_{3} \\ \hline p_{4} \\ \hline p_{1} \\ \hline p_{1} \\ \hline p_{2} \\ \hline p_{3} \\ \hline p_{4} \\ \hline p_{1} \\ \hline p_{2} \\ \hline p_{3} \\ \hline p_{4} \\ \hline p_{1} \\ \hline p_{2} \\ \hline p_{3} \\ \hline p_{4} \\ \hline p_{1} \\ \hline p_{1} \\ \hline p_{2} \\ \hline p_{3} \\ \hline p_{4} \\ \hline p_{1} \\ \hline p_{2} \\ \hline p_{3} \\ \hline p_{4} \\ \hline p_{5} \hline$ 

#### Harmonicrejecting downconversion

#### Switched-Cap RF Front End



Process:
40nm LP CMOS
Active Area:
1.4mm x 1.45mm

#### Switched-Cap. RF Front End Functional Equivalence





#### **Conversion Gain**



#### **Conversion Gain & B1dB**



Measured at 200MHz LO frequency

#### **Performance Comparison**



	SCRX	N-path	n filter	Mixer-f	irst RX
	This work	[Darvis	shi-16]	[Andrev	ws-10]
Filter order before active circuits	1-4	1		1	
Attenuation (dB)	0	0	8	0	10
Max. B1dB (dBm)	15	7	15	5	15
Noise Figure (dB)	6.8	2.8	10.8	3.5	13.5

## **Desired Circuit Innovations**

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Device Scaling Circuit Techniques	Signal Processing
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### **Traditional Spectrum Scanner/Sensors**



System Attributes	Sweeping Scanner	Multi-Branch Sensor		
Scan Time	×	✓		
Power Consumption	$\checkmark$	×		
Hardware Complexity	✓	×		

**Energy Consumption = Scan Time x Power = Constant for both approaches** 

Fixed trade-off between Scan Time & Power

#### **Compressive Sampling (CS) to the Rescue**



#### Quadrature Analog-to-Information Converter (QAIC)



#### Analog Preprocessing for Compressive Sampling with Pseudorandom (PN) Sequences



Block diagram of a PN Mixer + LPF



# Quadrature Analog-to-Information Converter (QAIC)



#### **Quadrature Analog-to-Information Converter** (QAIC) **Band-pass CS Approach**



**PN Sequence** Clock Freq. = 1.26GHz Length = 63

# of Branches = 8 I/Q

#### Energy Consumption

Power Cons. = 80mW Scan Time = 4uSec



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#### **Rapid Interferer Detector Demonstration**

**QAIC SYSTEM** 

ADC/FPGA

SAMPLING SYSTEM

#### 1GHz MULTI-BAND SIGNAL GENERATOR



#### Wideband Rapid Interferer Detection with a Compressed Sampling QAIC



#### Wideband Rapid Interferer Detection RF Span=1GHz; T=4.4uS

#### **QAIC Detector Time Agility**

### Comparison of Spectrum Scanner/Sensor Architectures

System Attributes	Sweeping Spectrum Scanner	Nyquist FFT Spectrum Sensor	QAIC
Scan Time	220µs	4µs	4.4µs ➡ <b>50x faster</b>
Energy Consumption	50E	50E	E 50x lower
Aggregate Sampling Rate	40MS/s	2GS/s	320MS/s 6.3x compression

RBW=20MHz, 1GHz wideband spectrum ranging from 2.7 to 3.7GHz

### Spectrum Scanners/ Sensors Performance Plane



### Conclusions

- <u>Device</u> scaling enables new <u>circuit</u> solutions for RF applications
- Advanced <u>signal processing</u> concepts enable novel architectures for RF signal processing
- Reconfigurable performance profiles, on-chip DT filtering, and energy-efficient spectrum scanning, will become critical features in cognitive terminals for next generation wireless <u>systems</u>

#### "Crossing the boundaries" enables RF circuit and system innovations

### References

- T. Haque, R. Yazicigil, J. Wright, and P.R. Kinget, "Theory and Design of a Sub-Nyquist Analog-to-Information Converter for Energy Efficient Wideband Spectrum Sensing," IEEE Transactions on Circuits and Systems I, 2014.
- R. Yazicigil, T. Haque, M. Whalen, J. Yuan, J. Wright, and P.R. Kinget, "A 2.7-3.7GHz Rapid Interferer Detector Exploiting Compressed Sampling with a Quadrature Analog-to-Information Converter," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2015.
- R. Yazicigil, T. Haque, M. Whalen, J. Yuan, J. Wright, and P.R. Kinget, "Wideband Rapid Interferer Detector Exploiting Compressed Sampling with a Quadrature Analog-to-Information Converter," IEEE Journal of Solid-State Circuits, invited, pp. 3047-3064, Dec. 2015.
- R. Yazicigil, T. Haque, M. Kumar, J. Yuan, J. Wright, and P. R. Kinget, "Time-Segmented Quadrature Analog-to-Information Converter for Rapid Detection of up to 6 Interferers in the 2.7-3.7GHz PCAST Band," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2016.
- R. Yazicigil, T. Haque, J. Zhu, Y. Xu, and P. R. Kinget, "RF Circuit and System Innovations for a New Generation of Wireless Terminals," IEEE International Symposium on Circuits and Systems (ISCAS), invited talk, Special Session on "Design Enhancements and Simulation Methods for Radio Frequency Circuits and Systems in Emerging Applications," May 2016.
- Y. Xu and P. R. Kinget, "A Switched-Capacitor RF Front End with Embedded Programmable High Order Filtering and a +15dBm OB-B1dB," IEEE Radio Frequency Integrated Circuits Symposium (RFIC), June 2015.
- Y. Xu, and P. R. Kinget, "A Switched-Capacitor RF Front End with Embedded Programmable High-Order Filtering," IEEE Journal of Solid-State Circuits, invited, vol. 51, no. 5, pp.1154-1167, 2016.
- Y. Xu and P. R. Kinget, "A Chopping SwitchedCapacitor RF Receiver with Integrated Blocker Detection, +31dBm OBIIP3, and +15dBm OBB1dB," IEEE Symposium on VLSI Circuits, June 2016.
- J. Zhu and P.R. Kinget, "A Field-Programmable Noise-Canceling Wideband Receiver with High-Linearity Hybrid Class-AB-C LNTAs," IEEE Custom Integrated Circuits Conference (CICC), Sept. 2015.

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### Thank You for Your Attention

#### **Crossing The Boundaries**

