



IEEE Electron Devices and Solid-State Circuits Hong Kong Joint-Chapter

Jointly Present a Seminar on

| Title: | Designing Analog and RF Circuits in Nanoscale CMOS Technologies: |
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| | Scale the Supply, Reduce the Area and Use Digital Gates. |
| Speaker: | Professor Peter Kinget |
| | Dept. of Electrical Engineering, Columbia University, New York, USA |
| Time: | 10:30am – 12:00noon |
| Date: | 22 September 2009 (Tuesday) |
| Venue: | Room 222, Ho Sin Hang Engineering Building, CUHK |

Abstract:

We will present our recent research that has centered around three themes aimed at designing analog and RF interface circuits in digital nanoscale CMOS processes. Design techniques for analog and RF circuits operating well below 1V can keep them compatible with future low power SOCs. Reclaiming the space under inductors is necessary to reduce area and cost. Digital gates can facilitate self-calibration for RF front ends to improve performance and simplify design.

Biography of the speaker:

Peter R. Kinget received an engineering degree in electrical and mechanical engineering and the Ph.D. in electrical engineering from the Katholieke Universiteit Leuven, Belgium.

He has worked in industrial research and development at Bell Laboratories, Broadcom, Celight and Multilink before joining the faculty of the Department of Electrical Engineering, Columbia University, NY in 2002. His research interests are in analog and RF integrated circuits and signal processing using nanoscale CMOS technologies.



He has been an Associate Editor of the IEEE Journal of Solid State Circuits (2003-2007) and is currently an Associate Editor for the IEEE Transactions on Circuits and Systems II. He is also serving on the Technical Program Committees of the International Solid-State Circuits Conference and the European Solid-State Circuits Conference. He is a "Distinguished Lecturer" for the IEEE Solid-State Circuits Society.

*** ALL ARE WELCOME *** Enquiry: Prof. K.P. Pun, Tel.: 2609 8293