**Example: Miller Opamp in 0.5um CMOS technology**

**Schematic:**
Below is the schematic for the Miller Opamp evaluated in this example. The load capacitor is assumed to be 10pF. In this example $I_{\text{BIAS}}$ was (arbitrarily) set to 100uA. $M5_{\text{ref}}, M5, M7, M3$ and $M4$ were sized for a $V_{GS-VT}$ of 300 to 500mV whereas $M1, M2$ and $M6$ were sized for a $V_{GS-VT}$ of about 200mV (see DC operating point information below).
For this example a 0.5um CMOS technology was used; the level 3 CMOS model parameters are included in the spice simulation deck.
This example was simulated using a port to windows of Spice3. Links to several ports are listed on the class homepage.

![Schematic Diagram]

**Spice3 Simulation Deck:**

```
** Miller Opamp 0.5um CMOS **
**
** P. Kinget 03-2002
*** circuit description ***
* as=w*1um ps=w+w/3+1u+1u
* M1  d1 inn source source pmos w=12.5u L=0.5u as=40p ad=40p ps=55u pd=55u
M2  d2 inp source source pmos w=12.5u L=0.5u as=40p ad=40p ps=55u pd=55u
M3  d1 d1 vss vss nmos w=2.5u L=0.5u as=3p ad=3p ps=6u pd=6u
M4  d2 d1 vss vss nmos w=2.5u L=0.5u as=3p ad=3p ps=6u pd=6u
M6  out d2 vss vss nmos w=10u L=0.5u as=30p ad=30p ps=42u pd=42u
M5  source pbias vdd vdd pmos w=5u L=0.5u as=20p ad=20p ps=29u pd=29u
M7  out pbias vdd vdd pmos w=5u L=0.5u as=20p ad=20p ps=29u pd=29u
```
* compensation capacitor
Cc d2 outz 10p
Rc outz out 1.5

* load
Cload out vss 10p

* biasing
M5ref pbias pbias vdd vdd pmos w=5u L=0.5u as=20p ad=20p ps=29u pd=29u
Ibias pbias vss 100u

* power supplies
vdd vdd 0 3.3
vss vss 0 0

* itest 0 out dc 0 ac 1

* differential ac input ; dc for inn is set by feedback
* differential in reference
vind indref vss dc 0 ac 1
rindref indref vss 1000

* vcm reference
vcm vcm vss 1.5

* sources & source resistances
einp inps vcm indref vss 0.5
Rsp inp inps 100
einn inns vfb indref vss -0.5
Rsn inn inns 100

* very lf feedback for dc operating point
Efb outbuf vss out vss 1
Rfb outbuf vfb 1k
Cfb vfb vss 1

*** simulation commands ***
*.op
*.ac dec 10 1 100e9
*.pz inp inn out vss vol pz

* you can use a nodeset to speed up the dc convergence.
* .nodeset
* + v(d1) = 9.346309e-001
* + v(d2) = 7.622190e-001
* + v(indref) = 0.000000e+000
* + v(inn) = 1.499637e+000
* + v(out) = 1.499637e+000
* + v(pbias) = 1.991110e+000
* + v(source) = 2.641648e+000
* + v(vcm) = 1.500000e+000
* + v(vdd) = 3.300000e+000
* + v(vss) = 0.000000e+000
* + v(vfb) = 1.499637e+000
* + v(outbuf) = 1.495894e+000

.options itl1=50e3 itl2=50e3

*** transistor models
*SPICE LEVEL3 PARAMETERS
.MODEL NMOS NMOS LEVEL=3 PHI=0.7 TOX=9.5E-09 XJ=0.2U TPG=1
  + VTO=0.7 DELTA=8.8E-01 LD=5E-08 KP=1.56E-04
  + UO=420 THETA=2.3E-01 RSH=2.0E+00 GAMMA=0.62
  + NSUB=1.40E+17 NFS=7.20E+11 VMAX=1.8E+05 ETA=2.125E-02
  + KAPPA=1E-01 CGDO=3.0E-10 CGSO=3.0E-10
  + CGBO=4.5E-10 CJ=5.50E-04 MJ=0.6 CJSW=3E-10
  + MJSW=0.35 PB=1.1

*SPICE LEVEL3 PARAMETERS
.MODEL PMOS PMOS LEVEL=3 PHI=0.7 TOX=9.5E-09 XJ=0.2U TPG=-1
  + VTO=-0.95 DELTA=2.5E-01 LD=7E-08 KP=4.8E-05
  + UO=130 THETA=2.0E-01 RSH=2.5E+00 GAMMA=0.52
  + NSUB=1.0E+17 NFS=6.50E+11 VMAX=3.0E+05 ETA=2.5E-02
  + KAPPA=8.0E+00 CGDO=3.5E-10 CGSO=3.5E-10
  + CGBO=4.5E-10 CJ=9.50E-04 MJ=0.5 CJSW=2E-10
  + MJSW=0.25 PB=1
.end

Spice3 Simulation Results:

Operating Point

Mos3: Level 3 MOSfet model with Meyer capacitance model

<table>
<thead>
<tr>
<th>device</th>
<th>m6</th>
<th>m4</th>
<th>m3</th>
<th>m5ref</th>
<th>m7</th>
<th>m5</th>
</tr>
</thead>
<tbody>
<tr>
<td>model</td>
<td>nmos</td>
<td>nmos</td>
<td>nmos</td>
<td>pmos</td>
<td>pmos</td>
<td>pmos</td>
</tr>
<tr>
<td>id</td>
<td>0.000118</td>
<td>4.14e-05</td>
<td>4.37e-05</td>
<td>0.0001</td>
<td>0.000118</td>
<td>8.52e-05</td>
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<tr>
<td>vgs</td>
<td>0.783</td>
<td>0.907</td>
<td>0.907</td>
<td>1.33</td>
<td>1.33</td>
<td>1.33</td>
</tr>
<tr>
<td>vds</td>
<td>1.48</td>
<td>0.783</td>
<td>0.907</td>
<td>1.33</td>
<td>1.82</td>
<td>0.896</td>
</tr>
<tr>
<td>vbs</td>
<td>-0.000236</td>
<td>-8.29e-05</td>
<td>-8.73e-05</td>
<td>-0.00025</td>
<td>-0.000295</td>
<td>-0.000213</td>
</tr>
<tr>
<td>von</td>
<td>0.542</td>
<td>0.602</td>
<td>0.593</td>
<td>-0.735</td>
<td>-0.676</td>
<td>-0.787</td>
</tr>
<tr>
<td>vdsat</td>
<td>0.228</td>
<td>0.274</td>
<td>0.28</td>
<td>-0.546</td>
<td>-0.596</td>
<td>-0.503</td>
</tr>
<tr>
<td>rs</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
</tr>
<tr>
<td>rd</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2.5</td>
<td>2.5</td>
<td>2.5</td>
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<tr>
<td>gm</td>
<td>0.000812</td>
<td>0.000227</td>
<td>0.000233</td>
<td>0.00032</td>
<td>0.000343</td>
<td>0.000299</td>
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<tr>
<td>gds</td>
<td>7.71e-06</td>
<td>2.83e-06</td>
<td>2.87e-06</td>
<td>4.19e-06</td>
<td>4.64e-06</td>
<td>3.81e-06</td>
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<tr>
<td>gmb</td>
<td>0.000204</td>
<td>5.95e-05</td>
<td>6.1e-05</td>
<td>5.45e-05</td>
<td>5.78e-05</td>
<td>5.15e-05</td>
</tr>
<tr>
<td>cbd</td>
<td>1.92e-14</td>
<td>2.69e-15</td>
<td>2.61e-15</td>
<td>1.71e-14</td>
<td>1.58e-14</td>
<td>1.87e-14</td>
</tr>
<tr>
<td>cbs</td>
<td>2.91e-14</td>
<td>3.45e-15</td>
<td>3.45e-15</td>
<td>2.48e-14</td>
<td>2.48e-14</td>
<td>2.48e-14</td>
</tr>
<tr>
<td>cgs</td>
<td>4.85e-15</td>
<td>1.21e-15</td>
<td>1.21e-15</td>
<td>2.18e-15</td>
<td>2.18e-15</td>
<td>2.18e-15</td>
</tr>
<tr>
<td>cgd</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>cgb</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Mos3: Level 3 MOSfet model with Meyer capacitance model

<table>
<thead>
<tr>
<th>device</th>
<th>m2</th>
<th>m1</th>
</tr>
</thead>
<tbody>
<tr>
<td>model</td>
<td>pmos</td>
<td>pmos</td>
</tr>
<tr>
<td>id</td>
<td>4.15e-05</td>
<td>4.35e-05</td>
</tr>
<tr>
<td>vgs</td>
<td>0.904</td>
<td>0.925</td>
</tr>
<tr>
<td>vds</td>
<td>1.62</td>
<td>1.5</td>
</tr>
<tr>
<td>vbs</td>
<td>-0.000104</td>
<td>-0.000109</td>
</tr>
<tr>
<td>von</td>
<td>-0.699</td>
<td>-0.714</td>
</tr>
<tr>
<td>vdsat</td>
<td>-0.215</td>
<td>-0.221</td>
</tr>
<tr>
<td>rs</td>
<td>2.5</td>
<td>2.5</td>
</tr>
<tr>
<td>rd</td>
<td>2.5</td>
<td>2.5</td>
</tr>
<tr>
<td>gm</td>
<td>0.000362</td>
<td>0.00037</td>
</tr>
</tbody>
</table>
AC Analysis for GAIN:

gain1: gain from vin differential to d2:  
\[
gm_{1,2} / (gds_4 + gds_2) = 34 \text{ dB}  
\]  
(AC simulation 34.05 dB)

gain2: gain from d2 to out:  
\[
gm_6 / (gds_6 + gds_7) = 36.36 \text{ dB}  
\]  
(AC simulation 36.36 dB)

gain from vin differential to d1:  
\[
gm_{1,2} / 2 / gm_3 = -2 \text{ dB}  
\]  
(AC simulation -1.0 dB)

AC Analysis (Cc=0)
Pole-zero Analysis (Cc=0)

WinSpice -> pz inp inn out 0 vol pol

Pole analysis ...

<table>
<thead>
<tr>
<th>Pole</th>
<th>Real</th>
<th>Imag</th>
</tr>
</thead>
<tbody>
<tr>
<td>pole(1)</td>
<td>-8.42399e+09</td>
<td>0.000000e+00</td>
</tr>
<tr>
<td>pole(2)</td>
<td>-5.76236e+09</td>
<td>4.013318e+09</td>
</tr>
<tr>
<td>pole(3)</td>
<td>-5.76236e+09</td>
<td>-4.01332e+09</td>
</tr>
<tr>
<td>pole(4)</td>
<td>-1.30504e+08</td>
<td>0.000000e+00</td>
</tr>
<tr>
<td>pole(5)</td>
<td>-1.18917e+06</td>
<td>0.000000e+00</td>
</tr>
</tbody>
</table>

Estimations:

pole: at node d2
\[
\frac{(gds2+gds4)/(cgs6+cdb4+cdb2+cgd6(1+gain2))}{(4.3u+2.83u)/(4.85f+2.7f+32.1f+0(1+66))/2\pi} = 28.61 \text{ MHz}
\]
\[
cgd6 = cgdo \times w6 = 3f
\]
\[
(4.3u+2.83u)/(4.85f+2.7f+32.1f+3f(1+66))/2\pi = 4.93 \text{ MHz}
\]

pole: at node out
\[
\frac{(gds6+gds7)/(cdb6+cdb7+cgd6+cgd7+c)}{7.7u+4.4u)/(19.2f+15.8f+3f+1.75f+10p)/2\pi} = 192.6 \text{ kHz}
\]

pole: at node d1
\[
\frac{(gm3)/(cgs3+cgs4+cdb3+cdb1)}{(233u)/(1.21f+1.21f+2.61f+32.1f)/2\pi} = 998 \text{ MHz}
\]

Extra simulations: no ac source at vin but an itest ac source into d2:
- conductance ~7u
- capacitance ~45fF
- pole ~ 24.6MHz
itest into out:
  conductance ~12.3u
  capacitance ~10.042pF
  pole ~ 195khz

Conclusion: dominant (first) pole at the output for the present sizing !! not at the intermediary node d1 ...

Maximum frequency to where we can push the output pole is approximately $\frac{gm6}{(2\pi CL)} = 13\text{MHz}$. This output pole is then the non dominant pole of open loop transfer function. The GBW needs to be at least half the non-dominant pole to have a good phase margin. So, GBW is maximum about $13/2\text{MHz}$. DC Gain ~ 70dB, this means BW of about $13/2/70\text{dB} = 2\text{kHz}$.

$$\text{BW} \approx \frac{(gds4+gds2)}{(2 \pi Cc \cdot \text{gain2})} \Rightarrow Cc \approx 8.5\text{pF}$$

Remark: where is the RHP zero going to be ... $\frac{gm6}{(2 \pi Cc)} = 15\text{Mhz}$ – can potentially interfere ...

AC Simulation:

***************
** Cc=8.5p **
***************
ac sim
freq mag(out) db phase(out) deg
6.272727e+06 2.980612e-02 -1.381222e+02
6.303030e+06 -1.371481e-02 -1.383284e+02

PhaseMargin = 180+phase(out) = 42 degrees

***************
** Cc=10p **
***************
ac sim
freq    mag(out) db     phase(out) deg
5.454545e+06    7.446248e-02   -1.355930e+02
5.545455e+06   -6.844927e-02   -1.362750e+02

Unity Gain Frequency = 5.5 MHz

Phase Margin = 180-136 = 44 degrees

freq    mag(out) db     phase(out) deg
1.258925e+07 -7.143873e+00   -1.784467e+02
1.584893e+07 -9.127555e+00    1.682966e+02

Gain Margin = 7dB

Pole-Zero analysis

Pole-Zero analysis ...

real(pole(1)) = -1.96549e+13
imag(pole(1)) = 0.000000e+00
real(pole(2)) = -7.34013e+11
imag(pole(2)) = 0.000000e+00
real(pole(3)) = -8.50074e+09
imag(pole(3)) = 0.000000e+00
real(pole(4)) = -5.66561e+09 \    | complex poles: wn = 6.17 Grad/sec
imag(pole(4)) = 2.616092e+09    | fn = 982 MHz
real(pole(5)) = -5.66561e+09 /
imag(pole(5)) = -2.61609e+09
real(pole(6)) = -8.26867e+07 => 13MHz
imag(pole(6)) = 0.000000e+00
real(pole(7)) = -1.03976e+04 => 1.6kHz
imag(pole(7)) = 0.000000e+00
real(pole(8)) = -5.72170e-03 => miliHz due to dc feedback network
imag(pole(8)) = 0.000000e+00

WinSpice 86 -> pz inp inn out 0 vol pol

WinSpice 86 -> pz inp inn out 0 vol zer
Pole-Zero analysis ...
Warning: Pole-zero iteration limit reached; giving up after 259 trials

Still the values below look more or less ok ...

real(zero(1)) = -9.65642e+09
imag(zero(1)) = 0.000000e+00
real(zero(2)) = -5.99958e-03
imag(zero(2)) = 0.000000e+00
real(zero(3)) = 8.131073e+07 RHP ... 12.93 MHz
imag(zero(3)) = 0.000000e+00

CONCLUSION:
At this point we have an opamp with:
• a unity gain frequency of 5.5MHz,
• a DC gain of 69dB,
• a first pole at 1.6kHz
• a phase margin of 44 degrees
• a gain margin of 7 dB
• a power consumption of approx. 3*100uA*3.3V = 1mW
• for a load capacitance of 10pF and a compensation capacitance of 10pF.

Remarks:
This is of course just a crude illustration and much more work is needed to polish this design. Some of the things that have not been considered:
• input and output voltage ranges
• sensitivity to temperature variations, supply voltage variations and process variations
• sensitivity to load variations
• time domain response
• systematic and random offset voltages
• noise performance
• ..... 

This opamp design was simulated with level 3 MOS models; level 3 models are known to only poorly model the output impedance which typically result in too high gain estimations ....