ELEN E6312
Spring 2004
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Final

Instructions – PLEASE READ:

- ***You are allowed to use a calculator; please CLEAR the calculator memory before the exam!***
- ***You are allowed to use one side of a letter size sheet with formulas; no text or schematics allowed!***
- Clearly write your name on every page and every examination booklet you hand in.
- Do your derivations and calculations in the examination booklets. Clearly indicate which question the derivation is for.
- Give all answers their appropriate S.I. Unit or indicate that the number is unitless.
- Hand in clean and clear derivations; annotate the steps in your derivations with a concise description.
- **You are graded for your derivations.** ***Results without a clear derivation do not receive a grade.***
- **If you think information is missing to solve the question, make a reasonable assumption and document your assumptions.**
- **Always make reasonable simplifications but document and justify which approximations you are making.**

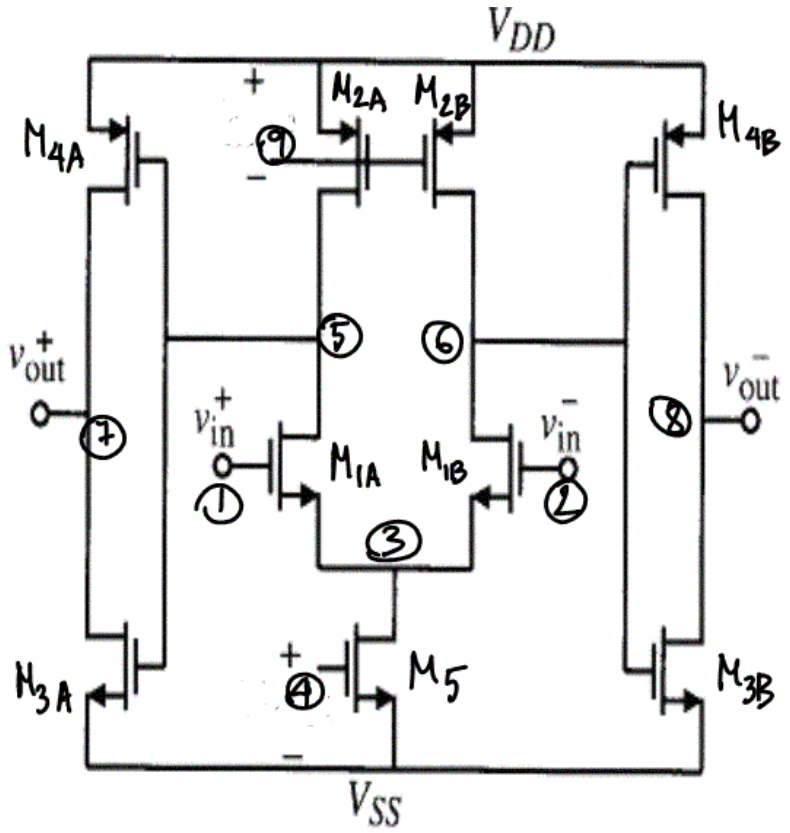
You can assume the following transistor characteristics:

- $(uC_{ox})_{nMOS} = 110$ uA/V^2 and $(uC_{ox})_{pMOS} = 50$ uA/V^2
- $V_{Tn} = |V_{Tp}| = 0.7$ V
- $V_{ALn} = 25$ V/um; $V_{ALp} = 20$ V/um
- Coxn = Coxp =2.5fF/um2; Cgdon = Cgdop = 0.2fF/um
- Cjdb=0.6fF/um2; length drain/source extension: 1.8um
    - you can ignore perimeter capacitance and voltage dependence for your junction capacitance calculations
    - you should assume NON-fingered devices

For devices in *strong inversion*, you can use the following simplified I/V relationships:

- Saturation: $I_{DS} = u\ C_{ox} / 2\ (W/L)\ (V_{GS}-V_T)^2\ (1 + V_{DS}/V_A)$
- Non-Saturation: $I_{DS} = u\ C_{ox}\ (W/L)\ (V_{GS}-V_T)\ V_{DS}$

Good luck !



For this question, use the device and node names as in the figure. This opamp circuit has the following parameters:

- Vdd=2.15V
- For M1a/b thru M4a/b: (W/L)=10um/1um
- For M5: (W/L)=20um/1um
- V_4 is such that I_{M5} is 100uA; V_9 is also biased appropriately for such current level in the input stage.

1) [10pts] Find the DC bias point for the circuit; you should assume that a common mode feedback circuit is present that assures that the output common mode voltage is set close to its ideal point for a maximal output signal swing; you can *ignore the effect of the output conductance* of the devices for this calculation.
   a) Put the node voltage of all nodes on the schematic.
   b) Calculate the current and the VGS-VT for all devices.
   c) Calculate the small signal equivalent circuit for all devices, including capacitances.

If you cannot find the solution to part 1, or if you want to solve the later parts first, use the following data for your calculations. Clearly indicate that you decided to use these default values in your booklet.

For transistors M1a/b and M3a/b: gm= 300uS and ro=450kOhm;
For transistors M2a/b and M4a/b: gm= 200uS and ro=450kOhm;
For transistor M5: gm= 600uS and ro=225kOhm.
For all transistors: (VGS-VT)=250mV; Cgs=14fF; Cdb=9fF; Cgdo= 2.5fF;

2) [7pts] Calculate the common mode input voltage range for V_{in}.

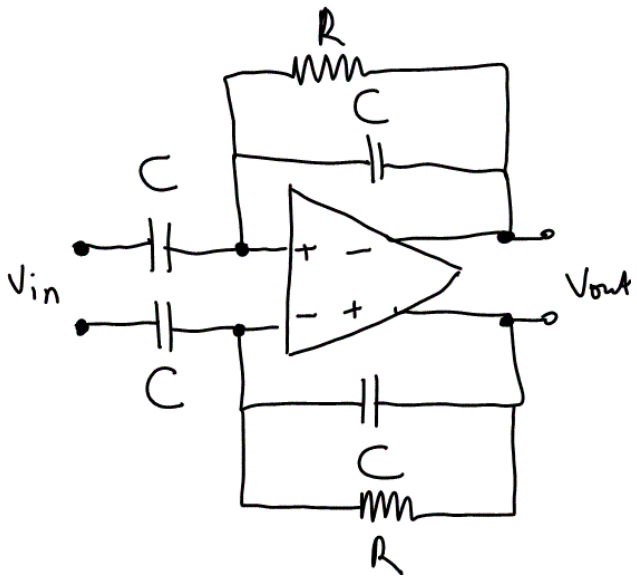
3) [8pts] Calculate the differential DC small signal gain of this circuit from V_{in} to V_{out}.

4) [5pts] Calculate the common mode DC small signal gain from the input V_{in} to the output V_{out} of this circuit; you can assume the common mode feedback loop is not active.

5) [25pts] Assume the amplifier is used in an application with unity feedback and with as a load a 100fF capacitor to ground on each output node.
   a) **Estimate** the open loop differential mode transfer function (differential in => differential out) of the amplifier and make a Bode plot for the transfer function; you do not need to do an exact calculation but should use typical assumptions and estimate the frequency response; calculate the important poles and zeros of this amplifier.
   b) You have two capacitors of your free choice of value and two resistors of 1KOhm, 2KOhm, or 3KOhm. You cannot freely choose the resistor value but have to pick it from these three values. The resistors also have a +/- 30% variation in their value.
      i) Indicate on the schematic where you will place these components to obtain as large a gain-bandwidth as possible with a phase margin of better than 55degrees for this amplifier in unity feedback.
      ii) Calculate the value of the capacitors.
      iii) Choose a value for the resistors.
      iv) Make a Bode plot of the open loop gain of the amplifier after compensation.

   For the solution of this part you can report your first pass estimate; you do not have to iterate over the calculations.

6) [10pts] Propose a common mode feedback scheme for this amplifier. Discuss the merits and disadvantages of your chosen approach. You do not need to do any calculations for this part, just give a schematic and a qualitative description of the operation and characteristics of the circuit.



7) [5pts] Your colleague reuses your amplifier with your compensation scheme for their application in the above configuration where C is 200fF. Will their feedback circuit have more or less phase margin? ***Explain!*** You can assume a very large resistance value so that the resistor does not affect the signal path but only provides DC feedback for proper biasing.

8) [15pts] Your design is getting really popular. Yet another colleague starts using it for a low power application; the only change they make is adjusting the bias voltages V4 and V9 so that the input stage draws only 100nA (i.e. I_{M5}=100nA). Discuss how it affects the DC gain, the gain-bandwidth and the phase margin, all for a unity-feedback configuration.

9) [15pts] Calculate the *equivalent differential input noise voltage* at low frequencies.

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